NEC
ELECTRON DEVICE

BIPOLAR INTEGRATED CIRCUIT

μPC1823A

PLL IF SIGNAL PROCESSOR FOR TV

The μPC1823A is an IF (Intermediate Frequency) signal processor for TV. This LSI contains PIF (Picture IF) and SIF (Sound IF) processing function in one chip, and support not only PAL-B/G but SECAM-L system.

The fine DG (Differential Gain) and DP (Differential Phase) characteristics are achieved by PLL (Phase Locked Loop) synchronizing picture detection circuit.

The μPC1823A is designed for MULTISTANDARD and PAL/SECAM standard TV. Almost alignment and switches functions except VCO (Voltage Controlled Oscillator) are controlled through I²C bus control. This LSI is molded in 42 pins plastic SDIP (600mil).

FEATURES

- System: PAL-B/G, SECAM-L system in one chip.
- The filter for AFT (Automatic Fine Tuning) is not necessary.
- PLL synchronizing detection for PIF processing.
  Fine DG and DP characteristics are achieved (DG: 2%, DP: 2deg typ.).
- PLL split carrier system for SIF processing.
  High input sensitivity and fine BUZZ characteristics are achieved.
- Keyed AGC is equipped for SECAM-L, and Peak AGC for PAL-B/G.
  On chip Keyed pulse generator reduces external components.
- On chip AM (Amplitude Modulation) sound detector is equipped for SECAM-L, and FM (Frequency Modulation) sound detector is equipped for PAL-B/G.
- AFT polality switch is on chip.
- Built-in I²C bus interface circuit.
  Almost alignment except VCO are controlled through I²C bus.
  - IF AGC for SECAM-L is controlled by 6 bit D/A.
  - RF AGC is controlled by 6 bit D/A.
  - 7 switches are controlled.

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPC1823ACU	42-pin plastic SHD (600mil)	Standard

Purchase of NEC I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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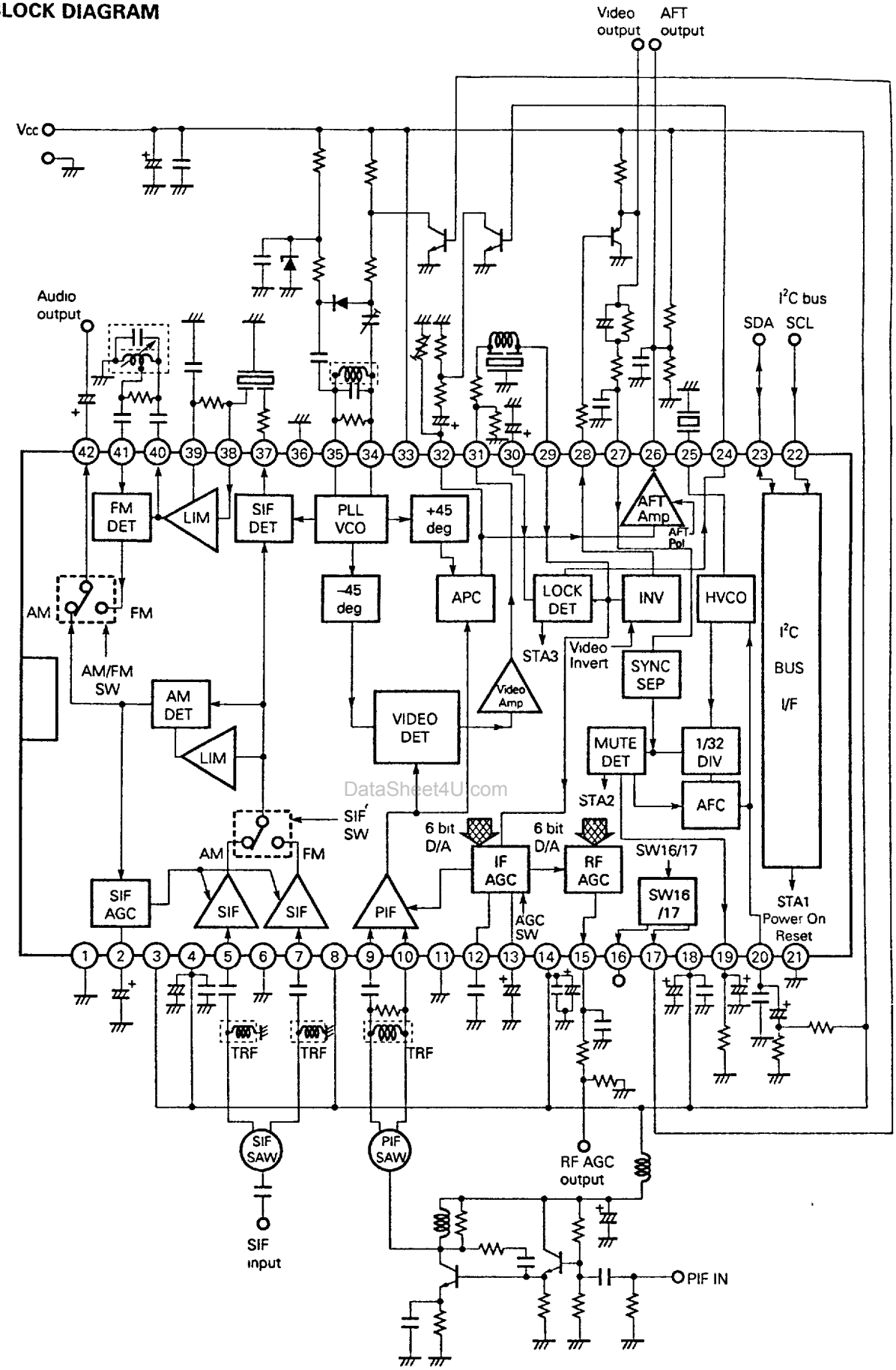
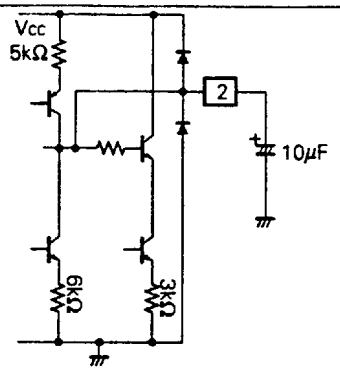
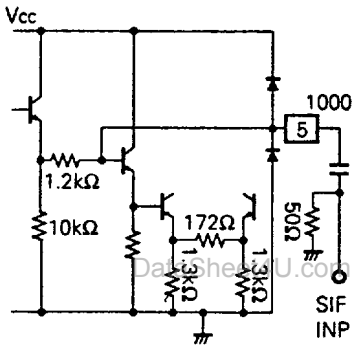
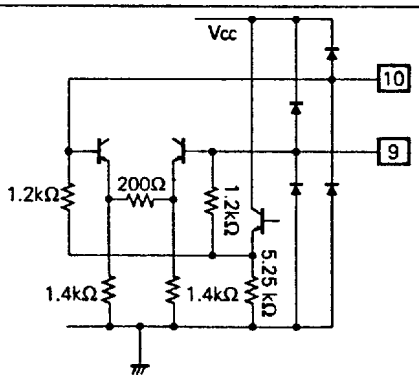
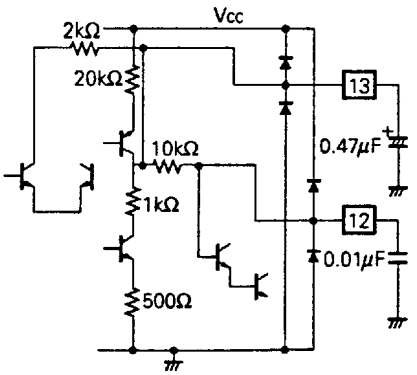
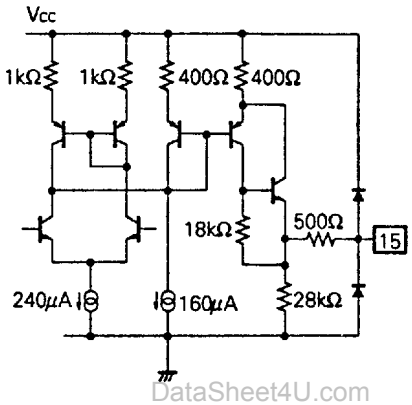
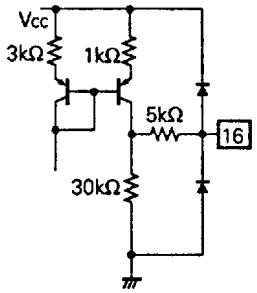
BLOCK DIAGRAM

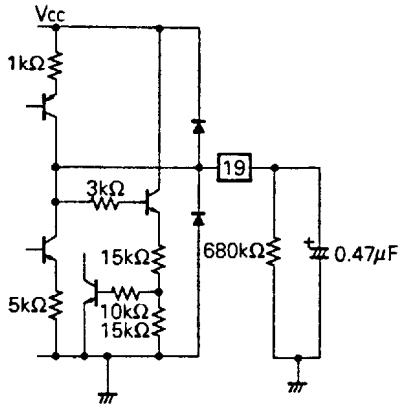
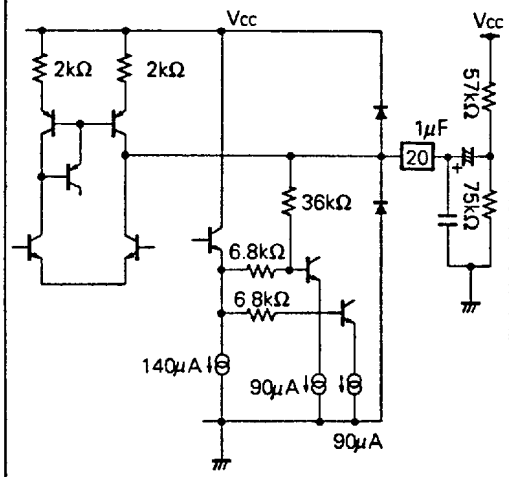
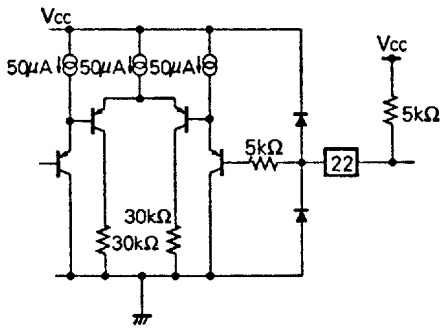


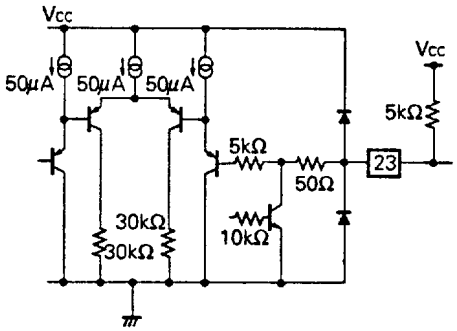
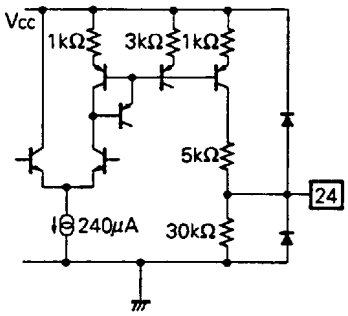
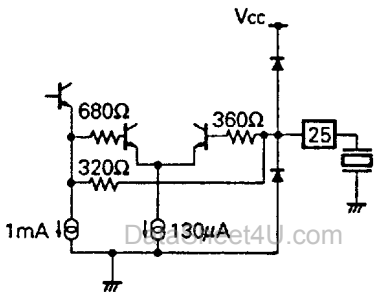
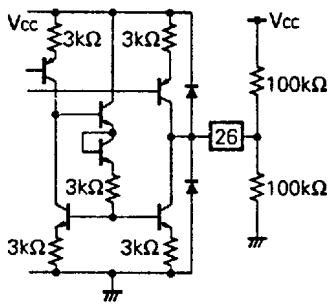
PIN CONNECTION (Top View)

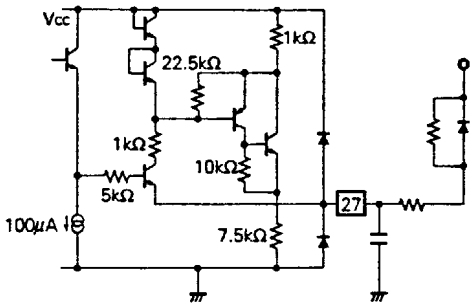
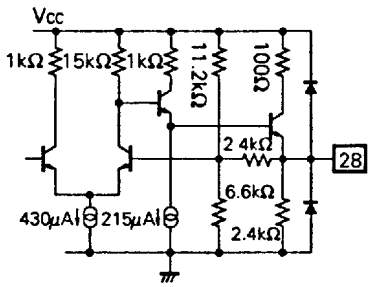
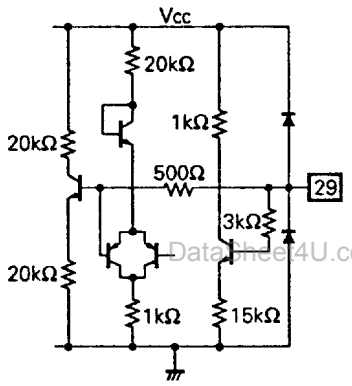
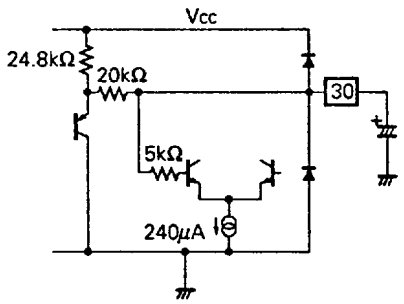
PIN DESCRIPTION

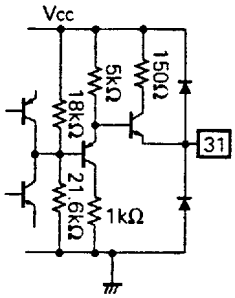
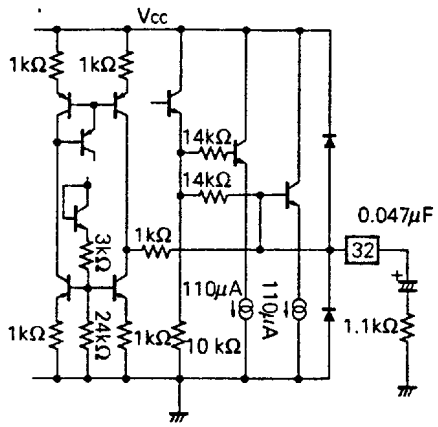
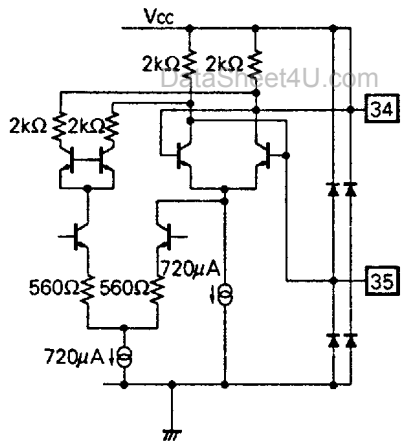
Pin No.	Pin Name	Equivalent Circuit	Function
1	SIF GND (0V)		GND pin for AM detector, FM detector, FM limiter, SIF AGC and AF OUT
2	SIF AGC FILTER (8.4V)		Capacitor connect pin of SIF AGC filter sets up to time constant of AGC.
3	SIF Vcc (9V)		Power supply for AM detector, FM detector, FM limiter, SIF AGC and AF OUT Vcc=8 to 10V
4	SIF AMP Vcc (9V)		Power supply for SIF amplifier Vcc=8 to 10V
5	SIF INPUT (3.0V)		Input pin for SIF AM amplifier Input impedance is approximately 1kΩ.
6	SIF AMP GND (0V)		GND pin for SIF amplifier
7	SIF FM INPUT (3.0V)	Similar to pin 5	Input pin for SIF FM amplifier Input impedance is approximately 1kΩ.
8	PIF AMP Vcc (9V)		Power supply for PIF amplifier Vcc=8 to 10V
9, 10	PIF AMP INPUT (2.4V)		Input pin for PIF amplifier Both pins are differential input. Input impedance is approximately 1kΩ.

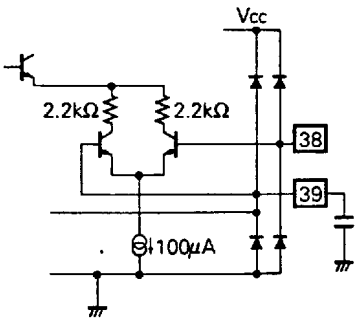
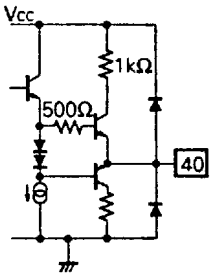
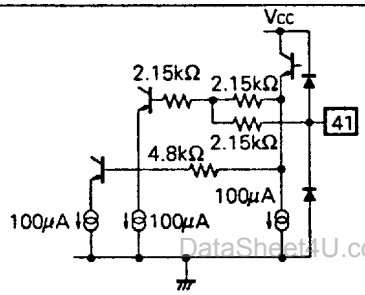
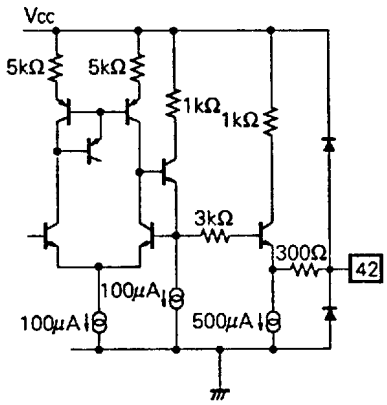
Pin No.	Pin Name	Equivalent Circuit	Function
11	PIF AMP GND (0V)		GND pin for PIF amplifier, PIF, IF/AGC, D/A converter
12, 13	PIF AGC FILTER (8.8V)		Capacitor connect pin of PIF AGC filter, sets up to time constant of AGC.
14	AGC Vcc (9V)		Power supply for PIF IF/RF AGC, D/A converter Vcc=8 to 10V
15	RF AGC OUTPUT (8.3V)		Output pin of RF AGC control signal used as tuner AGC signal
16	SIF TRAP SW OUT (6.9V)		Output pin of drive signal for SIF TRAP switch (Current output of approximately 170μA)
17	VCO FREQ SW OUT (6.9V)		Output pin of drive signal for VCO f_0 (Current output of approximately 170μA)
18	SYNC SEP Vcc (9V)	Similar to pin 16	Power supply for synchronization separator, linear interface. Vcc=8 to 10V

Pin No.	Pin Name	Equivalent Circuit	Function
19	MUTE DET FILTER (8V)		MUTE detector filter pin, sets up to time constant. When Horizontal Lock is unlocked, this pin outputs low level (about 1V).
20	AFC FILTER (7.5V)		AFC filter pin, sets up to time constant of AFC filter.
21	DIGITAL GND (0V)		GND pin for 32f_H PLL, I²C bus
22	SCL (5V)		SCL line of I²C bus Logic level is CMOS compatible.

Pin No.	Pin Name	Equivalent Circuit	Function
23	SDA (5V)		SDA line of I²C bus Logic level is CMOS compatible.
24	PLL LOCK SW OUTPUT (7.3V)		Output pin of drive signal for LOCK switch (Current output, approximately 200μA). When PLL is locked, this pin outputs high level.
25	32fH X'tal (5.4V)		X'TAL pin for 500 kHz HVCO
26	AFT OUTPUT (4.5V)		AFT output pin

Pin No.	Pin Name	Equivalent Circuit	Function
27	SYNC SEP INPUT (6.6V)		Synchronization separator input pin
28	VIDEO INV OUTPUT (5.6V)		Video inverter output pin
29	VIDEO INV INPUT (4.9V)		Video inverter input pin
30	LOCK DET FILTER (5.6V)		Capacitor connect pin of LOCK detector filter, sets up to time constant.

Pin No.	Pin Name	Equivalent Circuit	Function
31	VIDEO DET OUTPUT (4.9V)		Video detector output pin
32	PLL APC FILTER (4.6V)		APC filter pin of PLL loop for PIF, sets up to time constant.
33	PLL VCO Vcc (9V)		Power supply for APC, SIF detector, PLL VCO, video inverter, video amplifier, AFT, video detector, LOCK detector Vcc=8 to 10V
34, 35	PLL VCO COIL (8.4V)		Oscillator coil pin for PLL VCO
36	PLL VCO GND (0V)		GND pin for APC, SIF detector, PLL VCO, video inverter, video amplifier, AFT, video detector, LOCK detector

Pin No.	Pin Name	Equivalent Circuit	Function
37	SIF DET OUTPUT (6.4V)		SIF detector output pin
38	FM LIMITER INPUT (2.2V)		FM limiter input pin
39	FM LIMITER FILTER (2.2V)		Bipass capacitor connect pin of SIF limiter
40	FM LIMITER OUTPUT (3.6V)		FM limiter output pin
41	FM DET INPUT (3.9V)		FM detector input pin
42	SOUND DET OUTPUT (3.1V)		Sound (AM/FM) detector output pin

ABSOLUTE MAXIMUM RATINGS (Ta = +25°C)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{CC}	11	V
Serial bus input voltage SCL and SDA	V22, V23	0 to 6	V
Power dissipation	Pd	910 (Ta = +70 °C)	mW
Operating temperature	T_{OPT}	−20 to +70	°C
Storage temperature	T_{STG}	−40 to +135	°C

RECOMMENDED OPERATING CONDITION (Ta = +25°C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	8.0	9.0	10.0	V
Serial bus input high level voltage	V_{IH}	3.5		5.0	V
Serial bus input low level voltage	V_{IL}	0		1.5	V

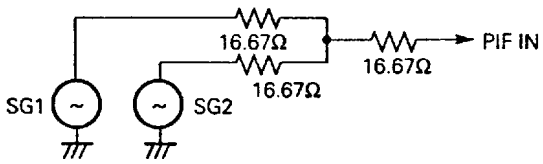
ELECTRICAL CHARACTERISTICS (Ta = +25±3°C, Vcc = 9V, unless otherwise specified)
Concerning Notes, see **TEST CONDITION LIST** on the following page.

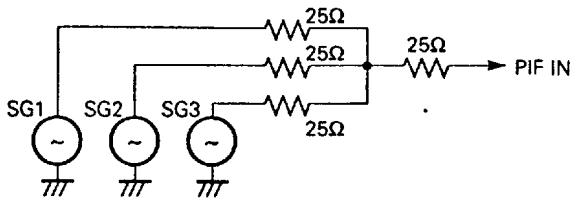
Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
Supply current on Video circuit	I_{CCP}	No signal. Input current to pin 8, 14, 18, 33		–	45	60	mA
Video detection output DC voltage 1	V_{oPDC1}	No signal. B/G mode Output DC voltage at pin 28.		5.5	5.7	5.9	V
Video detection output DC voltage 2	V_{oPDC2}	No signal. L mode Output DC voltage at pin 28.		2.7	2.9	3.1	V
Sync tip level 1	V_{sync1}	Note 1 B/G mode		3.0	3.4	3.7	V
Sync tip level 2	V_{sync2}	Note 2 L mode		2.6	3.0	3.3	V
Video detection output voltage	V_{oP}	Note 3 B/G mode		1.7	2.0	2.35	V
Video S/N	P/N	Note 4 B/G mode			60	–	dBμ
Input sensitivity (PIF)	$V_{iPsense}$	Note 5	B/G	–	43	47	dBμ
			L	–	43	47	
Maximum input voltage (PIF)	$V_{iP\ MAX}$	Note 5	B/G	107	110	–	dBμ
			L	105	108	–	
Video frequency response	BWP	Note 6 B/G mode		6.0	8.0	–	MHz
Differential gain 1	DG_1	Note 8 B/G mode		–	2	5	%
Differential gain 2	DG_2	Note 8 L mode		–	2	5	%
Differential phase 1	DP_1	Note 8 B/G mode		–	2	5	deg
Differential phase 2	DP_2	Note 8 L mode		–	2	5	deg
Inter-modulation (PIF)	IMP	Note 9 B/G mode		40	45	–	dB
IF AGC maximum voltage	$V_{AGCI\text{-}H}$	Note 10 B/G mode		8.2	8.6	–	V
IF AGC minimum voltage	$V_{AGCI\text{-}L}$	Note 10 B/G mode		–	3.5	3.7	V
RF AGC maximum voltage	$V_{AGCR\text{-}H}$	Note 10 B/G mode		7.0	8.0	–	V
RF AGC minimum voltage	$V_{AGCR\text{-}L}$	Note 10 B/G mode		–	0	0.5	V
RF AGC control sensitivity	μ_{VAGCR}	Set up sensitivity for I²C bus B/G mode			0.5		dB/STP
RF AGC temperature characteristic	Δ_{AGCR}	Note 7 B/G mode				3	dB
AFT maximum voltage	$V_{AFT\text{-}H}$	Note 11 B/G mode		8.0	8.7	–	V
AFT minimum voltage	$V_{AFT\text{-}L}$	Note 11 B/G mode		–	0.24	0.80	V
AFT control sensitivity	μ_{AFT}	Note 11 B/G mode		8	12	16	mV/kHz
VCO temperature characteristic	Δ_{VCO}	During 3 seconds to 3 minutes after power on. L mode		–	–	±50	kHz
APC offset adjustment resistance	R_{APC}	Note 27 No signal		510		820	kΩ
Capture range (Upper 1)	$f_{CLU\text{-}1}$	Note 12	B/G	1.0	1.94	–	MHz
		LOCK SW off	L	0.7	1.1	–	
Capture range (Lower 1)	$f_{CLL\ 1}$	Note 12	B/G	1.0	1.94	–	MHz
		LOCK SW off	L	0.7	1.1	–	

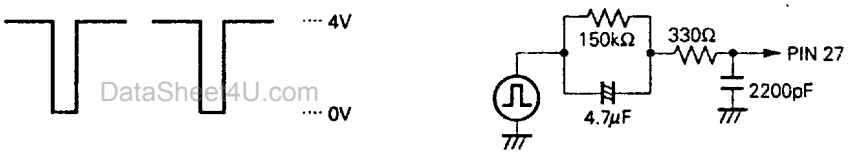
Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
Capture range (Upper 2)	f_{CLU2}	Note 12 LOCK SW on	B/G	1.0	1.94	–	MHz
			L	0.7	1.1	–	
Capture range (Lower 2)	f_{CLL2}	Note 12 LOCK SW on	B/G	1.0	1.94	–	MHz
			L	0.7	1.1	–	
Lock detection threshold voltage	V_{LOCK}	Note 13 No signal		4.3	4.6	4.9	V
RF AGC Delay point 1	V_{AGCR1}	Note 25 DATA="00H" L mode		95	–	–	dBμ
RF AGC Delay point 2	V_{AGCR2}	Note 25 DATA="10H" L mode		90	–	–	dBμ
RF AGC Delay point 3	V_{AGCR3}	Note 25 L mode DATA="00H to 3FH"		87	90	93	dBμ
RF AGC Delay point 4	V_{AGCR4}	Note 25 DATA="30H" L mode		–	–	90	dBμ
RF AGC Delay point 5	V_{AGCR5}	Note 25 No signal DATA="3FH" L mode		–	–	85	dBμ
SECAM Video detection output voltage 1	V_{oPL1}	Note 26 DATA="00H" L mode		2.4	–	–	V_{p-p}
SECAM Video detection output voltage 2	V_{oPL2}	Note 26 DATA="10H" L mode		1.6	–	–	V_{p-p}
SECAM Video detection output voltage 3	V_{oPL3}	Note 26 L mode DATA="00H to 3FH"		–	2.0	–	V_{p-p}
SECAM Video detection output voltage 4	V_{oPL4}	Note 26 DATA="30H" L mode		–	–	1.6	V_{p-p}
Horizontal oscillation starting voltage	HV_{cc-MIN}			–	5.3	6.3	V
Horizontal free run frequency	f_H	No signal		15.500	15.625	15.750	kHz
Horizontal capture range (Upper)	f_{CHU}	Note 15		400	600	–	Hz
Horizontal capture range (Lower)	f_{CHL}	Note 15		400	600	–	Hz
Supply current on Sound circuit	I_{CCS}	No signal Input current to pin 3, 4.			26	35	mA
SIF detection output voltage	V_{oS}	Note 16		100	105	110	dBμ
SIF detection intermodulation	IMs	Note 17	IMD_1	–	–43	–40	dB
			IMD_2	–	–52	–46	
FM sound detection output DC voltage	V_{oFMDC}	No signal		–	3.1	–	V
FM limiting sensitivity	$V_{iFMsense}$	Note 18		–	53	59	dBμ
FM maximum input voltage	$V_{iFM-MAX}$	Note 18		110	120	–	dBμ
FM sound output voltage	V_{oFM}	Note 19		500	630	760	mVrms
FM sound output distortion ratio	THD_{FM}	Note 19		–	0.3	1.0	%

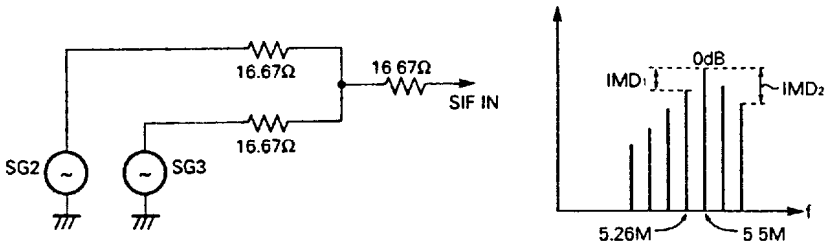
Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
AM rejection	AMR	Note 20	70dBμ		45	–	dB
			90dBμ		50	–	
FM sound S/N	S/N_{FM}	Note 21		60	70	–	dB
AM sound S/N	S/N_{AM}	Note 22		55	60	–	dB
AM sound detection output DC voltage	V_{oAMDC}	No signal		2.2	2.7	3.2	V
AM audio input sensitivity	$V_{IAMsense}$	Note 22	–3dB	39	43	47	dBμ
		[SIF AGC AMP+AM DET]	–10dB	37	41	45	
AM maximum input voltage	$V_{IAM\ MAX}$	Note 22 [SIF AGC AMP+AM DET]		104	107	–	dBμ
AM sound output voltage	V_{oAM}	Note 23		400	500	600	mVrms
FM sound output distortion ratio	THD_{AM}	Note 23	80% modulation	–	0.8	2.0	%
			50% modulation	–	0.5	1.0	
PIF input resistance	R_{IP}	Note 14		–	1.0	–	kΩ
PIF input capacitance	C_{IP}	Note 14		–	4.0	–	pF
SIF input resistance	R_{IS}	Note 14		–	1.0	–	kΩ
SIF input capacitance	C_{IS}	Note 14		–	4.0	–	pF
SIF input sensitivity	V_{Isense}	Note 24 [SIF AGC AMP+SIF DET]		36	40	44	dBμ
AM maximum input voltage	$V_{IS\text{-}MAX}$	Note 24 [SIF AGC AMP+SIF DET]		105	110	–	dBμ
FM audio input sensitivity	V_{Audsen}	Input level when –3dB down at pin 42. Output reference (0dB) at input 80dBμ signal to pin 7.		–	25	35	dBμ
I²C bus operation	———			Control to SW, D/A via I²C bus and confirm not to mismovement inputting the various data.			
Power on reset operation voltage	V_{PONRES}	Voltage when output the power on reset flag, changing supply voltage.		6.5	7.2	7.9	V

TEST CONDITION LIST (Notes in the ELECTRICAL CHARACTERISTICS)

Notes	Test Parameter	Test Conditions
Note 1	V_{sync1}	B/G system, f_{PIF}=38.9MHz, V_{in}=90dBμ Video AM modulation ratio 87.5%, Stair 10 steps signal (no chrominance signal) Input the signal to TP1 of PIF input terminal, and measure DC voltage of synchronous tip at TP2 of video output terminal with oscilloscope.
Note 2	V_{sync2}	L system, f_{PIF}=38.9MHz, V_{in}=90dBμ Video AM modulation ratio 97.0%, Stair 10 steps signal (no chrominance signal) Input signal to TP1, and measure DC voltage of sync. tip at TP2 with oscilloscope.
Note 3	V_{oP}	B/G system, f_{PIF}=38.9MHz, V_{in}=90dBμ Video AM modulation ratio 87.5%, Stair 10 steps signal (no chrominance signal) Input signal to TP1, and measure the amplitude of Video detection signal at TP2 with oscilloscope.
Note 4	P/N	B/G system, f_{PIF}=38.9MHz, V_{in}=90dBμ Video AM modulation ratio 87.5%, 100% white video signal Input signal to TP1, and measure S/N of Video detection signal at TP2 with noise meter. Measurement range: From 100kHz to 4MHz
Note 5	$V_{iPsense}$ $V_{iP\text{-}MAX}$	B/G system, f_{PIF}=38.9MHz, V_{in}=variable Video AM modulation ratio 87.5%, Stair 10 steps signal (no chrominance signal) Input signal to TP1, and measure the amplitude of video detection signal at TP2 with oscilloscope. When input 90dBμ of input video signal voltage, video detection output signal is 0dB. And decrease the input video signal voltage from 90dBμ until video detection voltage of TP2 becomes −3dB. This video detection output voltage is input sensitivity ($V_{iPsense}$). Similar $V_{iP\text{-}MAX}$ with $V_{iPsense}$. Increase the input video signal voltage from 90dBμ until video detection voltage at TP2 becomes −1dB. This video detection output voltage is MAX. input voltage ($V_{iP\text{-}MAX}$). (In case of L system, Video AM modulation is ratio 97.0%)
Note 6	BW_P	B/G system a. Input signal to TP1 as followings; SG1:f_1=38.9MHz, V_{in}=90dBμ, CW (no modulation, only carrier) SG2:f_2=37.9MHz, V_{in}=70dBμ, CW (no modulation, only carrier) Signal is mixed SG1 with SG2 by below figure (RS=50Ω)  b. Measure amplitude of 1MHz level at TP2 with oscilloscope, and determine this level as 0dB. c. Decrease frequency (f_2) until amplitude of (f_1–f_2) level at TP2 becomes −3dB. d. Measure frequency (f_2). e. Video frequency response (BW_P) is leaded by this f_2 as following; BW_P=38.9 − f_2 (MHz)

Notes	Test Parameter	Test Conditions
Note 7	Δ_{AGCR}	B/G system, f_{PIF}=38.9MHz, V_{in}=90dBμ Video AM modulation ratio 87.5%, Stair 10 steps signal (no chrominance signal) Input the signal to TP1, and measure RF AGC output voltage of RF AGC output terminal at TP3 with voltmeter. And then select RF AGC delay data by I²C bus to be 4.5V of RF AGC output voltage. Change ambient temperature Ta from –25°C to 75°C and keep RF AGC output voltage to constant 4.5V by changing input video signal voltage. Measure this changing level of input video signal voltage at TP1 with oscilloscope.
Note 8	DG_1, DG_2 DP_1, DP_2	B/G system, f_{PIF}=38.9MHz, V_{in}=90dBμ Video AM modulation ratio 87.5%, Stair 10 steps signal (no chrominance signal) Input signal to TP1, and measure DG, DP of video detection signal at TP2 with vector scope.
Note 9	IM_P	B/G system a. Measure DC voltage of IF AGC filter at TP4, when input 90dBμ of input video signal to TP1. Determine this voltage as Vset voltage. b. Input signal to TP1 as followings; SG1:f_1=38.9MHz, V_{in}=90dBμ, CW SG2:f_2=34.47Hz, V_{in}=80dBμ, CW (chrominance) Sg3:f_3=33.40Hz, V_{in}=80dBμ, CW (sound) Signals are mixed SG1 with SG2 and SG3 by below figure (RS=50Ω)  c. Input Vset voltage to TP4 and then measure at TP5 with spectrum analyzer. d. IM_P is 1.07MHz level of 4.43MHz video detection output signal.
Note 10	V_{AGCI-H} V_{AGCI-L} V_{AGCR-H} V_{AGCR-L}	B/G system, f_{PIF}=38.9MHz, V_{in}=variable Video AM modulation ratio 87.5%, Stair 10 steps signal (no chrominance signal) Input signal to TP1. Change input video signal voltage of TP1, and measure MAX. and MIN. voltage of IF AGC at TP4. RF AGC is similar with IF AGC. Change input video signal voltage of TP1, and measure MAX. and MIN. voltage of RF AGC at TP3. (MAX. value:V_{in}=106dBμ, MIN.:V_{in}=no signal)
Note 11	V_{AFT-H} V_{AFT-L} μ_{AFT}	B/G system, f_{PIF}=variable, V_{in}=90dBμ, CW Input signal to TP1. a. Change f_{PIF} at center of 38.9MHz, and measure MAX. and MIN. voltage of AFT output voltage at TP6. b. Measure frequency of f_{PIF} as f_1 when AFT output voltage of TP6 is 3V, and when TP6 is 6V, measure frequency as f_2. Determine this frequency range (f_1–f_2) as Δf, AFT sensitivity is described as following; AFT sensitivity:$\mu_{AFT}=\frac{300mV}{\Delta fkHz}$ (mV/kHz)

Notes	Test Parameter	Test Conditions
Note 12	f_{CLU-1} f_{CLU-2} f_{CLL-1} f_{CLL-2}	B/G system, f_{PIF}=38.9±5MHz, V_{in}=90dBμ Video AM modulation ratio 87.5%, Stair 10 steps signal (no chrominance signal) Iput signal to TP1 as following. a. Capture range f_{CLU-1}, f_{CLL-1} Lock detector remove from APC filter (SW1 is ⓑ side). • f_{CLU-1} Increase f_{PIF} until VCO unlock (Measure at TP7 with oscilloscope). And then decrease f_{PIF} until VCO lock again, and measure f_{PIF}. This lock frequency is f_{CLU-1}. • f_{CLL-1} Decrease f_{PIF} until VCO unlock. And then increase f_{PIF} until VCO lock again, and measure f_{PIF}. Determine this lock frequency as f_{CLL-1}. b. Capture range f_{CLU-2}, f_{CLL-2} Lock detector connect to APC filter (SW1 is ⓑ side). Measure f_{CLU-2} and f_{CLL-2} by similar methods with f_{CLU-1} and f_{CLL-1}. By similar methods, video AM modulation ratio is 97%, using L system.
Note 13	V_{LOCK}	Input DC voltage to TP8 (Lock detector filter), and change this voltage. Measure DC voltage at TP8 when lock SW change from off to on (from low to high). (See the state of lock SW at TP7 with oscilloscope).
Note 14	R_{ip}, C_{ip} R_{is}, C_{is}	Measure input resistance and capacitance at IC pin directly with impedance analyzer. Measurement frequency is 1MHz.
Note 15	f_{CHU} f_{CHL}	Input signal to TP9 (synchronization separator input) and SW2 is open. Amplitude from 0V to 4V, duty cycle 90%.  • f_{CHU} Increase input frequency until key pulse output waveform does not synchronize with input signal. And decrease frequency until key pulse output waveform synchronizes with input signal, and measure the frequency. Determine this frequency as f_{CHU}. • f_{CHL} Decrease input frequency until key pulse output waveform does not synchronize with input signal. And increase frequency until key pulse output waveform synchronizes with input signal, and measure the frequency. Determine this frequency as f_{CHL}.
Note 16	V_{OS}	Set signal generator as followings (sound mode:FM); SG1:f_{PIF}=38.9MHz, V_{in}=90dBμ, CW SG2:f_{SIF}=33.40Hz, V_{in}=90dBμ, CW Input SG1 signal to TP1, and SG2 signal to TP10 of SIF input terminal, and measure amplitude of 5.5MHz level of SIF DET OUTPUT with oscilloscope at TP11.

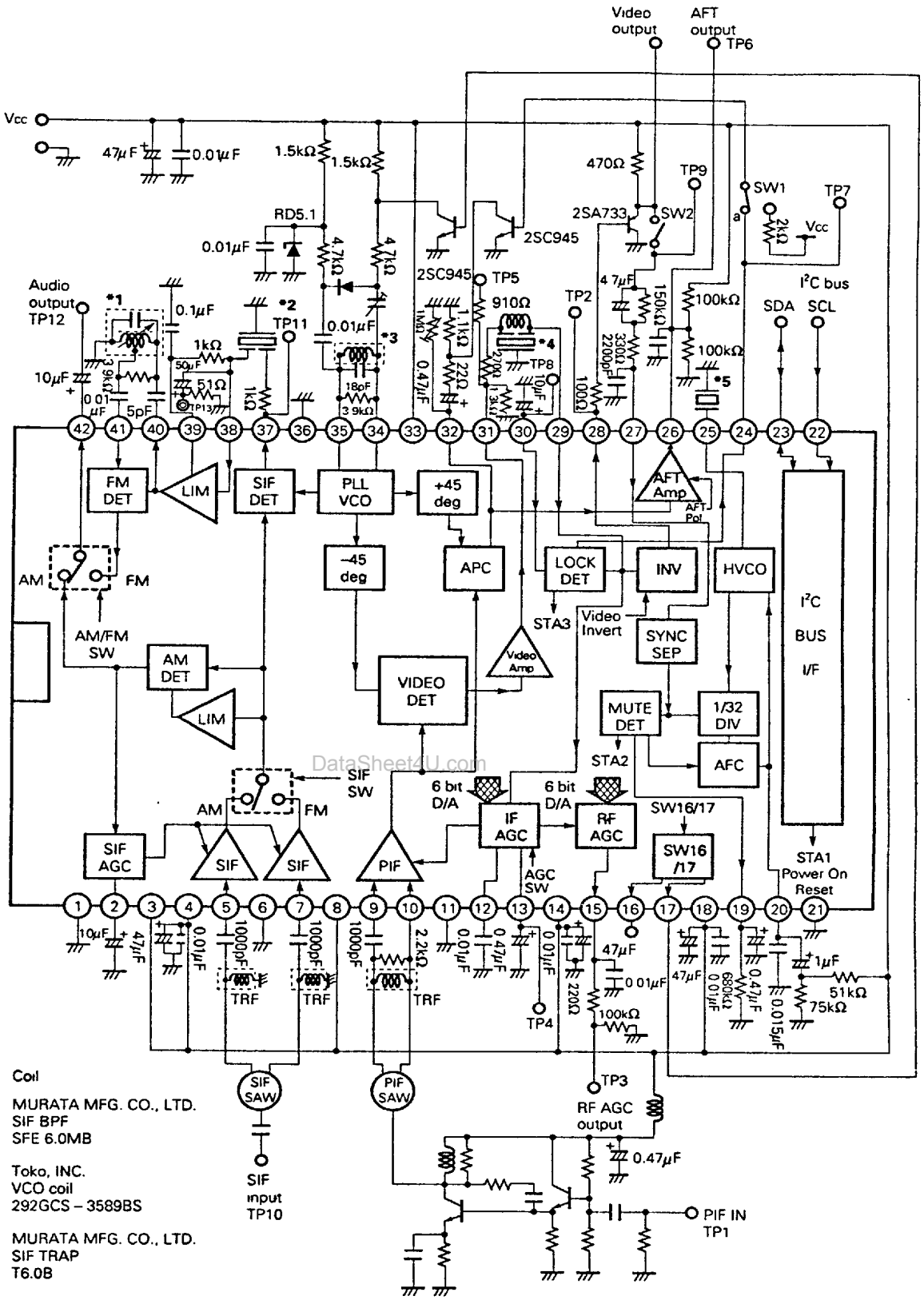
Notes	Test Parameter	Test Conditions
Note 17	IM_3	a. Input signal to TP10 as followings (sound mode:FM); SG1:f_1=38.9MHz, V_{in}=90dBμ, CW SG2:f_2=33.40Hz, V_{in}=90dBμ, CW SG3:f_3=33.16Hz, V_{in}=83dBμ, CW Signal is mixed SG2 and SG3 by below figure.  Input SG1 signal to TP1 (PIF input). Input signal mixed SG2 signal and SG3 signal to TP10 (SIF input). b. Measure 5.5MHz level of SIF DET OUTPUT at TP11 with spectrum analyzer, and determine the 5.5MHz level as 0dB. c. Measure the difference level between 5.5MHz level and 5.26MHz (5.5MHz–0.24MHz) level. Determine this difference level as IMD_1. And measure the difference level between 5.5MHz level and beat level generated by each 0.24MHz except of IMD_1. Determine this difference level as IMD_2.
Note 18	$V_{IFMsense}$	Input signal to TP13 (Limiter AMP input terminal) as following. (sound mode:FM) Signal:f_C=5.5MHz, f_M=400Hz, f_{DEV}=50kHz, V_{in}=variable, sound FM modulation signal Determine the audio output (TP12) level as 0dB with input of 90dBμ to TP13. Change input signal voltage of TP13. And then measure input signal voltage when audio output becomes –3dB.
Note 19	V_{OFM}	Input signal to TP13 (sound mode:FM) as following. Signal:f_C=5.5MHz, f_M=400Hz, f_{DEV}=50kHz, V_{in}=90dBμ, sound FM modulation signal Measure amplitude and distortion rate of audio output at TP12.
Note 20	AMR	Input signal to TP13 (sound mode:FM) as following. Signal:f_C=5.5MHz, f_M=400Hz, f_{DEV}=50kHz, V_{in}=90dBμ, sound AM modulation ratio 30% Measure amplitude of audio output at TP12 and get ratio against Vin. This ratio is AMR of 90dBμ. Measuring AMR of 70dBμ is similar to AMR of 90dBμ.
Note 21	S/N_{FM}	Input signal to TP13 (sound mode:FM) as following. Signal:f_C=5.5MHz, V_{in}=90dBμ Measure effective noise level of TP12 (audio output). Get ratio between this effective noise level and Note19's audio output level (=0dB). Determine this ratio as S/N_{FM}.

Notes	Test Parameter	Test Conditions
Note 22	S/N_{AM} $V_{iAMsense}$ $V_{iAM\text{-}MAX}$	Input signal to TP10 (SIF input terminal) as following. (sound mode:FM) Signal:fc=39.2MHz, f_M=1kHz, Vin=variable, sound AM modulation ratio 80% Determine audio output (TP12) as 0dB when sound input level is 90dBμ. Change sound input level, and measure sound input level when audio output becomes –3dB or –10dB. • AM audio input sensitivity is –3dB or –10dB. • MAX. input level is –1dB. Determine audio output (TP12) as 0dB when no–modulation signal. And then measure effective noise level of TP12 (Audio output). Get ratio between this effective noise level and Note 19's audio output level (=0dB). Determine this raito as S/N_{AM}.
Note 23	V_{oAM} THD_{AM}	Input signal to TP10 (sound mode:AM) as following. Signal:fc=39.2MHz, f_M=1KHz, V_{in}=90dBμ, sound AM modulation ratio 80 or 50% Measure amplitude and distortion rate of audio output. (Pin2 of SIF AGC FILTER is 10μF.)
Note 24	$V_{iSsense}$ $V_{iS\text{-}MAX}$	Set signal generator (sound mode:FM) as followings; SG1:f_1=38.9MHz, Vin=90dBμ, CW SG2:f_2=33.40Hz, Vin=variable, CW Input SG1 signal to TP1 of PIF input, and SG2 signal to TP10 of SIF input. Determine SIF DET output level as 0dB at this time. Change SIF input voltage, and measure SIF input voltage when SIF DET output level becomes –3dB.
Note 25	V_{AGCR1} to V_{AGCR5}	Set each data from 00H to 3FH, which is to set RF AGC delay point to D/A converter by I²C bus. Measure PIF input voltage at TP1 when RF AGC voltage becomes 4.5V.
Note 26	V_{oPL1} to V_{oPL4}	Input signal to TP1 as following. L system, f_{PIF}=38.9MHz, V_{in}=90dBμ Video AM modulation ratio 97.0%, Stair 10 steps signal (no chrominance signal) Set each data from 00H to 3FH, which is to set SECAM LEVEL to D/A converter by I²C bus. And measure amplitude of video signal of VIDEO INV OUTPUT at TP2.
Note 27	R_{APC}	Set B/G system by I²C bus control (SA_0:D_5="1", D_6="1"). No input signal. TP4 connects to GND. Measure AFT DC voltage at TP6. Adjust pin32's VR (1MΩ) to set 4.5±0.05V at TP6. And then measure resistance value. Determine this value as R_{APC}.

(Switch status: SW1 is ⓐ side, SW2 is closed unless otherwise specified.)

MEASURING CIRCUIT

(Switch status: SW1 is ⓐ side, SW2 is closed unless otherwise specified)



*1. Coil

*2. MURATA MFG. CO., LTD.
SIF BPF
SFE 6.0MB

*3. Toko, INC.
VCO coil
292GCS – 3589BS

*4. MURATA MFG. CO., LTD.
SIF TRAP
T6.0B

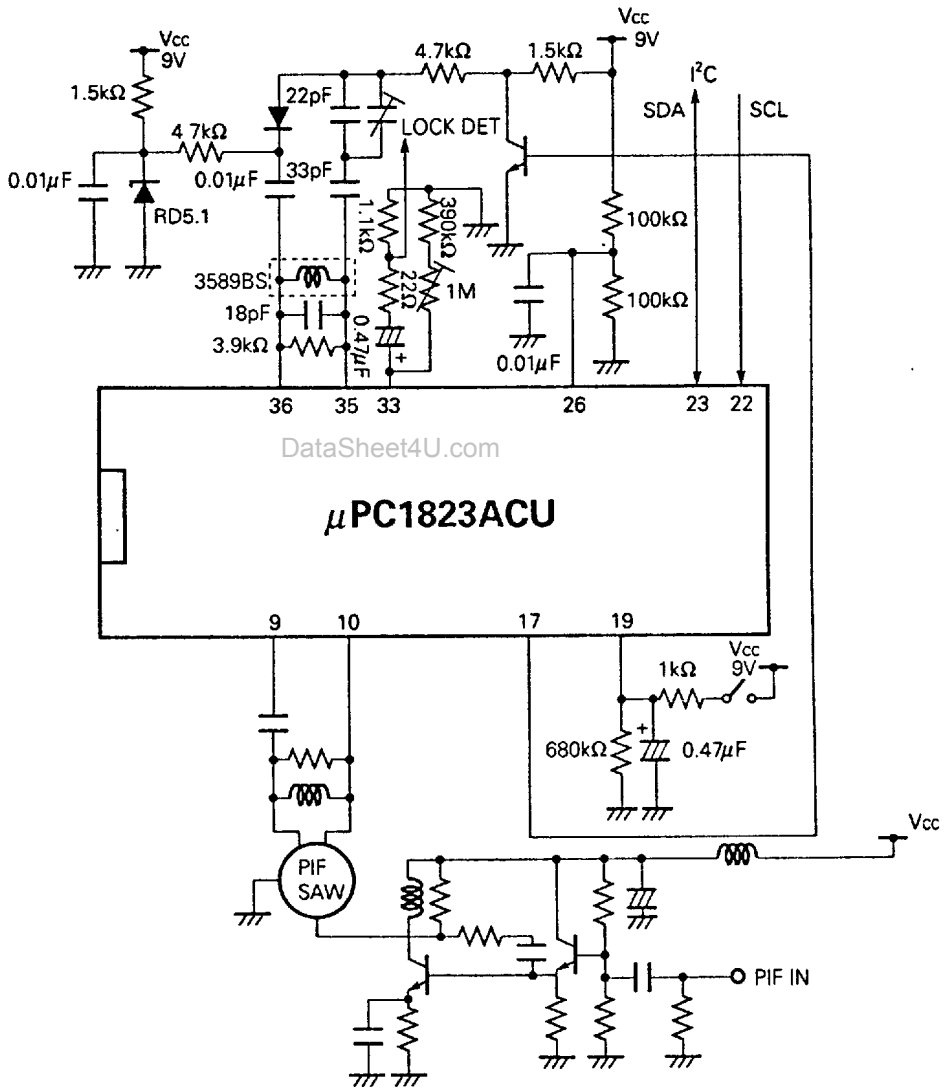
*5. MURATA MFG CO., LTD.
Ceralock
CSB500F32

ADJUSTMENT METHOD OF VCO FREE RUN FREQUENCY

① Control to select B/G mode via I²C BUS. (Set up to S A0→D5="1", D6="1",)
Input condition is no signal. Defeat PIF AGC (Pin 13 connects to GND), and then pin 19 connects to Vcc via resistor of 1kΩ
And so adjust VR of pin 33 to set pin 26 voltage (AFT DC voltage) to 4.5±0.05V.

② Input CW signal (unmodulated carrier, f_0=38.9MHz, v_i=90dBμ) to pin 9 and pin 10,
pin 19 connects to Vcc via resistor of 1kΩ.
And so adjust the core of VCO coil to set pin 26 voltage (AFT DC voltage) to 4.5±0.05V.

③ Control to select L mode via I²C BUS. (Set up to S A0→D5="0", D6="0",)
Input CW signal (unmodulated carrier, f_0=32.7MHz, v_i=90dBμ) to pin 9 and pin 10,
pin 19 connects to Vcc via resistor of 1kΩ.
And so adjust trimmer capacitor to set pin 26 voltage (AFT DC voltage) to 4.5±0.05V.



SERIAL BUS INTERFACE

The μPC1823A supports a serial bus interface function. The serial bus is I²C bus which developed by PHILIPS. This control bus uses two lines of serial clock line SCL and serial data line SDA.

The μPC1823A has I²C bus interface circuit of three registers (8 bits) which enables to write and one register which enable to read the state in IC.

Serial bus interface circuit makes inputting data or clock level to logic level of internal IC. And these bus lines (SDA and SCL) are connected to a positive supply voltage via pull-up resistors.

The outline of the I²C bus spec. is as following.

SCL (Serial Clock Line)

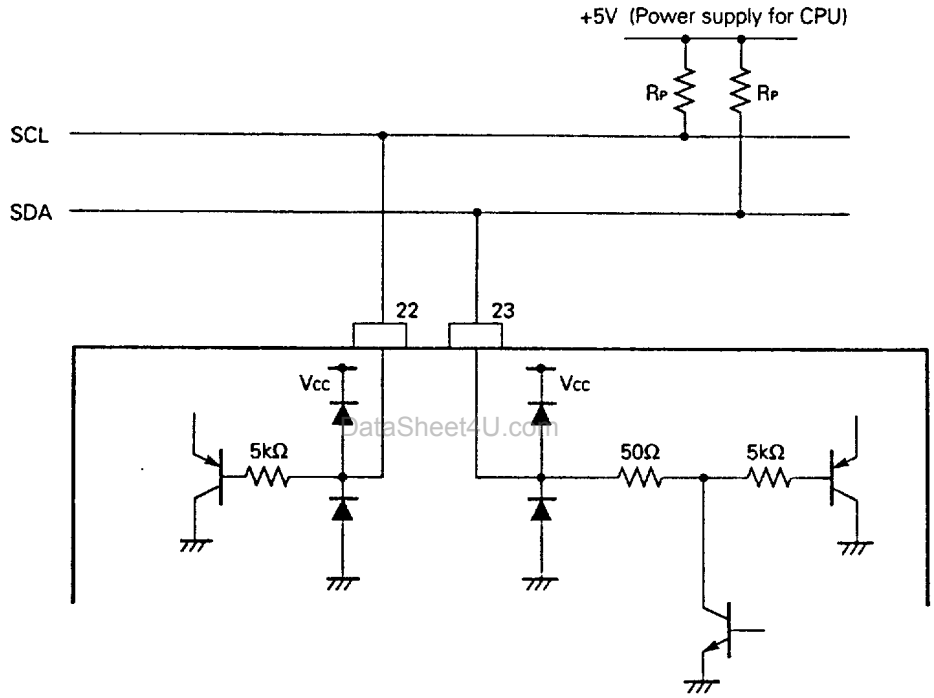
The master CPU outputs serial clock for synchronization. The μPC1823A takes serial data by this serial clock.

The input level is compatible with CMOS. However the circuit of input stage is designed by bipolar PNP device.

SDA (Serial Data Line)

The master CPU outputs serial data. The μPC1823A takes these data by the serial clock.

The input level is compatible with CMOS. However the circuit of input stage is designed by bipolar PNP device.



TRANSMISSION SPECIFICATION

START Condition

The start condition is generated by relation of SDA and SCL.

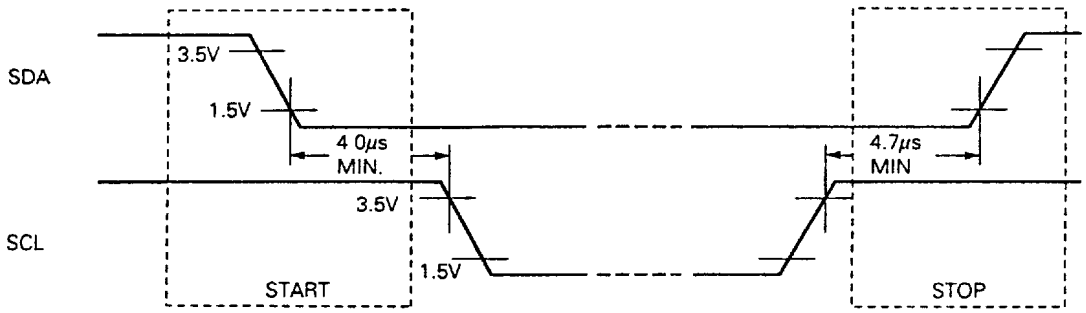
A HIGH to LOW transition of SDA line while SCL line is HIGH is the START condition. When the μPC1823A receives this condition, it takes in the following data.

STOP Condition

The stop condition is generated by relation of SDA and SCL.

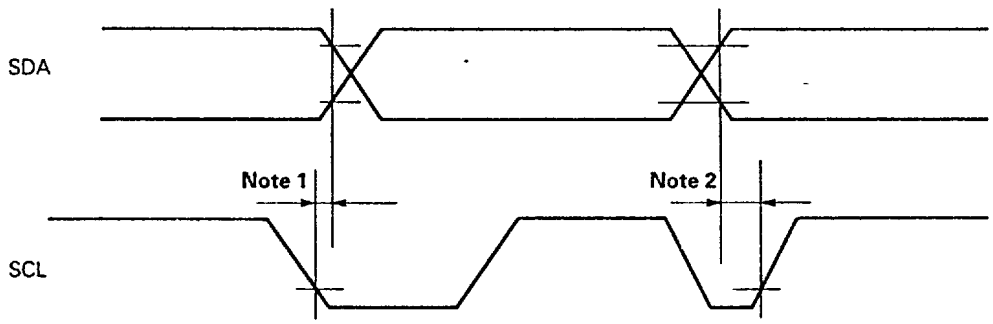
A LOW to HIGH transition of SDA line while SCL line is HIGH is the STOP condition. When the μPC1823A receives this condition, the μPC1823A stops the taking in or sending out the serial data.

The timing diagram is figured in the following diagram.



DATA Transmission

The variation of data must be done while SCL line is LOW. In another expression, SDA line must be stable while the SCL is HIGH. The timing diagram is figured in following diagram.



Note 1. Data hold time for CPU=5μs MIN.
Data hold time for I^2C device=300 ns MIN.

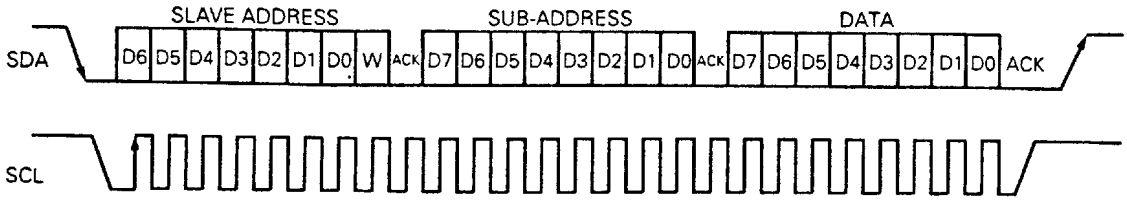
2. Data set-up time 250 ns MIN.

TRANSMISSION FORMAT

Every byte consists of 8-bits. And each byte must be followed by an acknowledge bit. And data are transfered with the MSB first.

The first byte after START condition is Slave chip address (7-bits) and a Read/Write bit. The Slave chip address of μ PC1823A is "C0H".

The LSB bit of first byte is allocated for Read/Write bit. High ("1") input indicates Read mode, and Low ("0") input indicates Write mode. The direction of data is from CPU to μPC1823A on Write mode, and is from μ PC1823A to CPU on Read mode.

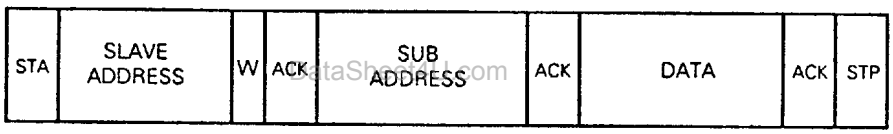


The μPC1823A has the automatic increment function of SUB-ADDRESS, so it's able to transmit data continuously.

The formats of data transmission are described as followings.

1 Byte Data Transfer

The master CPU must send START condition, Slave chip address, Sub-address, data byte, and STOP condition. The μPC1823A sends an acknowledge bit after the success of data receiving following to the every sending byte. (at 9th clock)



STA : START
W : WRITE MODE
ACK : ACKNOWLEDGE
STP : STOP

3 Byte Data Transfer

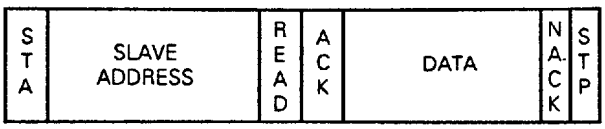
The μPC1823A has 3 Sub-address. By using automatic increment mode, the data transmission can be done easily.

The master CPU must send START condition, Slave chip address, Sub-address ("00H"), 3 data bytes, and STOP condition. The μPC1823A sends an acknowledge bit after the success of data receiving following to the every sending byte (at 9th clock). If the starting Sub-address is "01H" or "02H", the ending Sub-address is "02H". If there are more data than the number of Sub-address, the μPC1823A release the bus line.

Data Read

The μPC1823A has a read register. The master CPU can read this register through serial bus.

The master CPU must send START condition, Slave chip address and a Read bit. The μPC1823A sends an acknowledge bit after the success of address receiving (at 9th clock). After the acknowledge, the μPC1823A begins to send a data of read register. After the data sending, the μPC1823A release the bus line with no acknowledge.



ACKNOWLEDGE

This serial bus has the acknowledge bit which can decide to complete transmission data. Acknowledge bit is added to 9th bit in data.

Master CPU can judge to complete transmission data when acknowledge state is "High" or "Low".

When this acknowledge state is "Low", master CPU decides to complete transmission data. And so when the acknowledge state is "High", the state shows NAK (no acknowledge) state and master CPU decides not to complete transmission or compulsory to release BUS by slave side.

NAK state's condition is when master IC sends different address data to slave IC, or when slave IC ends to transfer data during Read state.

SUB-ADDRESS TABLE

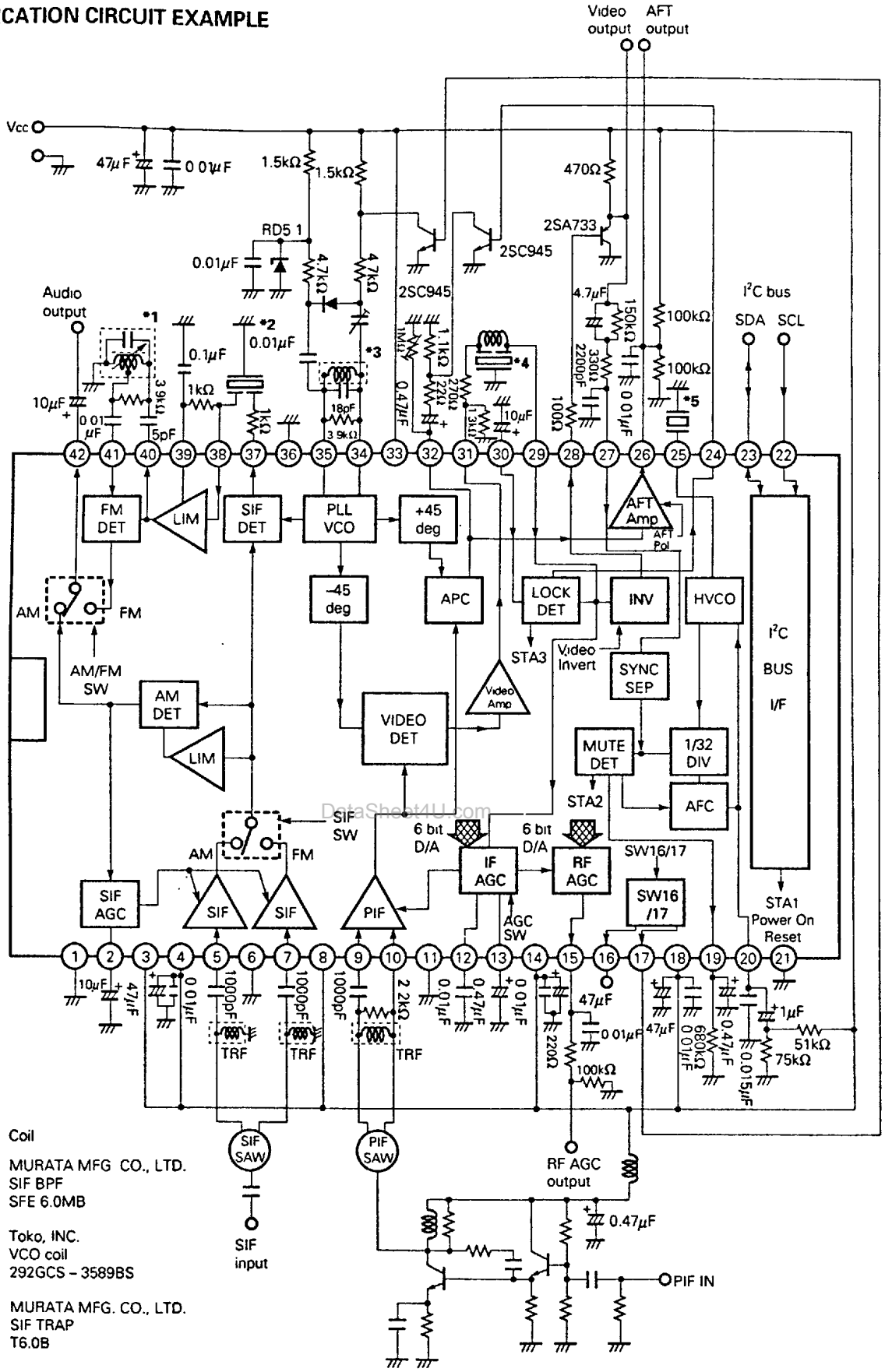
- Slave Address: "C0H"
- Write mode

Sub ADD.	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
00H	AFT	INV	VCO	AGC	Audio	SIF	TRAP	0
	AFT Polarity 0: right up 1: right down	Video Polarity 0: L mode 1: B/G mode	VCO SW 0: Low 1: High	AGC SW 0: Keyed 1: Peak	Audio Output SW 0: AM out 1: FM out	SIF Input SW 0: 5 pin 1: 7 pin	Audio trap fo SW 0: Low 1: High	
01H	DIF	SPD	Vadj					
	AFT SW 0: AFT ON 1: AFT OFF	IF AGC Response SW 0: Continuous 1: search	L Mode Video Output Adjust 0 to 63					
			D5	D4	D3	D2	D1	D0
	–	–	Vref					
02H	0	0	RF AGC Reference Adjust 0 to 63					
			D5	D4	D3	D2	D1	D0

- Read mode

	DATA							
	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
	STA1	STA2	STA3	–	–	–	–	–
	Power On Reset Flag 0: Normal 1: Power on	Mute Det Output 0: H-lock 1: Unlock	Lock Det Output 0: PLL lock 1: Unlock	1	1	1	1	1

APPLICATION CIRCUIT EXAMPLE



*1. Coil

*2. MURATA MFG CO., LTD.
SIF BPF
SFE 6.0MB

*3. Toko, INC.
VCO coil
292GCS – 3589BS

*4. MURATA MFG. CO., LTD.
SIF TRAP
T6.0B

*5. MURATA MFG. CO., LTD.
Ceralock
CSB500F32