

FEATURES

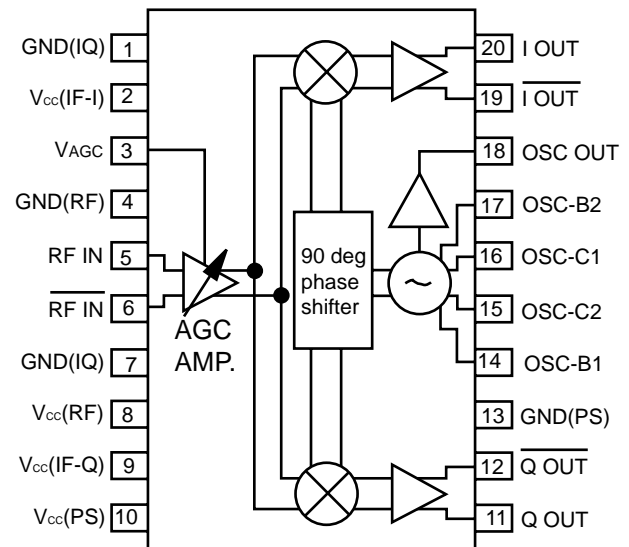
- **RF BANDWIDTH:**
440 - 520 MHz
- **IF BANDWIDTH:**
0.3 - 20 MHz
- **ON CHIP 90° PHASE SHIFTER**
- **IQ PHASE AND AMPLITUDE BALANCE**
Amplitude Balance: ± 0.5 dB
Phase Balance: ± 2.0 degree
- **LOW IM₃ DISTORTION:**
35 dBc Typical
- **SMALL 20 PIN SSOP PACKAGE**
- **TAPE AND REEL PACKAGE AVAILABLE**

DESCRIPTION

The UPC2781GR is a Silicon MMIC IQ demodulator manufactured with the NESAT III™ silicon bipolar process. The IC consists of an AGC amplifier, double balanced mixers, oscillator, 90° phase shifter, and I&Q output buffer amps. The device was specifically designed for DBS receivers and other digital communication systems.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

INTERNAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5 V, Z_L = 1k Ω)

PART NUMBER PACKAGE OUTLINE			UPC2781GR S20 (SSOP 20)		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I _{CC}	Supply Current (no input signal)	mA	52	70	88
f _{RF}	RF Input Bandwidth (f _{IF} = 10 MHz, f _{RF} > f _{LO} , IQ Phase Balance < $\pm 1.5^\circ$)	MHz	440	480	520
f _{IF}	IF Output Bandwidth (f _{RF} = 480 MHz, P _{LO} = -10 dBm, f _{RF} > f _{LO} , V _{AGC} = 0 V)	MHz	0.3		20
CG	Conversion Gain (f _{RF} = 480 MHz, f _{IF} = 10 MHz, V _{AGC} = 0 V)	dB		50	
NF	Noise Figure (f _{RF} = 480 MHz, f _{IF} = 10 MHz, P _{LO} = -10 dBm, V _{AGC} = 0 V)	dB		18	
IM ₃	3rd Order Intermodulation Distortion (f _{RF1} = 480 MHz, f _{RF2} = 481 MHz, f _{LO} = 470 MHz, P _{LO} = -10 dBm)	dBc		35	
$\Delta\Phi$	IQ Phase Balance (f _{RF} = 480 MHz, f _{IF} = 10 MHz, P _{RF} = -30 dBm, P _{LO} = -10 dBm)	deg	-2		+2
ΔG	IQ Amplitude Balance (f _{RF} = 480 MHz, f _{IF} = 10 MHz, P _{RF} = -30 dBm, P _{LO} = -10 dBm, V _{AGC} = 0 V)	dB	-0.5		+0.5
G _{AGC}	AGC Control Range (f _{RF} = 480MHz, P _{RF} = -30dBm, f _{IF} = 10MHz, P _{LO} = -10dBm, 0 ≤ V _{AGC} ≤ 5 V)	dB	15	20	
LO-RF	LO to RF Isolation (f _{LO} = 470 MHz, P _{LO} = -10 dBm, P _{RF} = -30 dBm, V _{AGC} = 0 V)	dB		30	
LO-IF	LO to IF Isolation (f _{LO} = 470 MHz, P _{LO} = -10 dBm, P _{RF} = -30 dBm, V _{AGC} = 0 V)	dB		20	
P _O (SAT)	Maximum Output Power (f _{RF} = 480 MHz, f _{IF} = 10 MHz, P _{RF} = -10 dBm)	dBm		0	
V _O	Output Voltage (f _{RF} = 480 MHz, f _{IF} = 10 MHz, P _{LO} = -10 dBm, Z _L = 1k Ω)	V _{P-P}		1.0	

ABSOLUTE MAXIMUM RATINGS¹ (TA = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
Vcc	Supply Voltage	V	6.0
PD	Power Dissipation ²	mW	500
TOP	Operating Temperature Range	°C	-40 to +75
TSTG	Storage Temperature	°C	-55 to +150

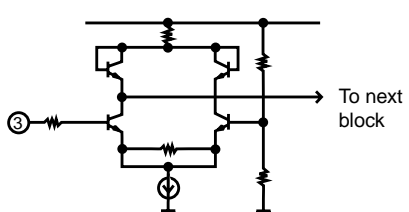
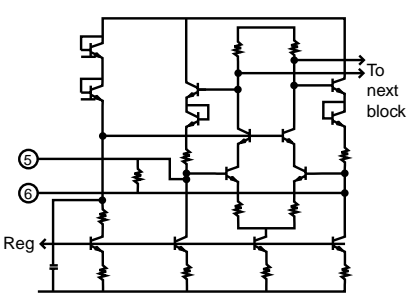
Notes:

1. Operation in excess of any one of these parameters may result in permanent damage.
2. Mounted on a 50x50x1.6 mm epoxy glass PWB (TA = 75°C).

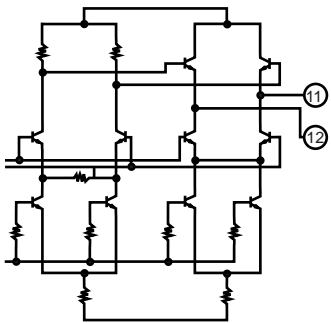
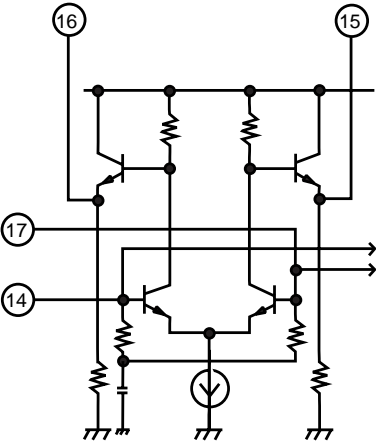
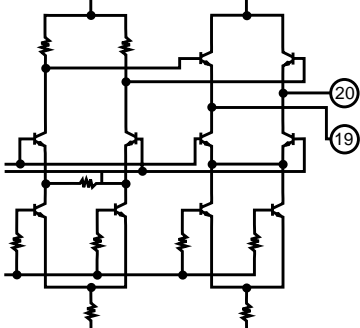
RECOMMENDED OPERATING CONDITIONS

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
Vcc	Supply Voltage	V	4.75	5.0	5.25
TOP	Operating Temperature	°C	-40	+25	+75

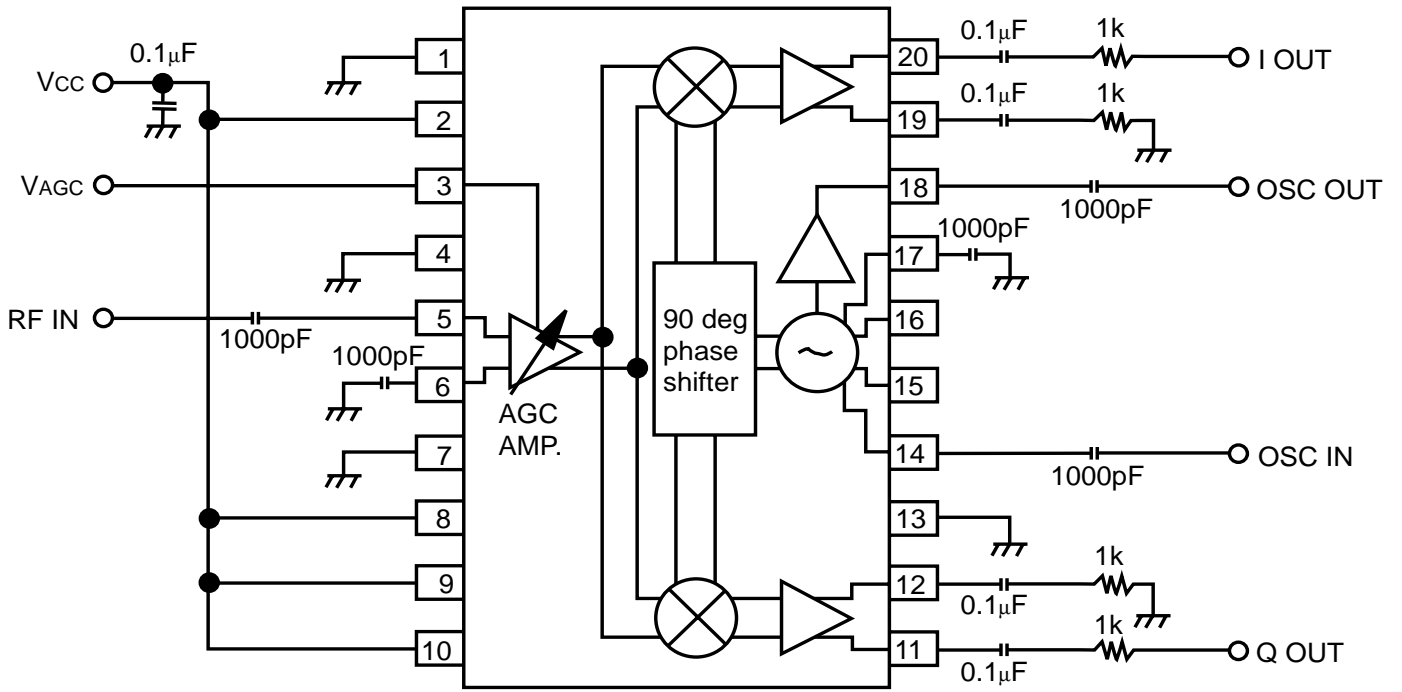
PIN FUNCTIONS

Pin No.	Pin Name	Pin Voltage Typ. (V)	Function and Explanation	Equivalent Circuit
1	GND(IQ)	0.0	Ground pin of IF (IQ) block.	
2	Vcc (IF I)	5.0	Power supply pin of I-output.	
3	VAGC	0.0 ~ 5.0	Gain control pin. <ul style="list-style-type: none"> • VAGC = 0 V : Full gain • VAGC = 5 V : Minimum gain 	
4	GND(RF)	0.0	Ground pin of RF, Mixer and regulator block.	
5	RFIN	2.3	RF input pin. In case of single input, pin 6 should be bypassed with a capacitor.	
6	RFIN	2.3		
7	GND(IQ)	0.0	Ground pin of IF (IQ) block.	
8	Vcc (RF)	5.0	Power supply pin of RF, Mixer and regulator block.	
9	Vcc (IFQ)	5.0	Power supply pin of Q-output.	
10	Vcc (PS)	5.0	Power supply pin of Phase Shifter block.	

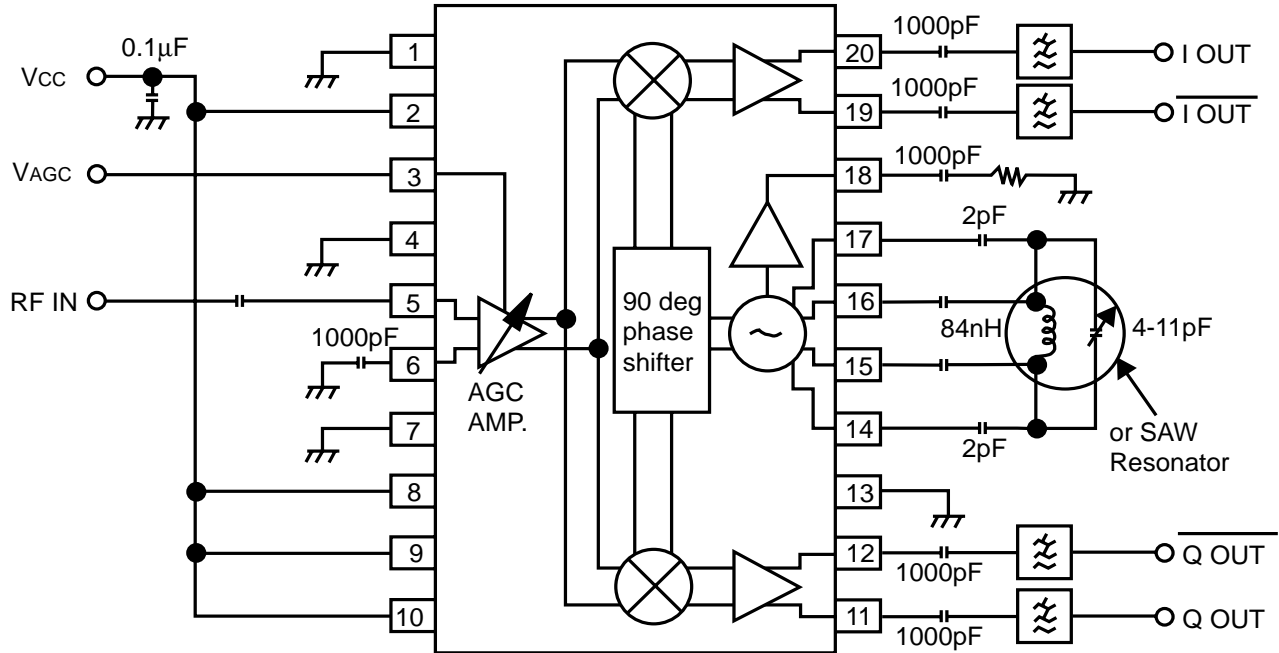
PIN FUNCTIONS

Pin No.	Pin Name	Pin Voltage Typ. (V)	Function and Explanation	Equivalent Circuit
11	Qout	2.4	Q-IF output pin. Pin 11 and pin 12 are balanced outputs.	
12	\overline{Qout}	2.4		
13	GND (IF _Q)	0.0	Ground pin of Phase Shifter block.	
14	OSC-B1	3.0	Oscillator signal input pin. In case of single input, pin 17 should be bypassed with a capacitor.	
15	OSC-C2	4.5		
16	OSC-C1	4.5		
17	OSC-B2	3.0	Oscillator signal input pin. In case of single input, pin 14 should be bypassed with a capacitor.	
18	OSCOUT	3.8	Oscillator output.	
19	\overline{Iout}	2.4	I-IF output pin. Pin 19 and pin 20 are balanced outputs.	
20	Iout	2.4		

TEST CIRCUIT

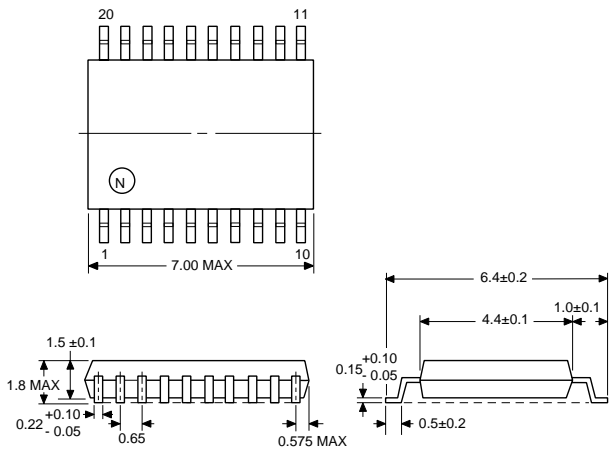


APPLICATION CIRCUIT



OUTLINE DIMENSIONS (Units in mm)

PACKAGE OUTLINE SSOP 20



Lead Material: Alloy 42
Lead Plating: Lead Tin Alloy

ORDERING INFORMATION

PART NUMBER	QUANTITY
UPC2781GR-E1	2500/Reel

Note:
Embossed Tape, 12 mm wide.

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