

# μPC3250T7L

SiGe CMOS/BiCMOS Integrated Circuit  
 IF Down-converter MMIC for Ku-band LNB Converter

R09DS0052EJ0100  
 Rev.1.00  
 Oct 23, 2012

## DESCRIPTION

The μPC3250T7L is a CMOS/BiCMOS MMIC for Ku-band LNB converter.

This device is housed in a 24-pin plastic QFN (Quad Flat Non-Leaded) (T7L) package.

## FEATURES

- Low power consumption : 3.3 V/63 mA, 208 mW
- Switched LO frequency : 9.75 GHz, 10.6 GHz, 10.75 GHz
- 2 step Gain selected function : 41 dB/36 dB
- Low noise figure : 7.5 dB
- Fully integrated Mixer/Oscillator/PLL synthesizer/IF Amplifier/4-channel FET bias supply circuit/  
Polarity control voltage detector/Tone control signal detector
- Integrated power save detector
- 24-pin plastic QFN (T7L) package (4.0 × 4.0 × 0.6 mm)

## APPLICATIONS

- Ku-band Low Noise Block (LNB) converters for satellite receiver (DVB-S, ABS-S application)

## ORDERING INFORMATION

Part Number	Order Number	Package	Marking	Supplying Form
μPC3250T7L-E1	μPC3250T7L-E1-A	24-pin plastic QFN (0.5 mm pitch) (Pb-Free)	C3250	<ul style="list-style-type: none"> <li>• Embossed tape 12 mm wide</li> <li>• Pin 7 to 12 face the perforation side of the tape</li> <li>• Qty 5 kpcs/reel</li> <li>• Dry packing specification (MSL 3 Equivalent)</li> </ul>

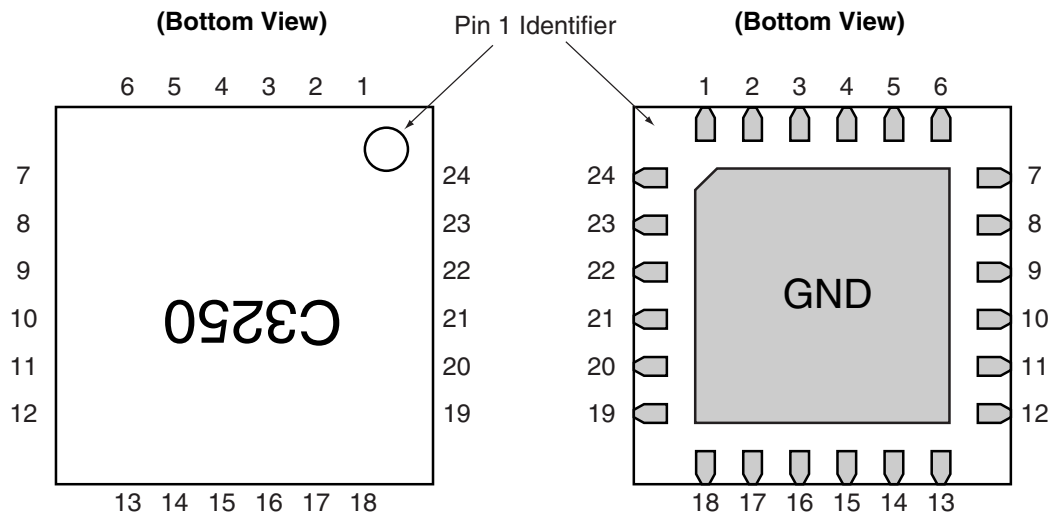
**Remark** To order evaluation samples, please contact your nearby sales office.

Part number for sample order: μPC3250T7L

### CAUTION

Observe precautions when handling because these devices are sensitive to electrostatic discharge.

## PIN CONNECTIONS



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	NC	7	V <sub>DV</sub>	13	G <sub>SW</sub>	19	V <sub>DDPLL</sub>
2	RF <sub>in</sub>	8	V <sub>GV</sub>	14	CVNeg	20	TonePol
3	NC	9	V <sub>D1</sub>	15	XO2	21	IF <sub>out</sub>
4	R <sub>cal</sub>	10	V <sub>G1</sub>	16	XO1	22	V <sub>CCIF</sub>
5	V <sub>DH</sub>	11	V <sub>D2</sub>	17	V <sub>ref</sub>	23	V <sub>CCRF</sub>
6	V <sub>GH</sub>	12	V <sub>G2</sub>	18	CP <sub>out</sub>	24	LO <sub>sel</sub>

**Remark** NC means no connection pin.

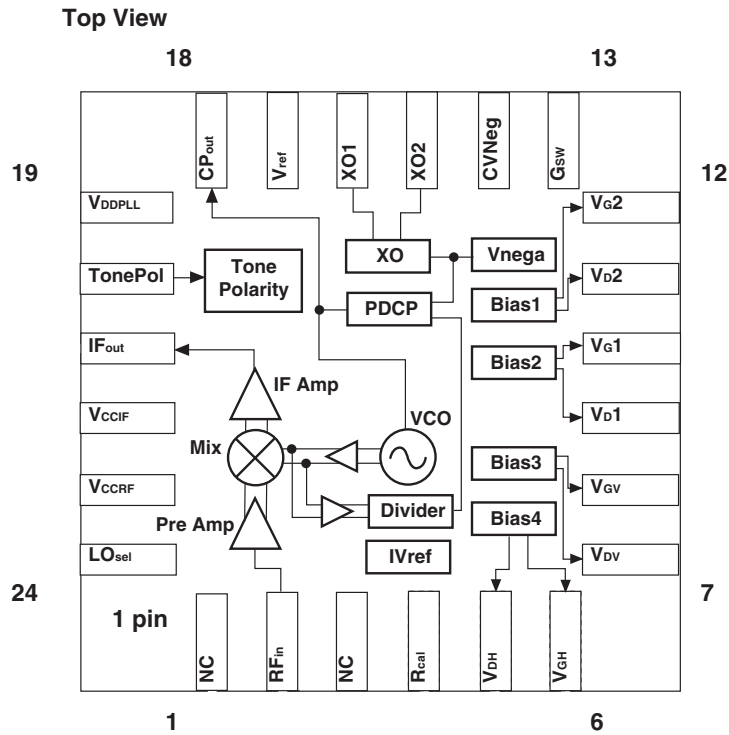
Heat sink of bottom side of this device is connected to GND.

## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply Voltage	V <sub>CCRF</sub> , V <sub>CCIF</sub> , V <sub>DDPLL</sub>	+4.0	V
Control Voltage (TonePol, LO <sub>sel</sub> , G <sub>SW</sub> )	V <sub>POLA</sub> , V <sub>LOsel</sub> , G <sub>SW</sub>	+4.0	V
Power dissipation <sup>Note</sup>	P <sub>tot</sub>	1.53	mW
Storage Temperature	T <sub>stg</sub>	-55 to +125	°C
Operating Ambient Temperature	T <sub>A</sub>	-40 to +85	°C
Input Power	P <sub>in</sub>	0	dBm

Note: Mounted on double-sided copper-clad 50 × 50 × 0.51 mm laminated PWB, T<sub>A</sub> = +85°C

**BLOCK DIAGRAM**



Pin No.	Name	Description
1	NC	No Connection
2	RF <sub>in</sub>	Ku band RF signal input, AC coupling required.
3	NC	No Connection
4	R <sub>cal</sub>	LNFET drain current adjust by resister
5	V <sub>DH</sub>	Horizontal LNFET drain voltage supply
6	V <sub>GH</sub>	Horizontal LNFET gate bias voltage
7	V <sub>DV</sub>	Vertical LNFET drain voltage supply
8	V <sub>GV</sub>	Vertical LNFET gate bias voltage
9	V <sub>D1</sub>	Common LNFET drain voltage supply 1
10	V <sub>G1</sub>	Common LNFET gate bias voltage 1
11	V <sub>D2</sub>	Common LNFET drain voltage supply 2
12	V <sub>G2</sub>	Common LNFET gate bias voltage 2
13	G <sub>sw</sub>	Gain control input terminal
14	CVNeg	Negative voltage line decoupling
15	XO2	Crystal oscillator connection terminal 2
16	XO1	Crystal oscillator connection terminal 1
17	V <sub>ref</sub>	Reference voltage line decoupling
18	CP <sub>out</sub>	Charge pump output, connect capacitor for loop filter
19	V <sub>DDPLL</sub>	PLL Power supply terminal. Decoupling capacitor required
20	TonePol	Tone and Polarity control signal input terminal
21	IF <sub>out</sub>	L band IF signal output, AC coupling required
22	V <sub>CCIF</sub>	IF Power supply terminal. Decoupling capacitor required
23	V <sub>CCRf</sub>	RF Power supply terminal. Decoupling capacitor required
24	LO <sub>sel</sub>	Local Oscillator frequency control input terminal

**Remark** NC means no connection pin.

Heat sink of bottom side of this device is connected to GND.

**RECOMMENDED OPERATING RANGE (T<sub>A</sub> = +25°C, unless otherwise specified)**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V <sub>CCRF</sub> , V <sub>CCIF</sub> , V <sub>DDPLL</sub>	+3.0	+3.3	+3.6	V
High level of Control Voltage (LO <sub>sel</sub> , G <sub>SW</sub> )	V <sub>High</sub>	V <sub>DD</sub> - 0.5	-	V <sub>DD</sub> <sup>Note 1</sup>	V
Low level of Control Voltage (LO <sub>sel</sub> , G <sub>SW</sub> )	V <sub>Low</sub>	0	-	0.5	V
Operating Ambient Temperature	T <sub>A</sub>	-40	+25	+85	°C
RF Input frequency	f <sub>RF</sub>	10.7	-	12.75	GHz
IF Output frequency	f <sub>IF</sub>	950	-	2 150	GHz
LO frequency	f <sub>LO</sub>	-	9.75	-	GHz
		-	10.6	-	
		-	10.75	-	
TONE control signal frequency	f <sub>TONE</sub>	18	22	26	kHz
TONE control signal voltage	V <sub>TONE</sub>	0.4	0.6	0.8	Vp-p
Polarity control voltage <sup>Note 2</sup>	V <sub>POLA</sub>	13	-	18	V
Input Voltage of pin 20 (TonePol)	V <sub>TP</sub>	0	-	V <sub>DD</sub>	V
Adjustment supply current for each FET	I <sub>D</sub>	5	10	18	mA

Notes: 1 V<sub>DD</sub> : Supply Voltage = V<sub>CCRF</sub> = V<sub>CCIF</sub> = V<sub>DDPLL</sub>

2 See the evaluation (application) circuit.

The detail connection of pin 20 (TonePol) is shown in the evaluation circuit.

This pin cannot be directly connected to 13 V/18 V polarity control voltage.

The polarity control voltage must be divided to a low voltage by the external resistors.

**ELECTRICAL CHARACTERISTICS**

**(T<sub>A</sub> = +25°C, V<sub>CCRF</sub> = V<sub>CCIF</sub> = V<sub>DDPLL</sub> = +3.3 V, Z<sub>S</sub> = Z<sub>L</sub> = 50 Ω, f<sub>xtal</sub> = 25 MHz, unless otherwise specified)**

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Total Supply Current 1 <sup>Note</sup> (V <sub>CCRF</sub> , V <sub>CCIF</sub> , V <sub>DDPLL</sub> ) Normal mode (High Gain selected)	I <sub>CC1</sub>	V <sub>POLA</sub> > 7.0 V , Non-RF input, G <sub>SW</sub> = +3.3 V (without FETs bias supply current)	50	63	80	mA
Total Supply Current 2 <sup>Note</sup> (V <sub>CCRF</sub> , V <sub>CCIF</sub> , V <sub>DDPLL</sub> ) Normal mode (Low Gain selected)	I <sub>CC2</sub>	V <sub>POLA</sub> > 7.0 V , Non-RF input, G <sub>SW</sub> = 0 V (without FETs bias supply current)	48.5	61.5	78.5	mA
Total Supply Current 3 <sup>Note</sup> (V <sub>CCRF</sub> , V <sub>CCIF</sub> , V <sub>DDPLL</sub> ) Power Save mode	I <sub>CC3</sub>	V <sub>POLA</sub> = 0 V ( < 3.6V) Non-RF input (without FETs bias supply current)	-	5	10	mA

Note: See the evaluation (application) circuit.

The detail connection of pin 20 (TonePol) is shown in the evaluation circuit.

This pin cannot be directly connected to 13 V/18 V polarity control voltage.

The polarity control voltage must be divided to a low voltage by the external resistors.

## ELECTRICAL CHARACTERISTICS

( $T_A = +25^\circ\text{C}$ ,  $V_{CCRF} = V_{CCIF} = V_{DDPLL} = +3.3\text{ V}$ ,  $G_{SW} = +3.3\text{ V}$ ,  $Z_S = Z_L = 50\ \Omega$ ,  $f_{xtal} = 25\text{ MHz}$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Conversion Gain 1 <sup>Note 1</sup>	$G_{conv1}$	$f_{LO} = 9.75\text{ GHz}$ , $f_{IF} = 1.5\text{ GHz}$ , $P_{in} = -50\text{ dBm}$	37	41	45	dB
Conversion Gain 2 <sup>Note 1</sup>	$G_{conv2}$	$f_{LO} = 10.6\text{ GHz}$ , $f_{IF} = 1.5\text{ GHz}$ , $P_{in} = -50\text{ dBm}$	37	41	45	dB
Conversion Gain 3 <sup>Note 1</sup>	$G_{conv3}$	$f_{LO} = 10.75\text{ GHz}$ , $f_{IF} = 1.5\text{ GHz}$ , $P_{in} = -50\text{ dBm}$	37	41	45	dB
POLA control Threshold Voltage 1 <sup>Note 1</sup>	$V_{th\_POLA1}$	Power Save mode to Normal mode Dividing resistor : 8.2 kΩ/51 kΩ	3.6	–	7.0	V
POLA control Threshold Voltage 2 <sup>Note 1</sup> (Channel selection )	$V_{th\_POLA2}$	Vertical mode to Horizontal mode Dividing resistor : 8.2 kΩ/51 kΩ	15.2	15.7	16.2	V
TONE control signal Threshold Voltage <sup>Note 1</sup> (Channel selection)	$V_{th\_TONE}$	Low band to High band $f_{TONE} = 22\text{ kHz}$ , Duty Cycle = 50%, Pulse wave Divider capacitor : 0.1 μF/0.1 μF	0.1	0.15	0.35	V <sub>p-p</sub>
Drain Voltage H <sup>Note 1, 2</sup>	$V_{DH}$	$V_{POLA} = 18\text{ V}$ , $I_D = 10\text{ mA}$ , $R_{cal} = 22\text{ k}\Omega$	1.8	2.0	2.2	V
Drain Voltage V <sup>Note 1, 2</sup>	$V_{DV}$	$V_{POLA} = 13\text{ V}$ , $I_D = 10\text{ mA}$ , $R_{cal} = 22\text{ k}\Omega$	1.8	2.0	2.2	V
Drain Voltage 1 <sup>Note 1, 2</sup>	$V_{D1}$	$I_D = 10\text{ mA}$ , $R_{cal} = 22\text{ k}\Omega$	1.8	2.0	2.2	V
Drain Voltage 2 <sup>Note 1, 2</sup>	$V_{D2}$	$I_D = 10\text{ mA}$ , $R_{cal} = 22\text{ k}\Omega$	1.8	2.0	2.2	V
Drain Current H <sup>Note 1, 2</sup>	$I_{DH}$	$V_{POLA} = 18\text{ V}$ , $R_{cal} = 22\text{ k}\Omega$	8.5	10	11.5	mA
Drain Current V <sup>Note 1, 2</sup>	$I_{DV}$	$V_{POLA} = 13\text{ V}$ , $R_{cal} = 22\text{ k}\Omega$	8.5	10	11.5	mA
Drain Current 1 <sup>Note 1, 2</sup>	$I_{D1}$	$R_{cal} = 22\text{ k}\Omega$	8.5	10	11.5	mA
Drain Current 2 <sup>Note 1, 2</sup>	$I_{D2}$	$R_{cal} = 22\text{ k}\Omega$	8.5	10	11.5	mA
Gate Voltage H <sup>Note 1, 2</sup> of FET OFF mode	$V_{GH}$	$V_{POLA} = 13\text{ V}$	-2.0	-2.5	-3.0	V
Gate Voltage V <sup>Note 1, 2</sup> of FET OFF mode	$V_{GV}$	$V_{POLA} = 18\text{ V}$	-2.0	-2.5	-3.0	V

Notes: 1 See the evaluation (application) circuit.

The detail connection of pin 20 (TonePol) is shown in the evaluation circuit.

This pin cannot be directly connected to 13 V/18 V polarity control voltage.

The polarity control voltage must be divided to a low voltage by the external resistors.

- 2 See the graph of “ $R_{cal}$  vs.  $I_{DFET}$ ,  $V_{DFET}$ .” FET’s drain current can be adjusted by the external resistors ( $R_{cal}$ ).

**STANDARD CHARACTERISTICS FOR REFERENCE**

(T<sub>A</sub> = +25°C, V<sub>CCRF</sub> = V<sub>CCIF</sub> = V<sub>DDPLL</sub> = +3.3 V, G<sub>SW</sub> = +3.3V, Z<sub>S</sub> = Z<sub>L</sub> = 50 Ω, f<sub>xtal</sub> = 25 MHz, unless otherwise specified)

Parameter	Symbol	Test Conditions	Reference Value	Unit
Conversion Gain Flatness 1	ΔG <sub>conv1</sub>	f <sub>LO</sub> = 9.75 GHz, f <sub>IF</sub> = 0.95 G to 1.95 GHz, P <sub>in</sub> = -50 dBm	2.5	dB
Conversion Gain Flatness 2	ΔG <sub>conv2</sub>	f <sub>LO</sub> = 10.6 GHz, f <sub>IF</sub> = 1.1 G to 2.15 GHz, P <sub>in</sub> = -50 dBm	2.0	dB
Conversion Gain Flatness 3	ΔG <sub>conv3</sub>	f <sub>LO</sub> = 10.75 GHz, f <sub>IF</sub> = 0.95 G to 2.0 GHz, P <sub>in</sub> = -50 dBm	2.0	dB
Noise Figure 1	NF1	f <sub>LO</sub> = 9.75 GHz, f <sub>IF</sub> = 1.5 GHz	7.5	dB
Noise Figure 2	NF2	f <sub>LO</sub> = 10.6 GHz, f <sub>IF</sub> = 1.5 GHz	7.5	dB
Noise Figure 3	NF3	f <sub>LO</sub> = 10.75 GHz, f <sub>IF</sub> = 1.5 GHz	7.5	dB
Gain 1 dB Compression Output Power 1	P <sub>O(1 dB)1</sub>	f <sub>LO</sub> = 9.75 GHz, f <sub>IF</sub> = 1.5 GHz	5	dBm
Gain 1 dB Compression Output Power 2	P <sub>O(1 dB)2</sub>	f <sub>LO</sub> = 10.6 GHz, f <sub>IF</sub> = 1.5 GHz	5	dBm
Gain 1 dB Compression Output Power 3	P <sub>O(1 dB)3</sub>	f <sub>LO</sub> = 10.75 GHz, f <sub>IF</sub> = 1.5 GHz	5	dBm
Output 3rd Order Intercept Point 1	OIP <sub>31</sub>	f <sub>LO</sub> = 9.75 GHz, f <sub>IF1</sub> = 1 500 MHz, f <sub>IF2</sub> = 1 501 MHz	16	dBm
Output 3rd Order Intercept Point 2	OIP <sub>32</sub>	f <sub>LO</sub> = 10.6 GHz, f <sub>IF1</sub> = 1 500 MHz, f <sub>IF2</sub> = 1 501 MHz	16	dBm
Output 3rd Order Intercept Point 3	OIP <sub>33</sub>	f <sub>LO</sub> = 10.75 GHz, f <sub>IF1</sub> = 1 500 MHz, f <sub>IF2</sub> = 1 501 MHz	16	dBm
RF Input Return Loss	RL <sub>RF</sub>	f <sub>RF</sub> = 10.7 G to 12.75 GHz	10	dB
IF Output Return Loss	RL <sub>IF</sub>	f <sub>RF</sub> = 950 M to 2 150 MHz	10	dB
Phase Noise 1	PN1	1 kHz offset	-78	dBc/Hz
Phase Noise 2	PN2	10 kHz offset	-80	dBc/Hz
Phase Noise 3	PN3	100 kHz offset	-88	dBc/Hz
Phase Noise 4	PN4	1 MHz offset	-108	dBc/Hz
Integrated phase noise density	Φnλ (itg)	Integrated offset frequency 10 k to 15 MHz	1.7	°RMS
Local signal Leakage 1	L <sub>o_Leakage1</sub>	f <sub>LO</sub> = 9.75 GHz, Local to RF <sub>in</sub>	-58	dBm
Local signal Leakage 2	L <sub>o_Leakage2</sub>	f <sub>LO</sub> = 10.6 GHz, Local to RF <sub>in</sub>	-58	dBm
Local signal Leakage 3	L <sub>o_Leakage3</sub>	f <sub>LO</sub> = 10.75GHz, Local to RF <sub>in</sub>	-57	dBm
Total Circuit current 1 (Reference status 1)	I <sub>CC1</sub>	2ch FET bias supplied V <sub>POLA</sub> > 7.0 V, Non-RF	83	mA
Total Circuit current 2 (Reference status 2)	I <sub>CC2</sub>	3ch FET bias supplied V <sub>POLA</sub> > 7.0 V, Non-RF	93	mA

Note: See the evaluation (application) circuit.

**STANDARD CHARACTERISTICS FOR REFERENCE**

( $T_A = +25^\circ\text{C}$ ,  $V_{CCRF} = V_{CCIF} = V_{DDPLL} = +3.3\text{ V}$ ,  $G_{SW} = 0\text{ V}$ ,  $Z_S = Z_L = 50\ \Omega$ ,  $f_{xtal} = 25\text{ MHz}$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	Reference Value	Unit
Conversion Gain 1	$G_{conv1}$	$f_{LO} = 9.75\text{ GHz}$ , $f_{IF} = 1.5\text{ GHz}$ , $P_{in} = -50\text{ dBm}$	36	dB
Conversion Gain 2	$G_{conv2}$	$f_{LO} = 10.6\text{ GHz}$ , $f_{IF} = 1.5\text{ GHz}$ , $P_{in} = -50\text{ dBm}$	36	dB
Conversion Gain 3	$G_{conv3}$	$f_{LO} = 10.75\text{ GHz}$ , $f_{IF} = 1.5\text{ GHz}$ , $P_{in} = -50\text{ dBm}$	36	dB
Conversion Gain Flatness 1	$\Delta G_{conv1}$	$f_{LO} = 9.75\text{ GHz}$ , $f_{IF} = 0.95\text{ G to }1.95\text{ GHz}$ , $P_{in} = -50\text{ dBm}$	2.5	dB
Conversion Gain Flatness 2	$\Delta G_{conv2}$	$f_{LO} = 10.6\text{ GHz}$ , $f_{IF} = 1.1\text{ G to }2.15\text{ GHz}$ , $P_{in} = -50\text{ dBm}$	2.0	dB
Conversion Gain Flatness 3	$\Delta G_{conv3}$	$f_{LO} = 10.75\text{ GHz}$ , $f_{IF} = 0.95\text{ G to }2.0\text{ GHz}$ , $P_{in} = -50\text{ dBm}$	2.0	dB
Noise Figure 1	NF1	$f_{LO} = 9.75\text{ GHz}$ , $f_{IF} = 1.5\text{ GHz}$	7.5	dB
Noise Figure 2	NF2	$f_{LO} = 10.6\text{ GHz}$ , $f_{IF} = 1.5\text{ GHz}$	7.5	dB
Noise Figure 3	NF3	$f_{LO} = 10.75\text{ GHz}$ , $f_{IF} = 1.5\text{ GHz}$	7.5	dB
Gain 1 dB Compression Output Power 1	$P_{O(1\text{ dB})1}$	$f_{LO} = 9.75\text{ GHz}$ , $f_{IF} = 1.5\text{ GHz}$	2	dBm
Gain 1 dB Compression Output Power 2	$P_{O(1\text{ dB})2}$	$f_{LO} = 10.6\text{ GHz}$ , $f_{IF} = 1.5\text{ GHz}$	2	dBm
Gain 1 dB Compression Output Power 3	$P_{O(1\text{ dB})3}$	$f_{LO} = 10.75\text{ GHz}$ , $f_{IF} = 1.5\text{ GHz}$	2	dBm
Output 3rd Order Intercept Point 1	$OIP_{31}$	$f_{LO} = 9.75\text{ GHz}$ , $f_{IF1} = 1\ 500\text{ MHz}$ , $f_{IF2} = 1\ 501\text{ MHz}$	12	dBm
Output 3rd Order Intercept Point 2	$OIP_{32}$	$f_{LO} = 10.6\text{ GHz}$ , $f_{IF1} = 1\ 500\text{ MHz}$ , $f_{IF2} = 1\ 501\text{ MHz}$	12	dBm
Output 3rd Order Intercept Point 3	$OIP_{33}$	$f_{LO} = 10.75\text{ GHz}$ , $f_{IF1} = 1\ 500\text{ MHz}$ , $f_{IF2} = 1\ 501\text{ MHz}$	12	dBm
RF Input Return Loss	$RL_{RF}$	$f_{RF} = 10.7\text{ G to }12.75\text{ GHz}$	10	dB
IF Output Return Loss	$RL_{IF}$	$f_{RF} = 950\text{ M to }2\ 150\text{ MHz}$	10	dB

Note: See the evaluation (application) circuit.

## TRUTH TABLE

### Local Oscillator frequency select pin function description (pin 24 (LO<sub>sel</sub>))

LO <sub>sel</sub>	LO <sub>sel</sub> = Low (DVB-S mode)		LO <sub>sel</sub> = High (ABS-S mode)
	Tone signal = 0 kHz	Tone signal = 22 kHz	–
Local Oscillator frequency	9.75 GHz	10.6 GHz	10.75 GHz

Note: The relationships between the LO<sub>sel</sub> state and the pin connection are as follows.

By connecting this pin to GND line (0 V DC), LO<sub>sel</sub> becomes “Low” state.

By connecting this pin to V<sub>DD</sub> line (V<sub>DD</sub> DC), LO<sub>sel</sub> becomes “High” state.

The V<sub>DD</sub> described above means the power supply voltage. Its value is 3.3 V the same as V<sub>CCRF</sub>, V<sub>CCIF</sub>, and V<sub>DDPLL</sub>.

### FET's DC bias control pin function description (pin 20 (TonePol), polarity control voltage)

FETs		Horizontal FET		Vertical FET		Common FET 1		Common FET 2	
V <sub>POLA</sub>		V <sub>GH</sub>	V <sub>DH</sub>	V <sub>GV</sub>	V <sub>DV</sub>	V <sub>G1</sub>	V <sub>D1</sub>	V <sub>G2</sub>	V <sub>D2</sub>
Normal mode	V <sub>POLA</sub> > 16.2 V Note	Controlled (-2.5 V to +1 V)	Controlled (≈ 2 V)	Disable (-2.5V)	Disable (0 V)	Controlled (-2.5 V to +1 V)	Controlled (≈ 2 V)	Controlled (-2.5 V to +1 V)	Controlled (≈ 2 V)
	V <sub>POLA</sub> < 15.2 V Note	Disable (-2.5 V)	Disable (0 V)	Controlled (-2.5 V to +1 V)	Controlled (≈ 2 V)	Controlled (-2.5 V to +1 V)	Controlled (≈ 2 V)	Controlled (-2.5 V to +1 V)	Controlled (≈ 2 V)
Power Save mode	V <sub>POLA</sub> < 3.6 V Note	Disable (-2.5 V)	Disable (0 V)	Controlled (-2.5 V to +1 V)	Controlled (≈ 2 V)	Controlled (-2.5 V to +1 V)	Controlled (≈ 2 V)	Controlled (-2.5 V to +1 V)	Controlled (≈ 2 V)

Note: Dividing Resistor: 8.2 kΩ/51 kΩ

See the evaluation (application) circuit.

The detail connection of pin 20 (TonePol) is shown in the evaluation circuit.

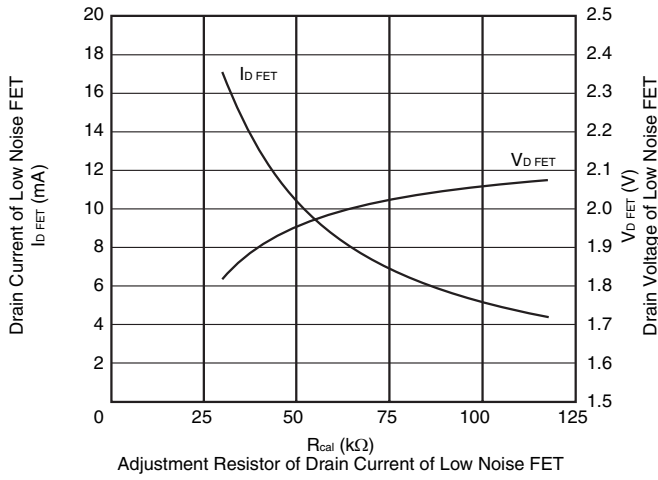
This pin cannot be directly connected to 13 V/18 V polarity control voltage.

The polarity control voltage must be divided to a low voltage.

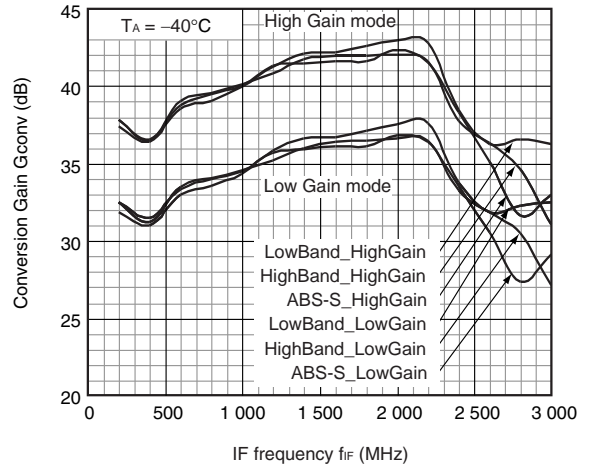


**TYPICAL CHARACTERISTICS**  
(T<sub>A</sub> = +25°C, unless otherwise specified)

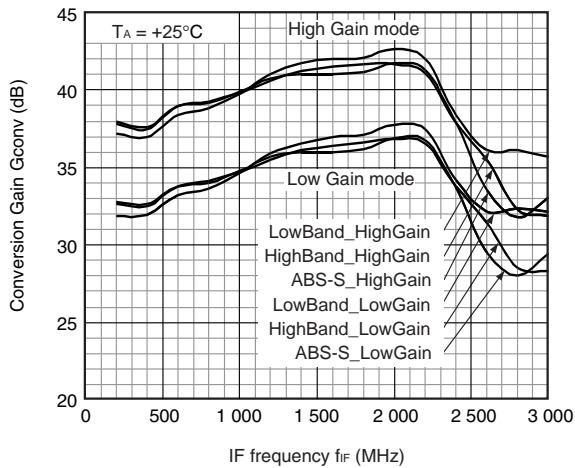
R<sub>cal</sub> vs. I<sub>D FET</sub>, V<sub>D FET</sub>



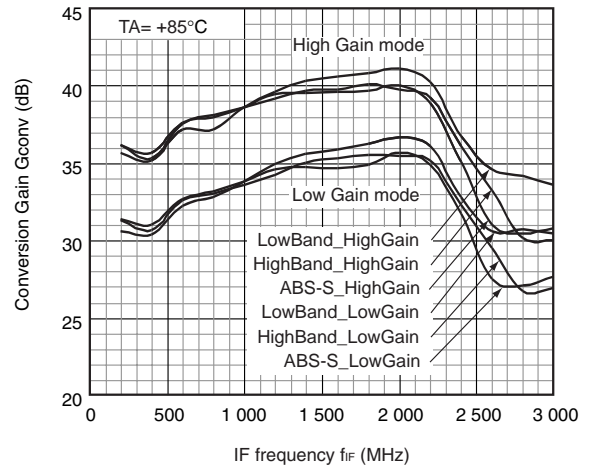
IF frequency vs. Conversion Gain



IF frequency vs. Conversion Gain

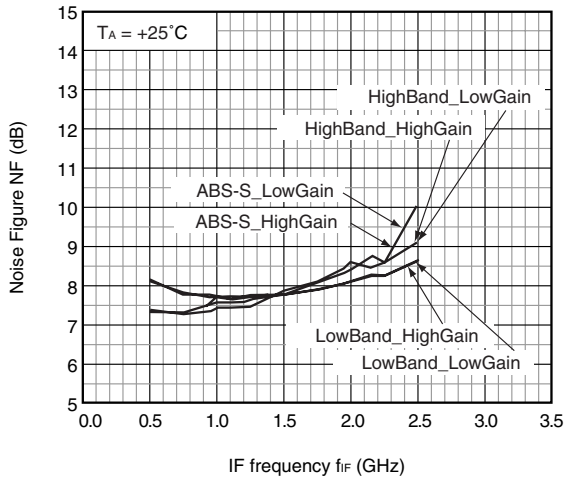


IF frequency vs. Conversion Gain

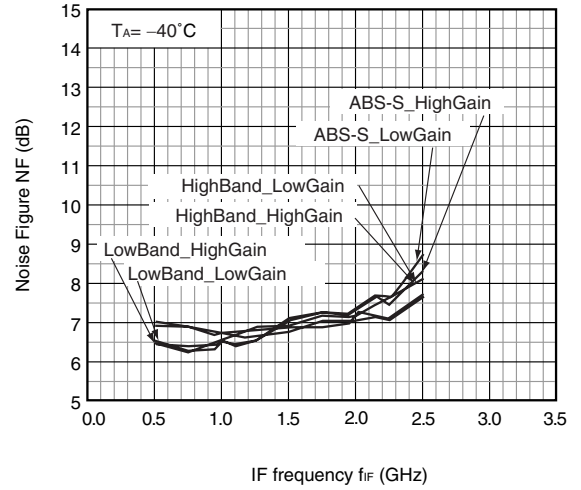


**Remark** The graphs indicate nominal characteristics.

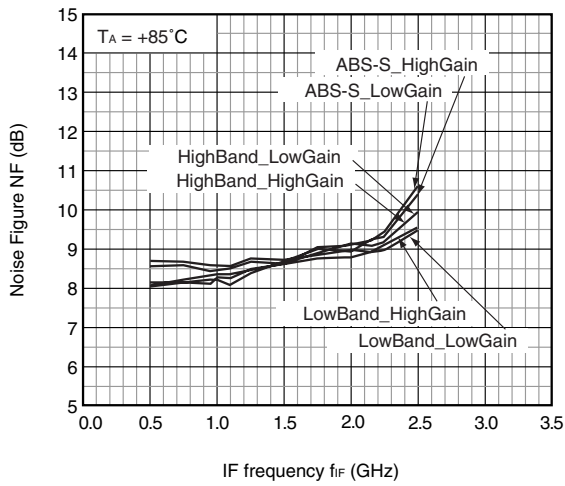
FREQUENCY VS. NOISE FIGURE



FREQUENCY VS. NOISE FIGURE



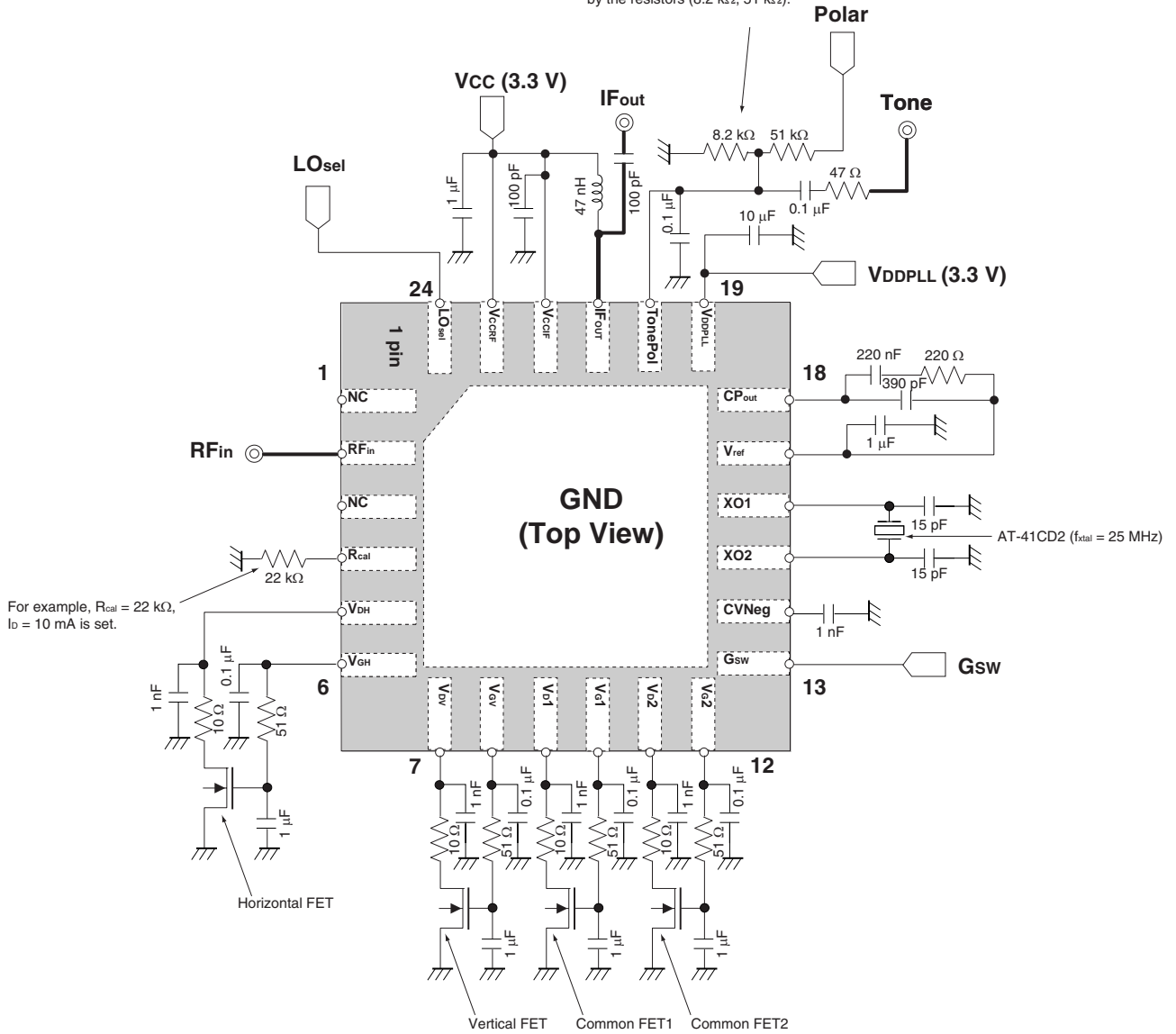
FREQUENCY VS. NOISE FIGURE



**Remark** The graphs indicate nominal characteristics.

EVALUATION CIRCUIT

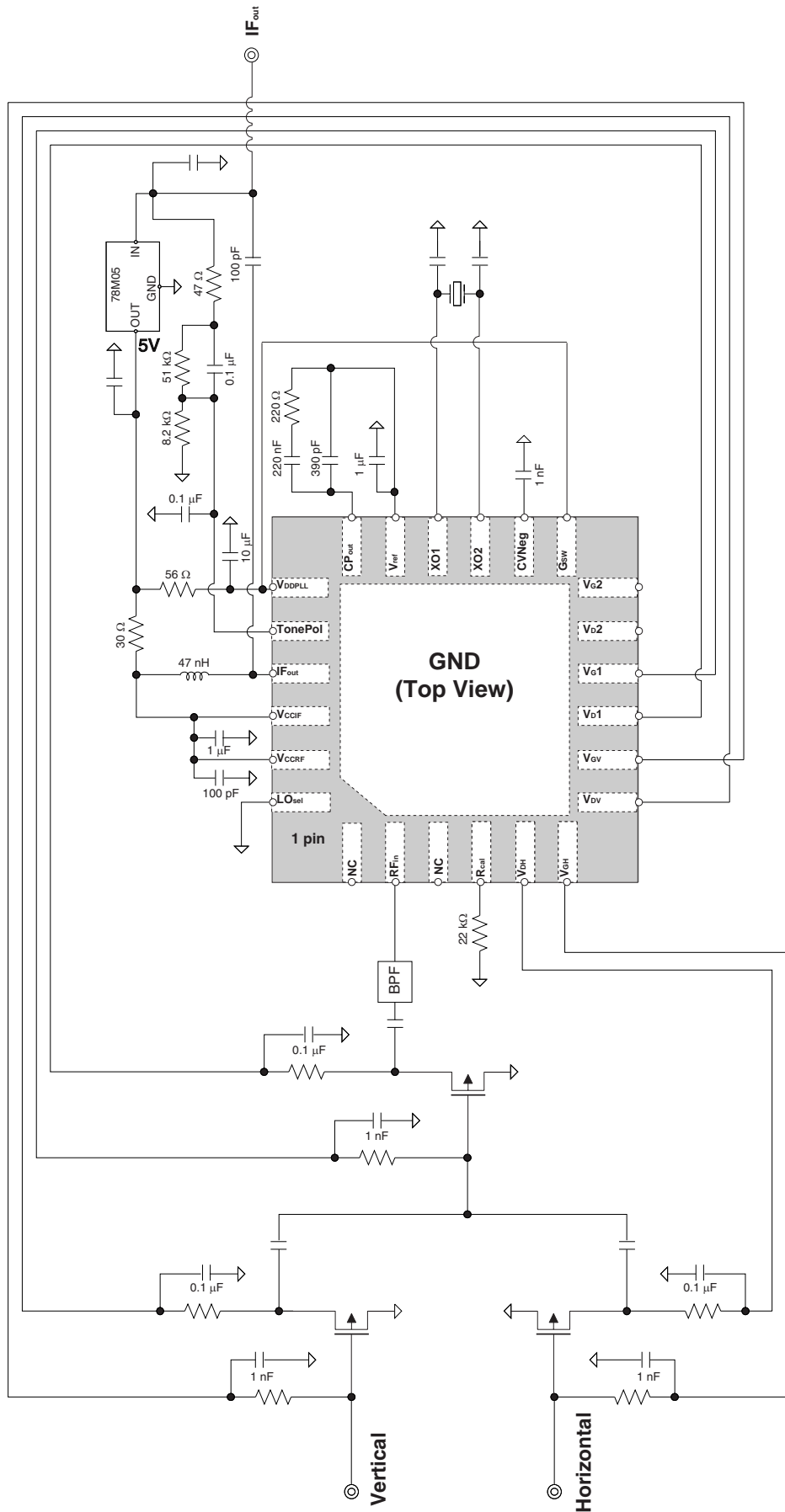
For example, Polarity control voltage is  $V_{POLA} = +13\text{ V}$  and  $+18\text{ V}$ ,  $V_{TP}$  is divided to a low voltage,  $+1.8\text{ V}$  and  $+2.5\text{ V}$ , respectively, by the resistors ( $8.2\text{ k}\Omega$ ,  $51\text{ k}\Omega$ ).



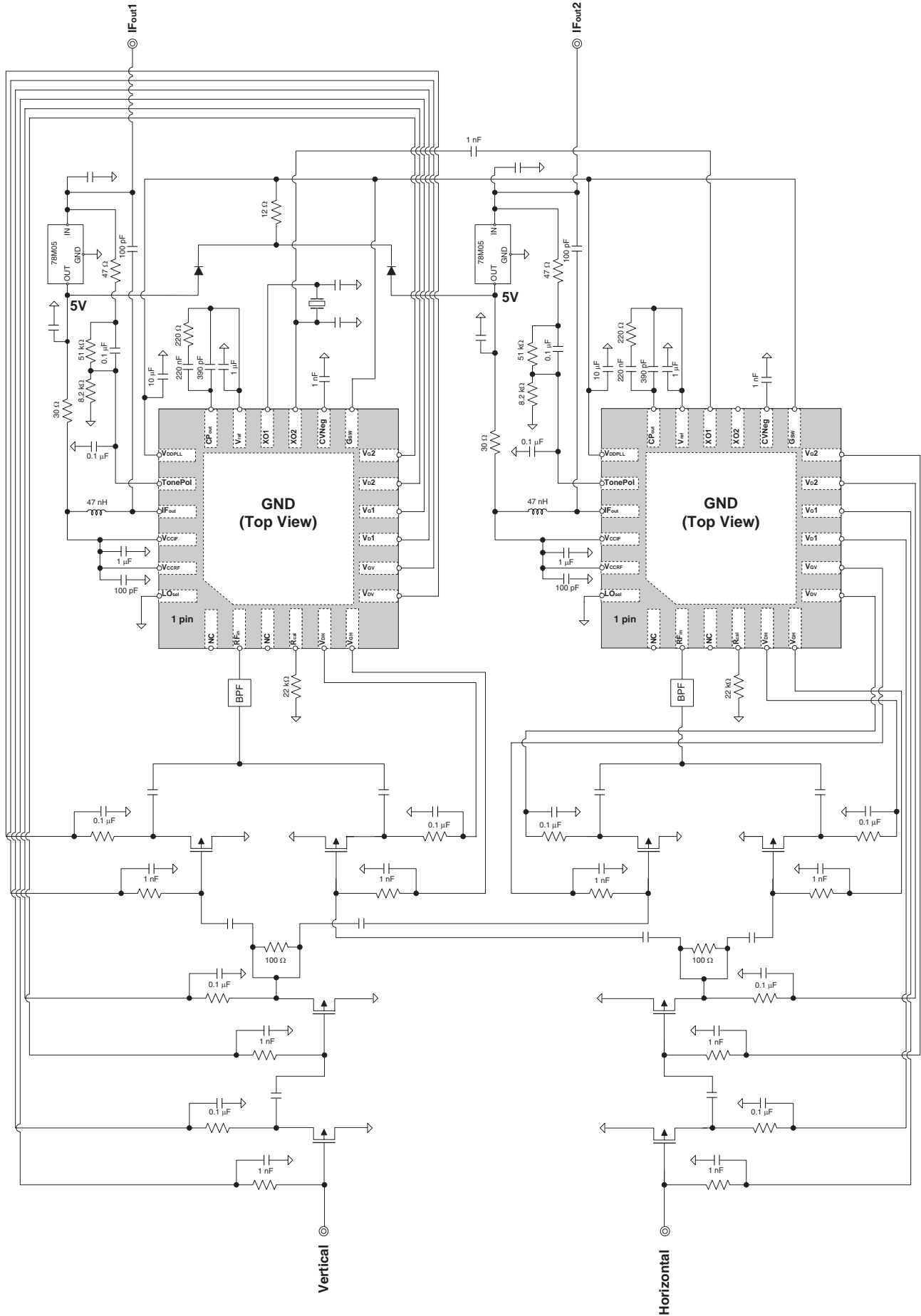
**Remark** NC means Non-Connection.  
Heat sink (bottom side of the device) is connected to GND.  
Board material is RO4003C (Rogers,  $t = 0.508\text{ mm}$ ).

# APPLICATION CIRCUIT

FOR SINGLE LNB (REFERENCE ONLY)

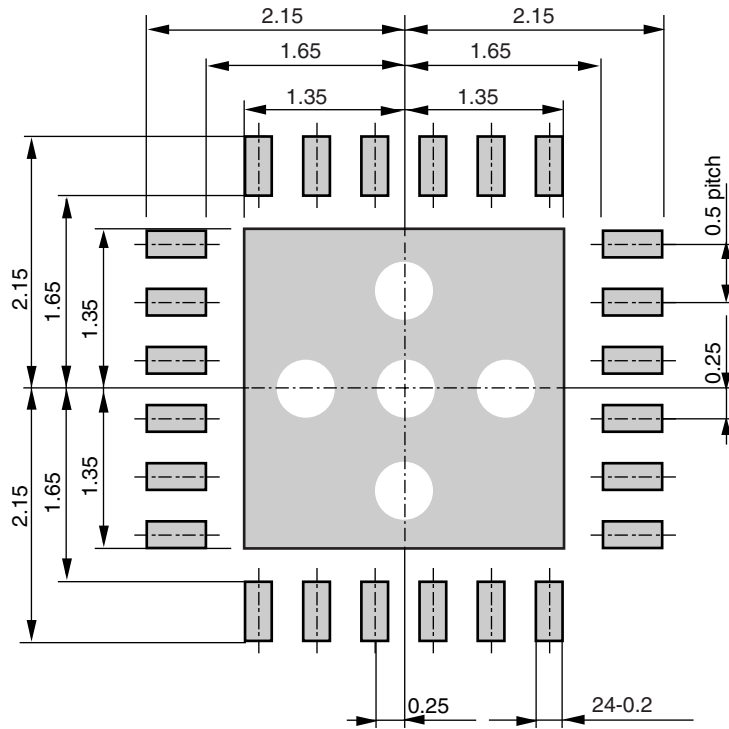


FOR TWIN LNB (DOUBLE SINGLE LNB) (REFERENCE ONLY)



### MOUNTING PAD LAYOUT DIMENSIONS

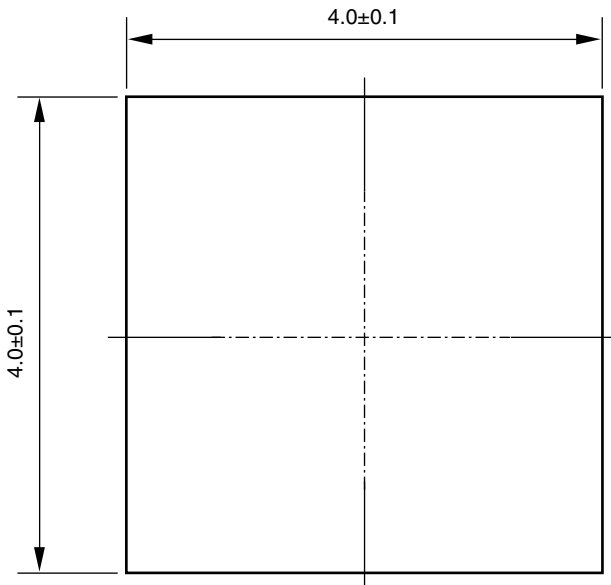
24-PIN PLASTIC QFN (T7L) PACKAGE (4.0 × 4.0 × 0.6 mm) (UNIT : mm)



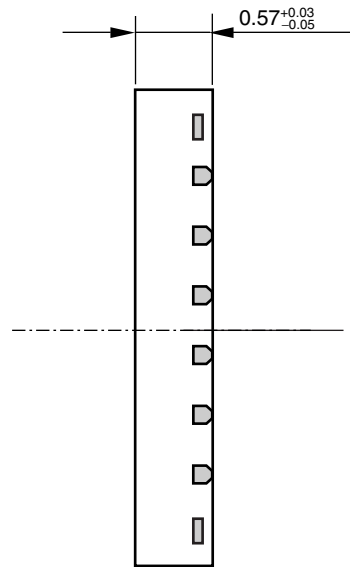
# PACKAGE DIMENSIONS

24-PIN PLASTIC QFN (T7L) PACKAGE (4.0 × 4.0 × 0.6 mm) (UNIT : mm)

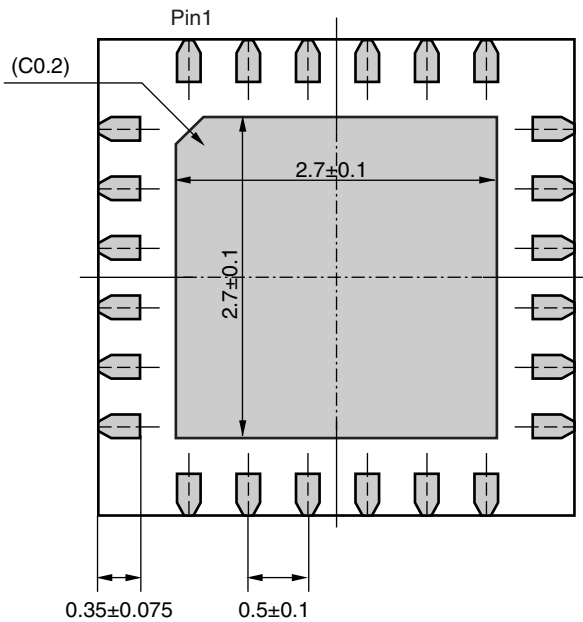
(Top View)



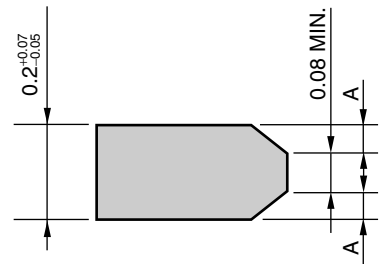
(Side View)



(Bottom View)



(Dimensions of Each Pin Part)



Remark A > 0

## RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions	Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature) : 260°C or below Time at peak temperature : 10 seconds or less Time at temperature of 220°C or higher : 60 seconds or less Preheating time at 120 to 180°C : 120±30 seconds Maximum number of reflow processes : 3 times Maximum chlorine content of rosin flux (% mass) : 0.2% (Wt.) or below	IR260
Partial Heating	Peak temperature (package surface temperature) : 350°C or below Soldering time (per side of device) : 3 seconds or less Maximum chlorine content of rosin flux (% mass) : 0.2% (Wt.) or below	HS350

### CAUTION

Do not use different soldering methods together (except for partial heating).



<b>Revision History</b>	<b>μPC3250T7L Data Sheet</b>
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Rev.	Date	Description	
		Page	Summary
1.00	Oct 23, 2012	–	First edition issued

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