μPC4072MF-DAA

J-FET Input Low-Noise Dual Operational amplifier
e_n = 17 nV/√Hz, SR = 13 V/μs, GBW = 3 MHz, V_{IO} = ±2 mV

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Rev.1.00
Jul 25, 2012

Description

The μPC4072MF-DAA is a J-FET input operational amplifier. This product is designed as low noise version of the μPC4082.

The features of the μPC4072MF-DAA are more improved input equivalent noise voltage, input offset voltage and input bias current than those of μPC4082. By these features, the μPC4072MF-DAA is excellent choice for wide variety of applications including audio preamplifier and active filter.

Features

- Input Offset Voltage: ±2 mV (TYP.)
- Input Bias Current :30 pA (TYP.)
- High Slew Rate: 13 V/μs (TYP.)
- Unity Gain Frequency: 3 MHz (TYP.)
- Low noise: 17 nV/√Hz (TYP.) @ f = 1 kHz
- Internal frequency compensation
- Output short circuit protection
- High input impedance: J-FET Input stage

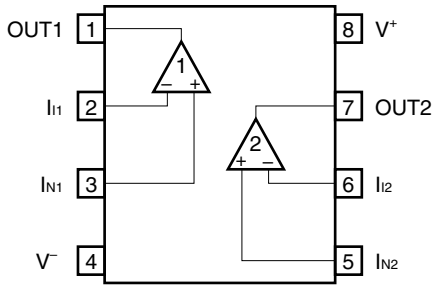
Ordering Information

Part Number	Package	Package Code (Previous Package Code)	Package Abbreviation	Supplying Form
μPC4072MF-DAA-E1-AT *1	8-pin plastic SOP (3.9 × 4.9)	PRSP0008DM-A (–)	MF	• 12 mm wide embossed taping • Pin 1 on draw-out side • 2500 p/reel

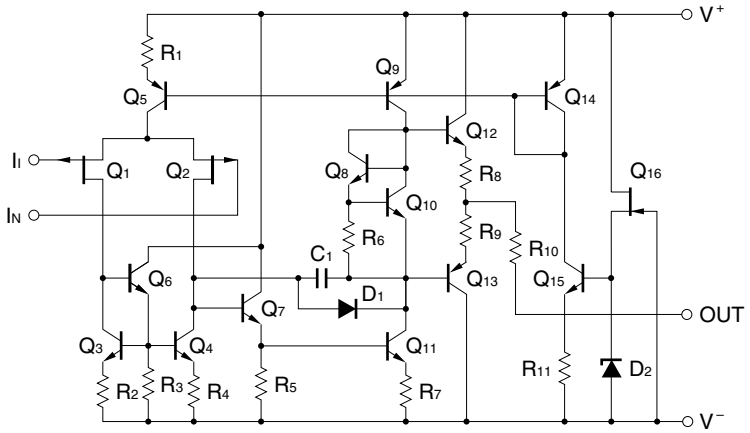
Note: *1. Pb-free (This product does not contain Pb in the external electrode and other parts.)

Caution Do not use the products in applications such as the transportation equipment (a car, a train, a ship, etc.) where “Special quality grade” is required, because the products are placed in a quality grade “standard” to be required at general devices.

Pin Configuration (Top View)



Equivalent Circuit (for Each Circuit)



Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Ratings	Unit
Voltage between V^+ and V^- *1	$V^+ - V$	−0.3 to +36	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage *2	V_I	V^- − 0.3 to V^+ + 0.3	V
Output Applied Voltage *3	V_O	V^- − 0.3 to V^+ + 0.3	V
Total Power Dissipation *4	P_T	440	mW
Output Short Circuit Duration (vs. GND) *5	t_s	Indefinite	s
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

Notes: *1. Note that reverse connections of the power supply may damage ICs.

*2. The input voltage is allowed to input without damage or destruction independent of the magnitude of V^+. Either input signal is not allowed to go negative by more than 0.3 V. In addition, the input voltage that operates normally as an operational amplifier is within the Common Mode Input Voltage range of an electrical characteristic.

*3. A range where input voltage can be applied to an output pin externally with no deterioration or damage to the feature (characteristic). The input voltage can be applied regardless of the electric supply voltage. This specification which includes the transition state such as electric power ON/OFF must be kept.

*4. This is the value in $T_A \leq 56°C$ of when the glass epoxy substrate (size: 100 mm x 100 mm, thickness: 1 mm, 15% of the substrate area where only one side is copper foiled is filling wired) is mounted. Derate at −6.4 mW/°C when $T_A > 56°C$. In the condition same as the above, Junction − ambient thermal resistance $R_{th(J-A)}$ = 156°C/W.

*5. Only as for $V^+ \leq 15V$ and any 1 channel. Please use the product within the derating condition or Total Power Dissipation, which are showed in Note *4.

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage (Split)	$V^{\pm}$	±5		±16	V
Output Current	I_O			±10	mA
Capacitive Load (A_V = +1, R_f = 0 Ω)	C_L			100	pF

Electrical Characteristics (T_A = 25°C, $V^{\pm}$ = ±15 V)

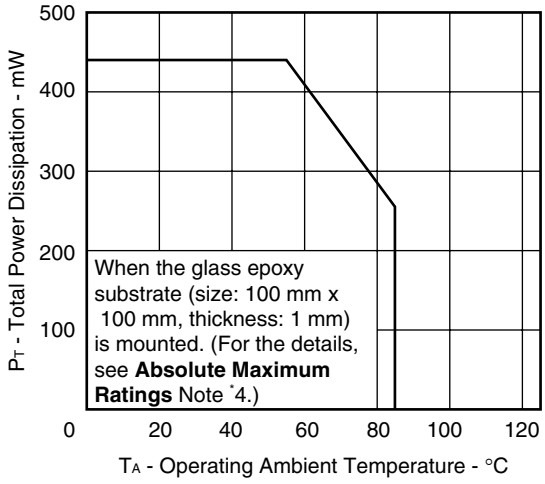
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Conditions
Input Offset Voltage	V_{IO}		±2	±10	mV	R_S ≤ 50 Ω
Input Offset Current	I_{IO}		±5	±50	pA	
Input Bias Current *1	I_B		30	200	pA	
Large Signal Voltage Gain	A_V	25000	200000			R_L ≥ 2 kΩ, V_O = ±10 V
Supply Current *2	I_{CC}		4	5.0	mA	I_O = 0 A
Common Mode Rejection Ratio	CMR	70	90		dB	
Supply Voltage Rejection Ratio	SVR	70	90		dB	
Output Voltage Swing	V_{om}	±12	±13.5		V	R_L ≥ 10 kΩ
		±10	±12		V	R_L ≥ 2 kΩ
Common Model Input Voltage Range	V_{ICM}	±10	+15 −13		V	
Slew Rate	SR		13		V/μs	A_V = +1
Unity Gain Frequency	f_{unity}		3		MHz	
Input Equivalent Noise Voltage	V_n		4		$\mu V_{r.m.s.}$	R_S = 100 Ω, f = 10 Hz to 10 kHz
Input Equivalent Noise Voltage Density	e_n		17		nV/√Hz	R_S = 100 Ω, f_O = 1 kHz
Channel Separation			120		dB	
Input Offset Voltage	V_{IO}			±13	mV	R_S ≤ 50 Ω, T_A = −20 to 70°C
Average V_{IO} Temperature Drift	$\Delta V_{IO}/\Delta T$		±10		μV/°C	T_A = −20 to 70°C
Input Offset Current *1	I_{IO}			±2	nA	T_A = −20 to 70°C
Input Bias Current *1	I_B			7	nA	T_A = −20 to 70°C

Notes: *1. Input bias currents flow into IC. Because each current is gate leak current of P-channel J-FET on input stage. And that are temperature sensitive. Short time measuring method is recommendable to maintain the junction temperature close to the operating ambient temperature.

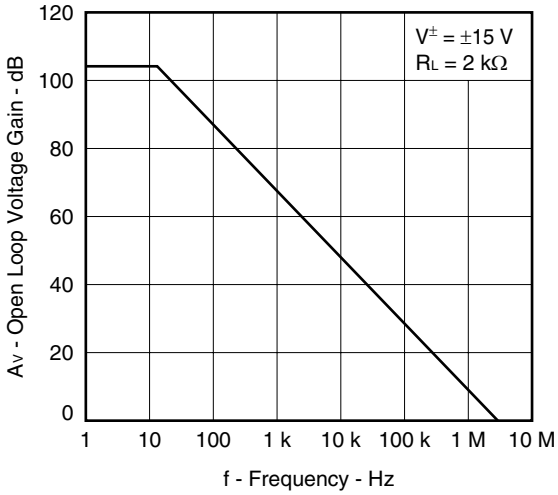
*2. This current flows irrespective of the existence of use.

Typical Characteristics (T_A = 25°C, TYP.) (Reference value)

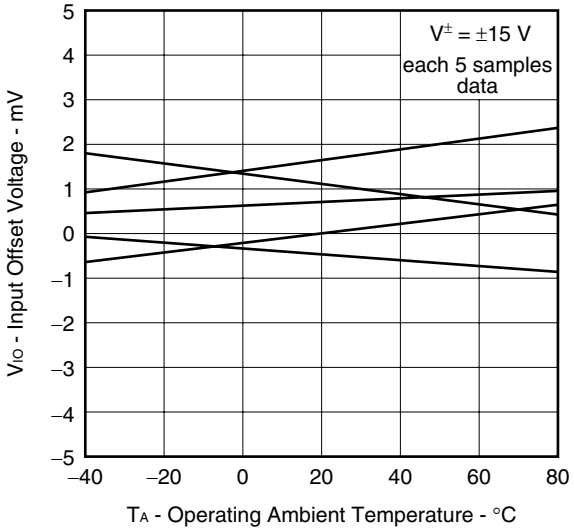
P_T vs. T_A



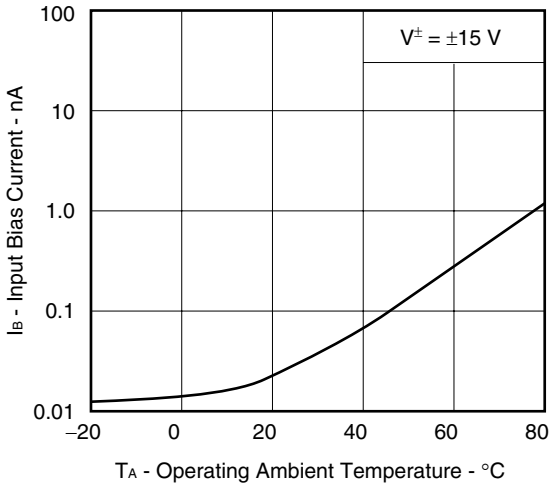
OPEN LOOP FREQUENCY RESPONSE



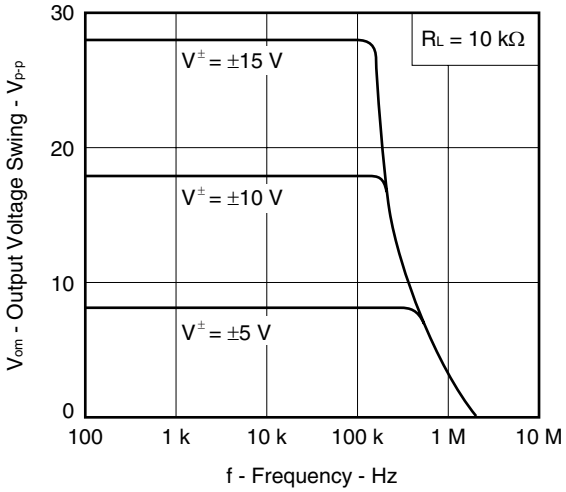
INPUT OFFSET VOLTAGE



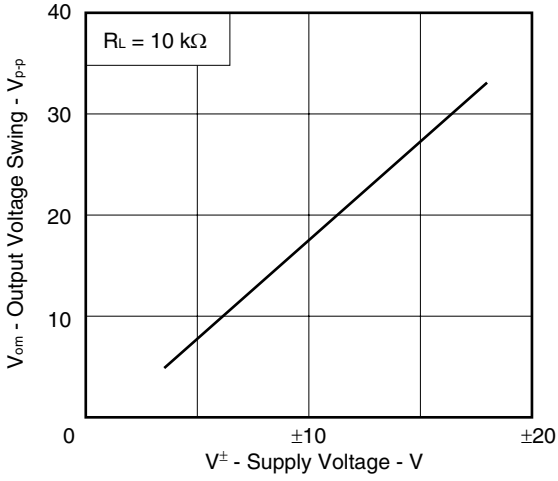
INPUT BIAS CURRENT



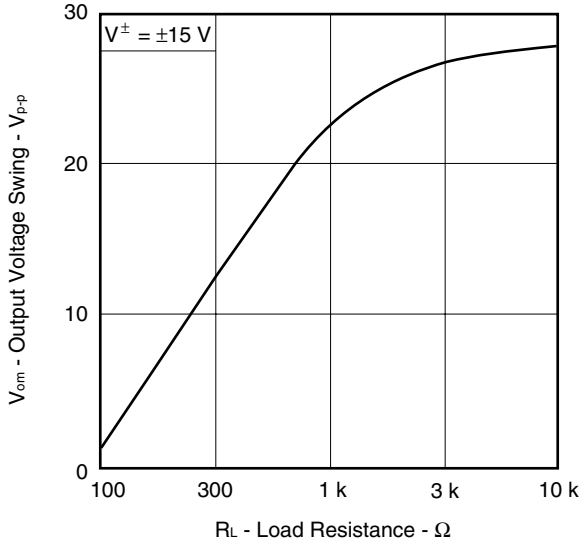
LARGE SIGNAL FREQUENCY RESPONSE



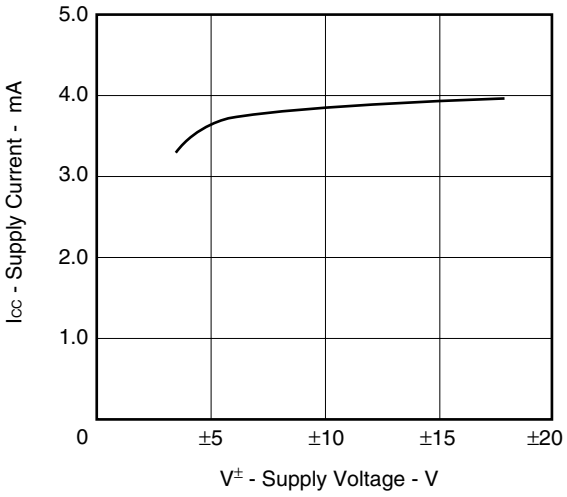
OUTPUT VOLTAGE SWING



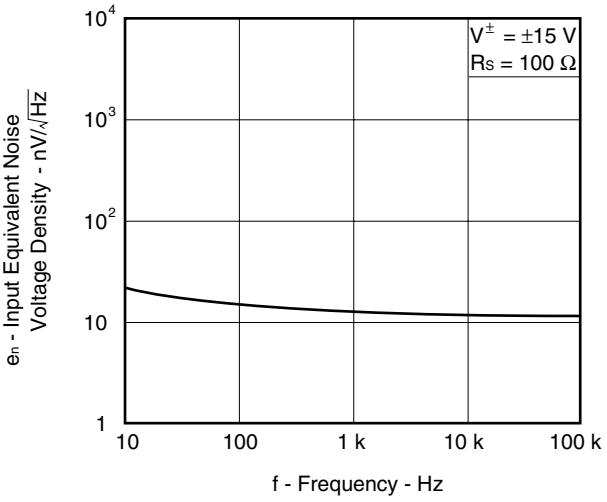
OUTPUT VOLTAGE SWING



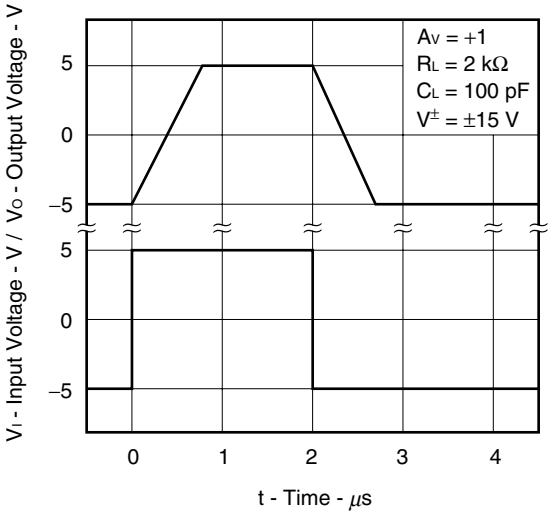
SUPPLY CURRENT vs. SUPPLY VOLTAGE



INPUT EQUIVALENT NOISE VOLTAGE DENSITY



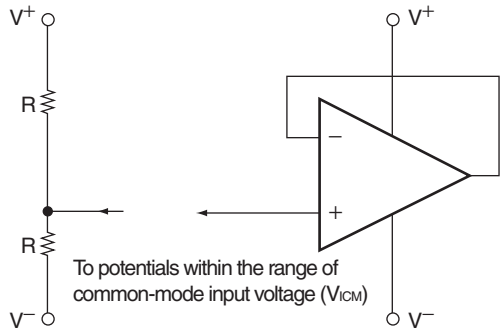
VOLTAGE FOLLOWER PULSE RESPONSE



PRECAUTIONS FOR USE

- **The process of unused circuits**
  If there is an unused circuit, the following connection is recommended.

Process example of unused circuits



Remark: A midpoint potential of V^+ and V^- is applied to this example.

- **Power supply used (Split/Single)**
  The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.

- **Ratings of input/output pin voltage**
  When the voltage of input/output pin exceeds the absolute maximum rating, it may cause degradation of characteristics or damages, by a conduction of a parasitic diode within an IC. In addition, when the input pin may be lower than V^-, or the output pin may exceed the power supply voltage, it is recommended to make a clump circuit by a diode whose forward voltage is low (e.g.: Schottky diode) for protection.

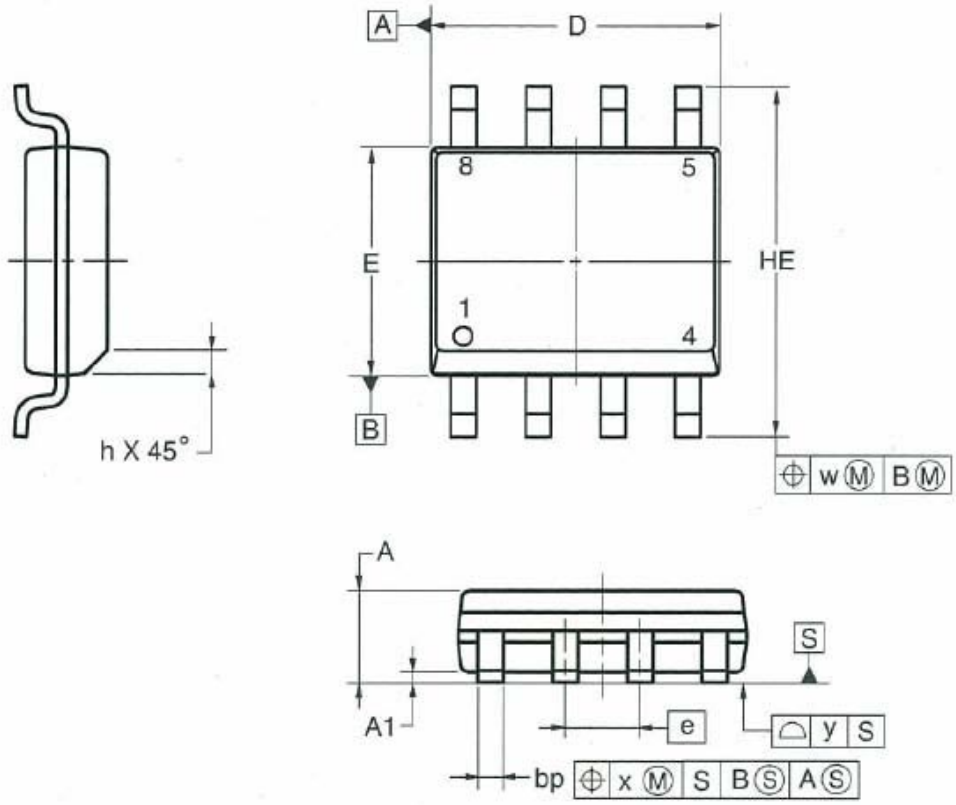
- **Range of common-mode input voltage**
  When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.
  V_{ICM} (TYP.): V^- +2 to V^+ (V) (T_A = 25°C)
  During designing, temperature characteristics for use with allowance.

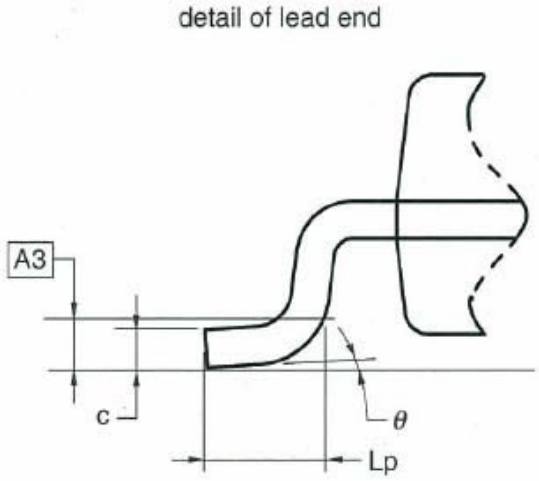
- **The maximum output voltage**
  The range of the TYP. value of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:
  $V_{om}{}^+$ (TYP.): V^+ −1.5 (V) (T_A = 25°C), $V_{om}{}^-$ (TYP.): V^- + 1.5 (V) (T_A = 25°C)
  During designing, consider variations in characteristics and temperature characteristics for use with allowance.
  In addition, also note that the output voltage range ($V_{om}{}^+ - V_{om}{}^-$) becomes narrow when an output current increases.

- **Handling of ICs**
  When stress is added to ICs due to warpage or bending of a board, the characteristic fluctuates due to piezoelectric effect. Therefore, pay attention to warpage or bending of a board.

Package Drawings

8-pin Plastic SOP (3.9 × 4.9)





(UNIT:mm)

ITEM	DIMENSIONS
D	4.80 to 5.00
E	3.80 to 4.00
HE	5.80 to 6.20
e	1.27
bp	0.35 to 0.49
A	1.35 to 1.75
A1	0.10 to 0.25
A3	0.25
c	0.19 to 0.25
Lp	0.40 to 1.25
h	0.25 to 0.50
w	0.25
x	0.25
y	0.10
θ	0° to 7°

Revision History	μPC4072MF-DAA Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Jul 25, 2012	–	First Edition Issued

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