NEC

NEC Electronics Inc.

μPC624
8-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER

Description

The μPC624 is a monolithic multiplying digital-to-analog converter designed for high speed performance and design/application flexibility. Advanced circuit design allows settling time of 85 ns. The outputs are high impedance dual complementary current types, which allow simple resistive loading, op-amp voltage conversion, and other configurations. The adjustable threshold logic input allows connection to all popular logic families.

Features

- ☐ Wide range multiplying capability
- ☐ Wide power supply range ±5 V to ±18 V
- ☐ High output impedance and compliance
- ☐ Variable logic threshold
- ☐ Direct interface to TTL, CMOS, PMOS
- ☐ Differential current outputs
- ☐ Pin to pin compatible with PMI'S DAC-08

Ordering Information

Part Number	Package	Operating Temperature Range
μPC624C	Plastic DIP	−20°C to −70°C
μPC624D	Ceramic DIP	−20°C to −80°C

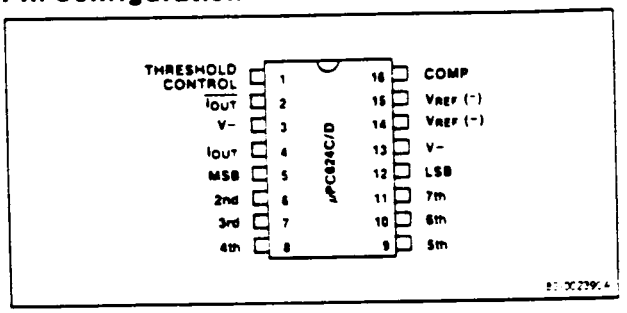
Absolute Maximum Ratings

T_A = 25°C

Supply Voltage	36 V
Logic Inputs	V⁻ to (V⁻ −36 V)
Logic Threshold Control Voltage	V⁻ to V⁻
Analog Current Outputs	4.2 mA
Reference Inputs	V⁻ to V⁻
Reference Input Differential Voltage	±18 V
Reference Input Current	5.0 mA
Power Dissipation, D or C Package	500 mW
Operating Temperature Range, D Package	−20 to +80°C
Operating Temperature Range, C Package	−20 to +70°C
Storage Temperature Range, D Package	−55 to +150°C
Storage Temperature Range, C Package	−55 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

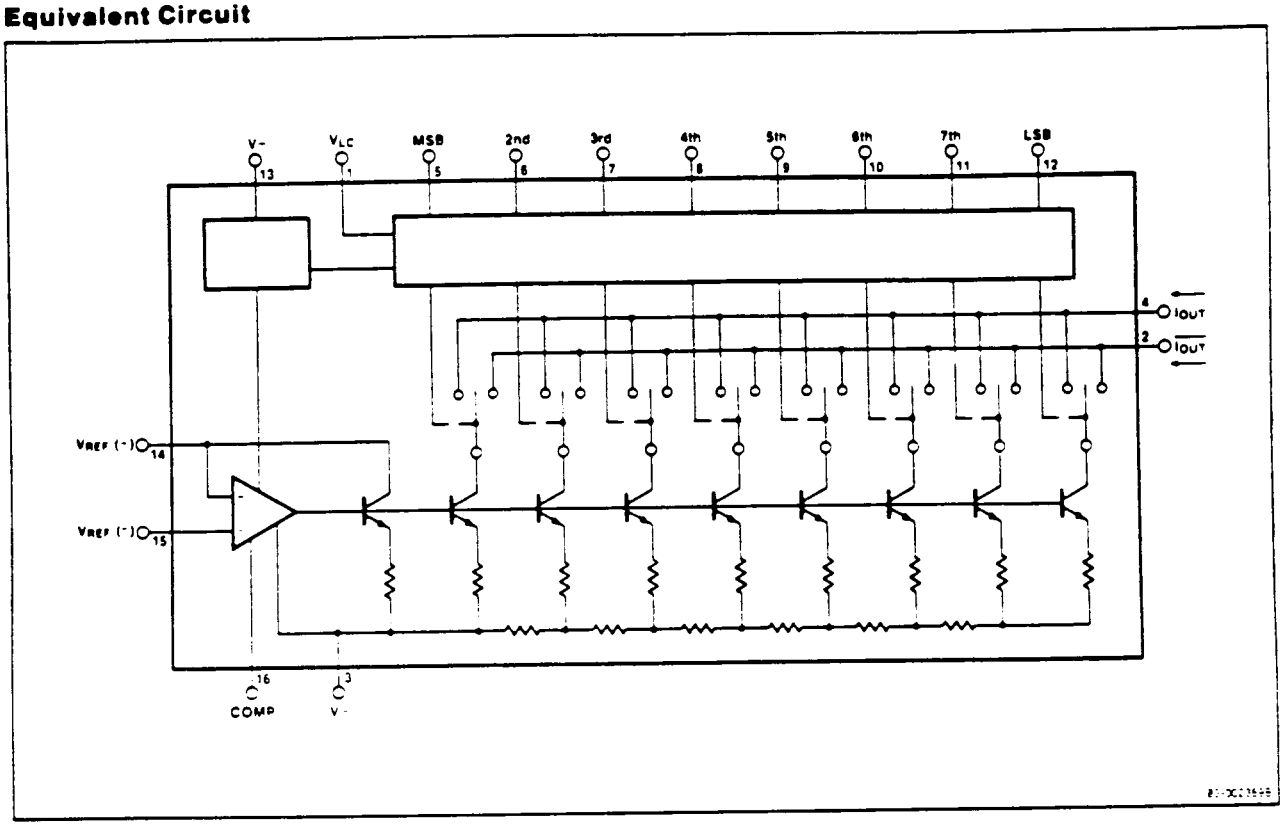
Pin Configuration



Pin Identification

Pin	Name	Function
1	Threshold Control	
2	I_{OUT}	Current Output
3	V−	Power Supply Negative
4	I_{OUT}	Current Output
5	MSB	Data Bit 1
6	2nd	Data Bit 2
7	3rd	Data Bit 3
8	4th	Data Bit 4
9	5th	Data Bit 5
10	6th	Data Bit 6
11	7th	Data Bit 7
12	LSB	Data Bit 8
13	V−	Power Supply Positive
14	V_{REF}−	Positive Reference Voltage
15	V_{REF}−	Negative Reference Voltage
16	Compensation	Amp Compensation

Equivalent Circuit



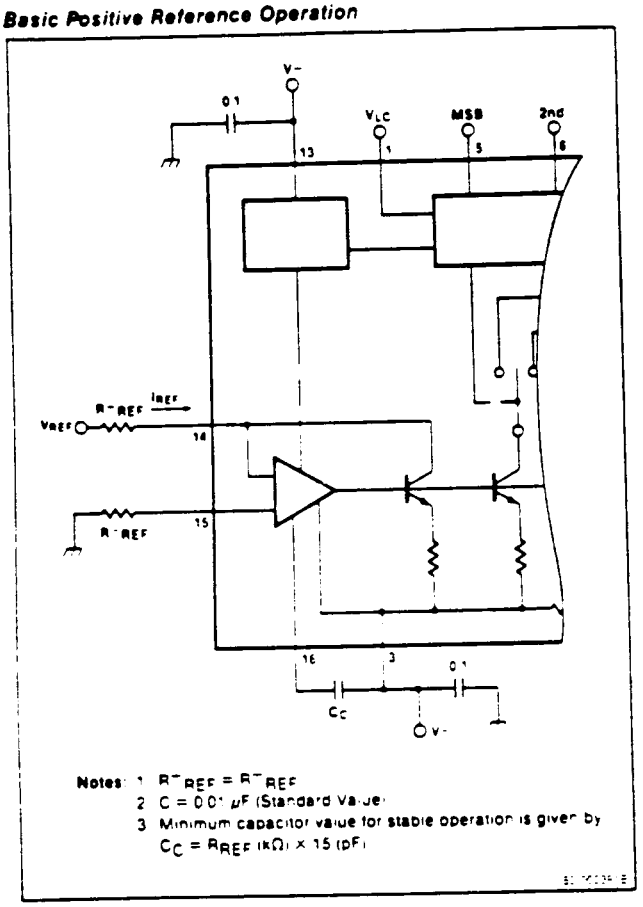
Electrical Characteristics

T_A = +25°C, $V^{\pm}$ = ±15 V, I_{REF} = 2.0 mA

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	8	8	Bit	
Monotonicity		8	8	8	Bit	
Nonlinearity	NL			0.19	%FSR	
Settling Time	T_S		85	150	ns	±½ LSB, $R_L \leq 50\ \Omega$ All bits ON/OFF
Full Scale Temperature Coefficient			10	50	ppm/°C	
Output Voltage Compliance	V_{OC}	−10		+18	V	$\Delta I_{FS} \leq$ ½ LSB
Full Scale Current	I_{FS}	1.94	1.99	2.04	mA	V_{REF} = 10.000 V, R^-_{REF} = 5.000 kΩ
Full Scale Symmetry	$I_{FS} - I_{FS}$		±1.0	±8.0	μA	
Zero Scale Offset Current	I_{ZS}		0.2	2.0	μA	
Output Current Range	I_O	0	2.0	2.1	mA	V^- = 5.0 V
		0	2.0	4.2	mA	V^- = 8.0 V to −18 V
Low Level Input Voltage	V_{IL}			0.8	V	V_{LC} = 0 V, Bit "OFF"
High Level Input Voltage	V_{IH}	2.0			V	V_{LC} = 0 V, Bit "ON"
Low Level Input Current	I_{IL}		−2.0	−10	μA	V_{LC} = 0 V, V_{IN} = −10 V to −0.8 V
High Level Input Current	I_{IH}		0.002	10	μA	V_{LC} = 0 V, V_{IN} = 2.0 V to 18 V
Logic Input Swing	V_{IS}	−10		−18	V	
Logic Threshold Range	V_{TH}	−10		−13.5	V	$V_{TH} \approx V_{LC}$ − 1.3 V
Reference Bias Current	I_{b-}			−3	μA	
Reference Input Slew Rate	$\Delta I_{REF}/\Delta T$	4.0	8.0		mA/μs	$R_{REF} \leq 200\ \Omega$, C_C = 0 pF
Power Supply Voltage Rejection Ratio	SVRR− V		0.0003	0.01	%FSR/%	V^- = 4.5 to 18 V, I_{REF} = 1 mA
	SVRR− V		0.002	0.01	%FSR/%	V^- = −4.5 to −18 V, I_{REF} = 1 mA
Power Supply Current	I^-		2.5	3.8	mA	
	I^-		−6.5	−7.8	mA	
	I^-		2.4	3.8	mA	V^- = 5 V, V^- = −15 V, I_{REF} = 2 mA
	I^-		−6.4	−7.8	mA	V^- = 5 V, V^- = −15 V, I_{REF} = 2 mA
	I^-		2.3	3.8	mA	$V^{\pm}$ = ±5 V, I_{REF} = 1 mA
	I^-		−4.3	−5.8	mA	$V^{\pm}$ = ±5 V, I_{REF} = 1 mA

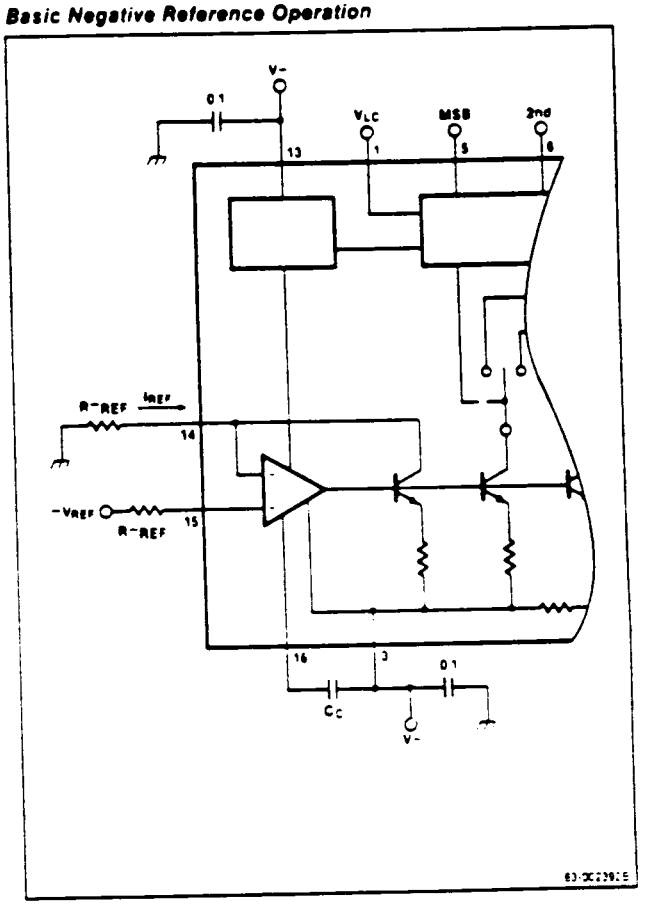
Typical Applications

Basic Positive Reference Operation

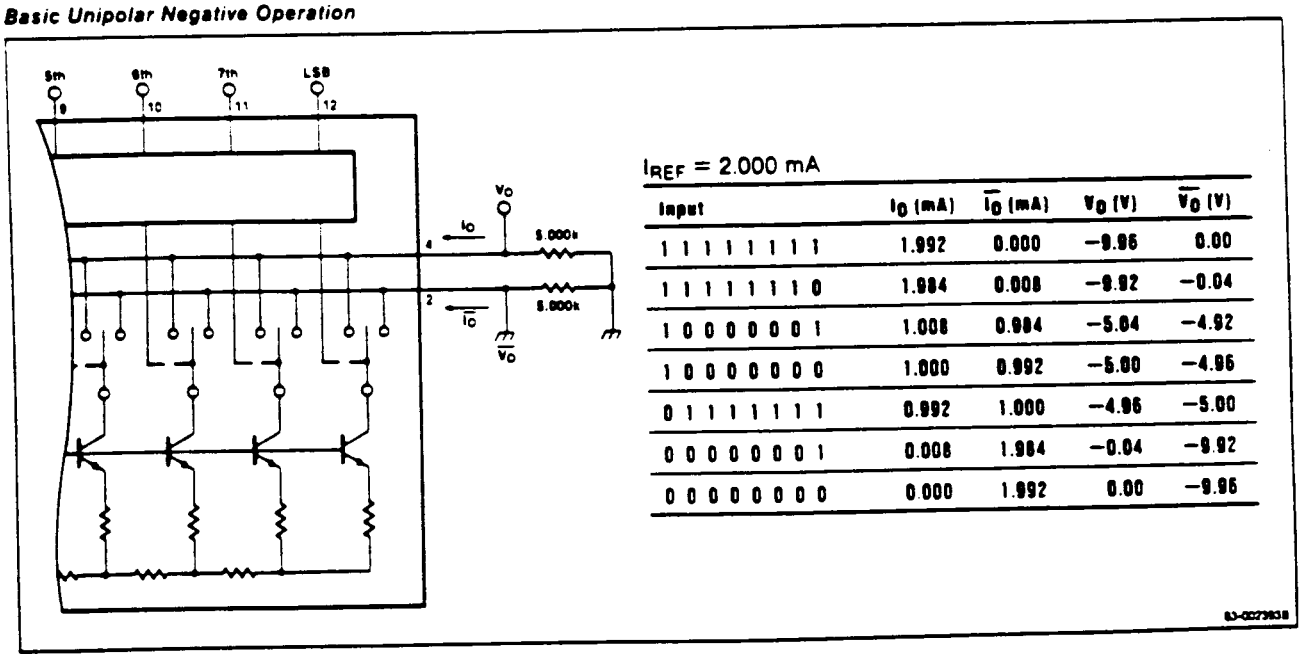


Notes: 1. $R^{-}_{REF} = R^{-}_{REF}$
2. C = 0.01 μF (Standard Value)
3. Minimum capacitor value for stable operation is given by $C_C = R_{REF}\ (k\Omega) \times 15\ (pF)$

Basic Negative Reference Operation



Basic Unipolar Negative Operation

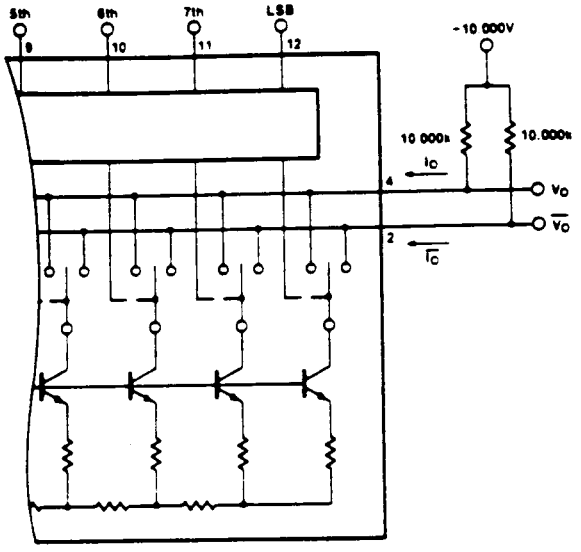


I_{REF} = 2.000 mA

Input	I_O (mA)	$\overline{I_O}$ (mA)	V_O (V)	$\overline{V_O}$ (V)
1 1 1 1 1 1 1 1	1.992	0.000	−9.96	0.00
1 1 1 1 1 1 1 0	1.984	0.008	−9.92	−0.04
1 0 0 0 0 0 0 1	1.008	0.984	−5.04	−4.92
1 0 0 0 0 0 0 0	1.000	0.992	−5.00	−4.96
0 1 1 1 1 1 1 1	0.992	1.000	−4.96	−5.00
0 0 0 0 0 0 0 1	0.008	1.984	−0.04	−9.92
0 0 0 0 0 0 0 0	0.000	1.992	0.00	−9.96

Typical Applications (Cont.)

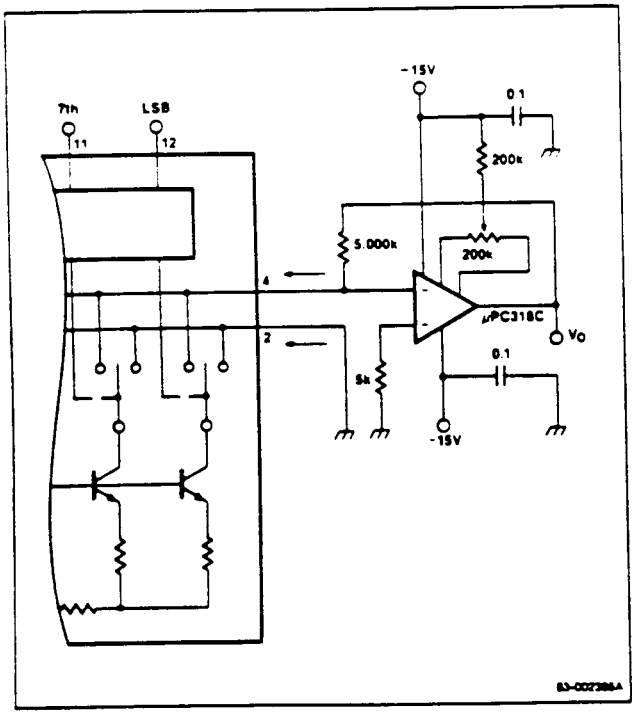
Basic Bipolar Output Operation



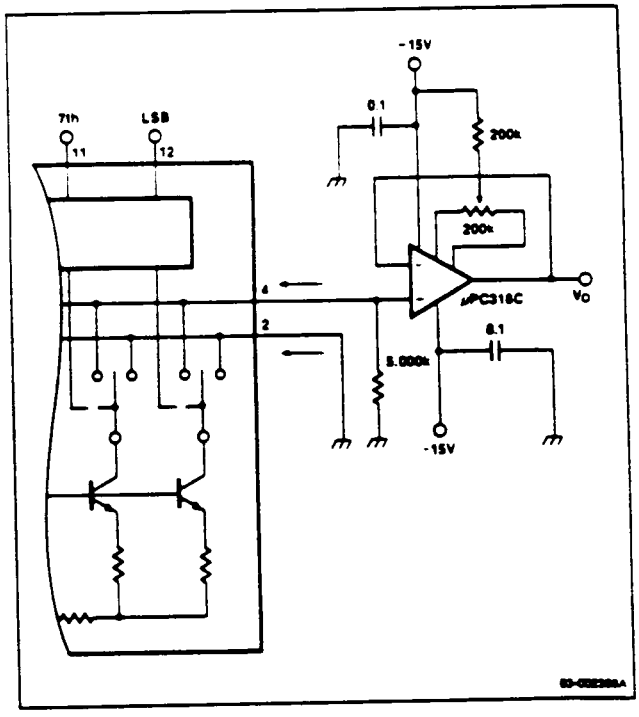
I_{REF} = 2.000 mA

Input	I_O (mA)	$\overline{I_O}$ (mA)	V_O (V)	$\overline{V_O}$ (V)
1 1 1 1 1 1 1 1	1.992	0.000	−9.92	+10.00
1 1 1 1 1 1 1 0	1.984	0.008	−9.84	+9.92
1 0 0 0 0 0 0 1	1.008	0.984	−0.08	+0.16
1 0 0 0 0 0 0 0	1.000	0.992	0.00	+0.08
0 1 1 1 1 1 1 1	0.992	1.000	−0.08	0.00
0 0 0 0 0 0 0 1	0.008	1.984	−9.92	−9.84
0 0 0 0 0 0 0 0	0.000	1.992	−10.00	−9.92

Positive Low Impedance Output Operation

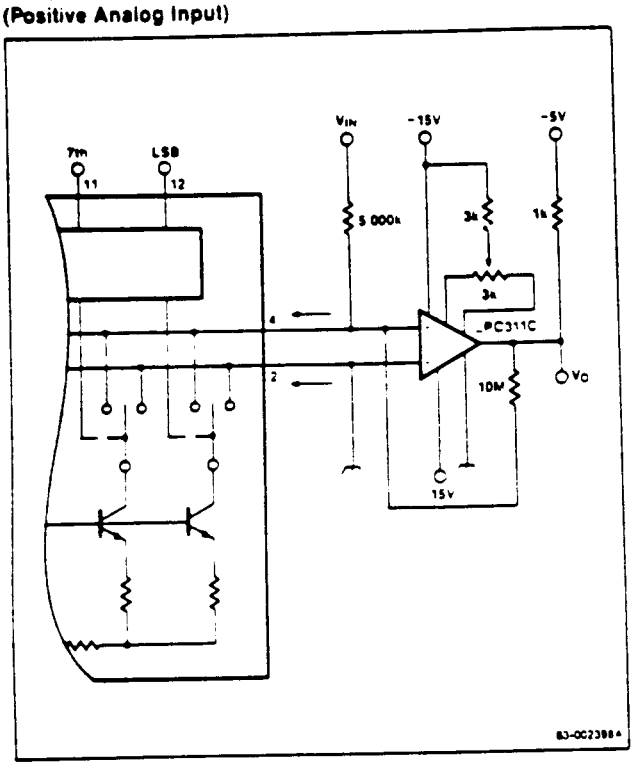


Negative Low Impedance Output Operation

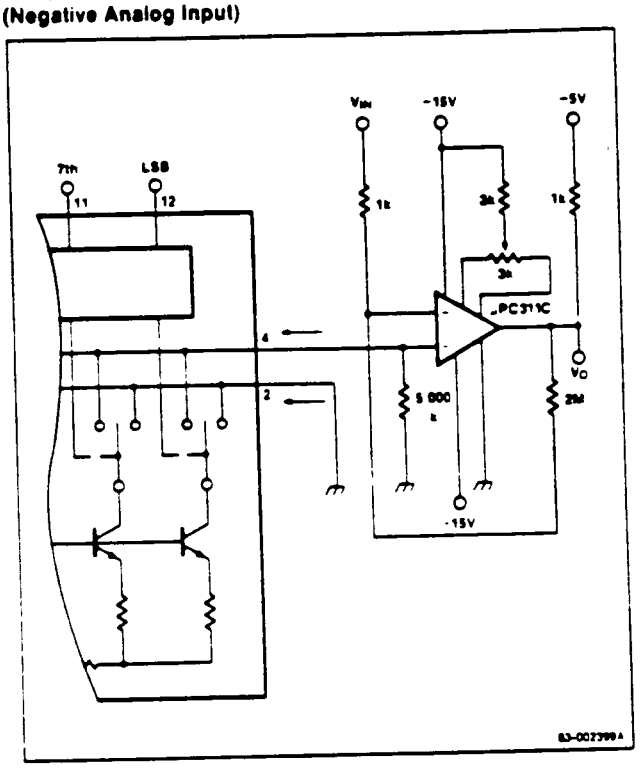


Typical Applications (Cont.)

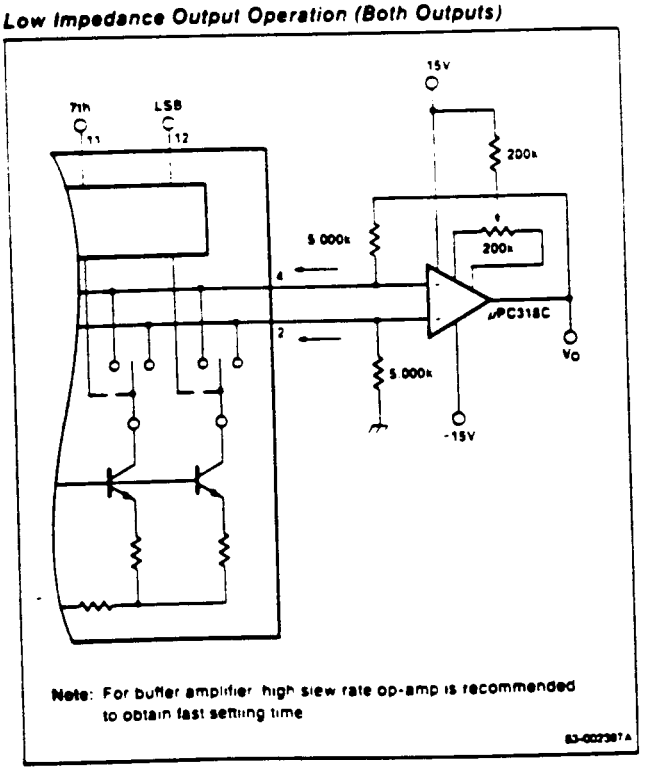
Comparator Connection Method for A/D Conversion
(Positive Analog Input)



Comparator Connection Method for A/D Conversion
(Negative Analog Input)



Low Impedance Output Operation (Both Outputs)



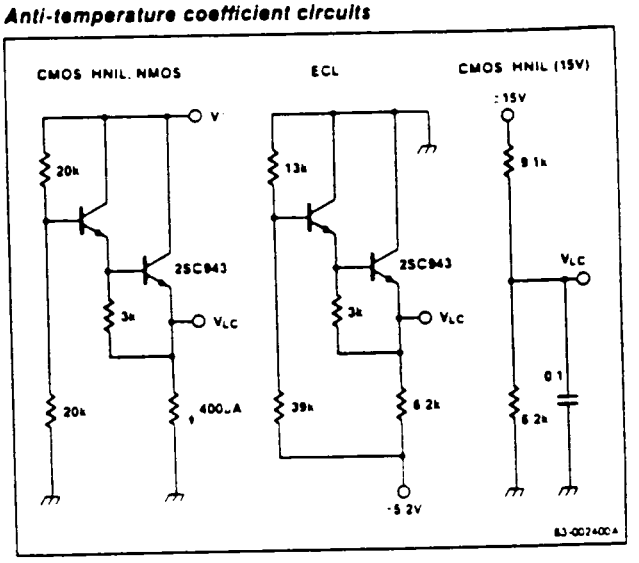
Note: For buffer amplifier high slew rate op-amp is recommended to obtain fast settling time

Interfacing with Various Logic Families

The logic threshold is set about 1.4 V above V_{LC}. This enables TTL level acceptance by simply grounding pin 1. By placing an appropriate voltage at the logic threshold control pin (pin 1), various threshold values are available for the other logic families.

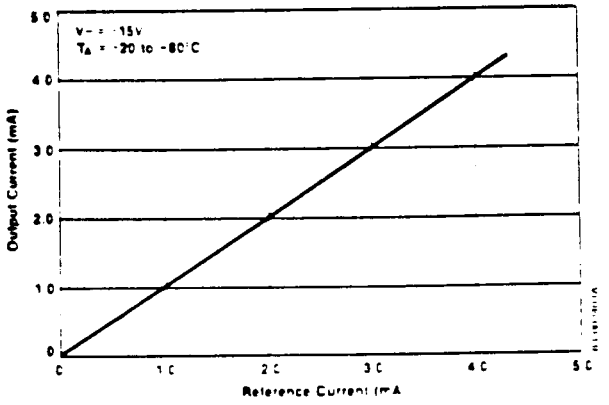
TTL interface permission gives the interval logic threshold −4 mV/°C temperature coefficient. $V_{TH} = V_{LC} + 1.4\ V - 0.004\ V \times (T_A - 25°C)$.

Anti-temperature coefficient circuits

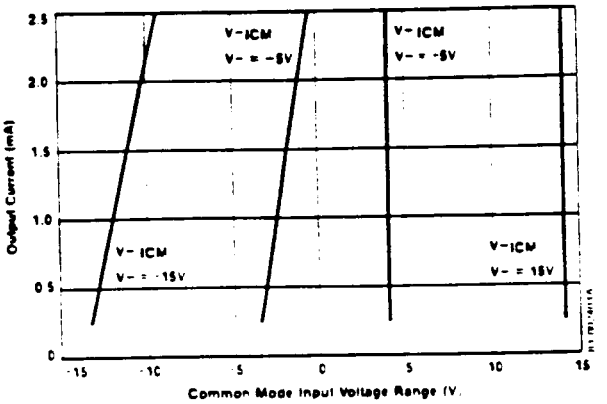


Operating Characteristics
(T_A = 25°C)

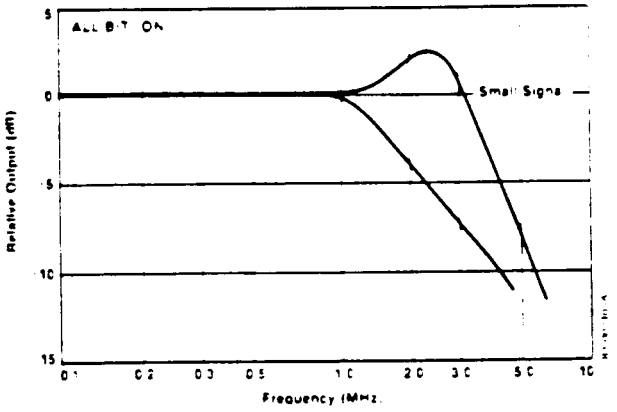
Full Scale Current



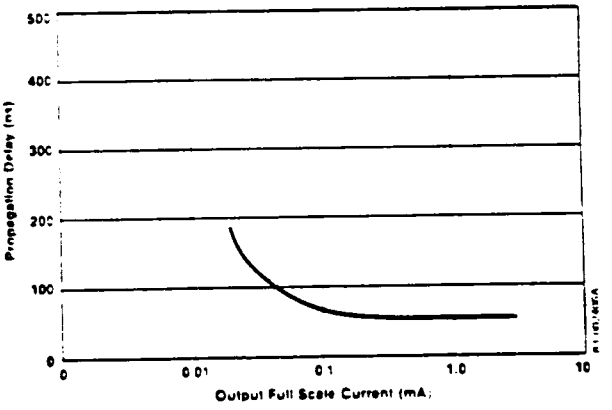
Full Scale Current



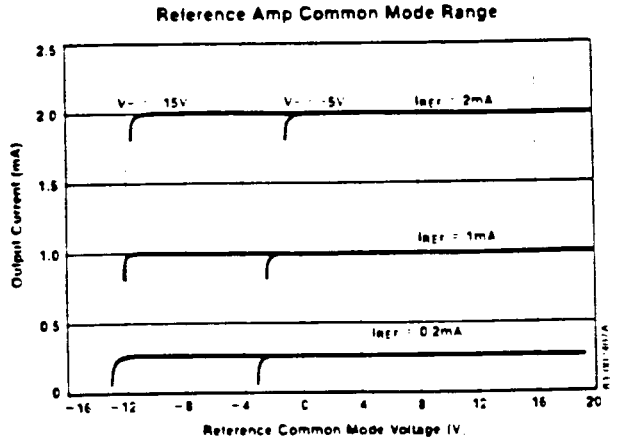
Reference Input Frequency Response



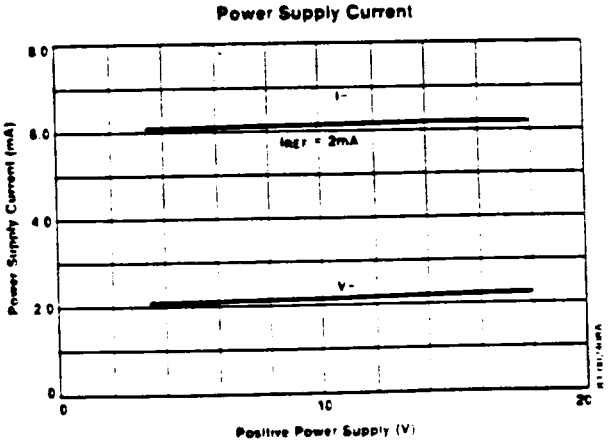
LSB Propagation Delay



Reference Amp Common Mode Range



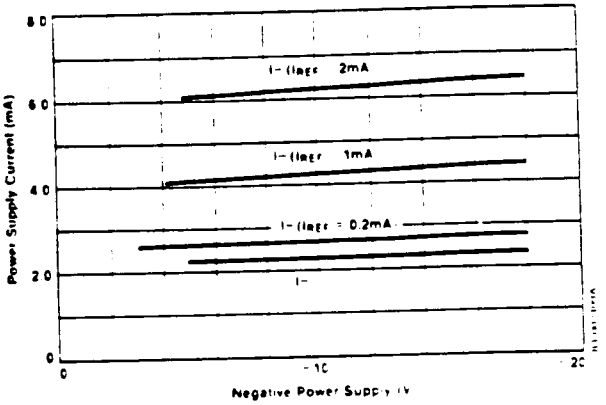
Power Supply Current



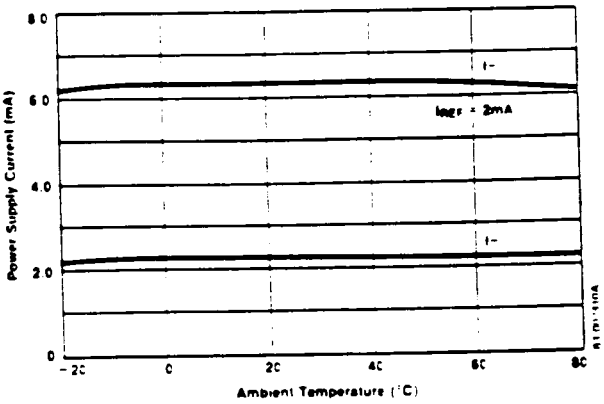
Operating Characteristics (Cont.)

(T_A = 25°C)

Power Supply Current



Power Supply Current



A/D Conversion Program List

0000		MVI	A, 89H	; CONTROL WORD FOR 8255
0002		OUT	(8255)	; PROGRAM TO 8255
0004		MVI	B, 80H	; BIT POINTER INITIALIZE
0006		MOV	A, B	; BIT SET WORD
0007	BIT TEST	OUT	(PORT B)	; BIT SET OUTPUT TO PB OF 8255
0009		MOV	C, A	
000A		NOP		
000B		IN	(PORT C)	; READ COMPARATOR
000D		RRC		; A_0 — CARRY FLG
000E		JC	DEC POINTER	; COMPARATOR TEST
0011		MOV	A, C	
0012		SUB	B	; BIT RESET
0013		MOV	C, A	
0014	DEC POINTER	MOV	A, B	
0015		RRC		; DECREMENT BIT POINTER
0016		JC	RETURN	; LSB WAS TESTED?
0019		MOV	B, A	
001A		ORA	C	; NEW BIT SET WORD
001B		JMP	BIT TEST	
001E	RETURN	RET	(MAIN PROGRAM)	; CONVERSION END & RETURN TO MAIN PROGRAM
	PROGRAM MEMORY		: 31 BYTE	
	CONVERSION TIME		: 371 μs (741 STATE) MAX. 323 μs (645 STATE) MIN (@ ϕ — 2 MHz)	
	WORKING REGISTER		:B & C (C REGISTER, FINAL ANSWER MEMORY)	