

BIPOLAR ANALOG INTEGRATED CIRCUIT

μ PC8002

SECOND MIXER + IF AMPLIFIER FOR DIGITAL CORDLESS TELEPHONES

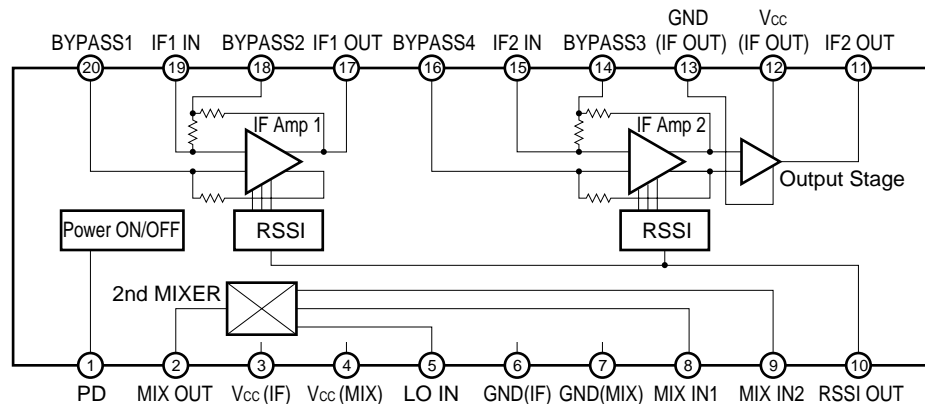
The μ PC8002 is a monolithic IC developed for use in digital cordless telephones. Its internal equivalent circuits comprise a double balanced mixer (DBM), IF amplifier circuit, and RSSI (Received Signal Strength Indicator) circuit. The μ PC8002 can operate on a wide range of power supply voltages from 2.7 V to 5.5 V, and incorporates a power-off function, making it ideal for achieving low set power consumption.

The package is a 20-pin plastic shrink SOP (225 mil) suitable for high-density surface mounting.

FEATURES

- Low-voltage, low-consumption-current operation possible ($V_{CC} = 2.7$ to 5.5 V, $I_{CC} = 3.4$ mA at $V_{CC} = 3$ V)
- Wide mixer input frequency range ($f_{MIX} = 250$ MHz (TYP.) to 500 MHz (MAX.))
- Wide IF amplifier input frequency range ($f_{IF} = 8$ MHz (MIN.) to 12 MHz (MAX.), 10.7 MHz (TYP.))
- High limiting sensitivity ($S_L = -100$ dBm (TYP.))
- Wide RSSI dynamic range ($D_R = 85$ dB (TYP.))
- On-chip power-off function
- Use of 20-pin plastic shrink SOP (225 mil) allows high-density surface mounting

BLOCK DIAGRAM

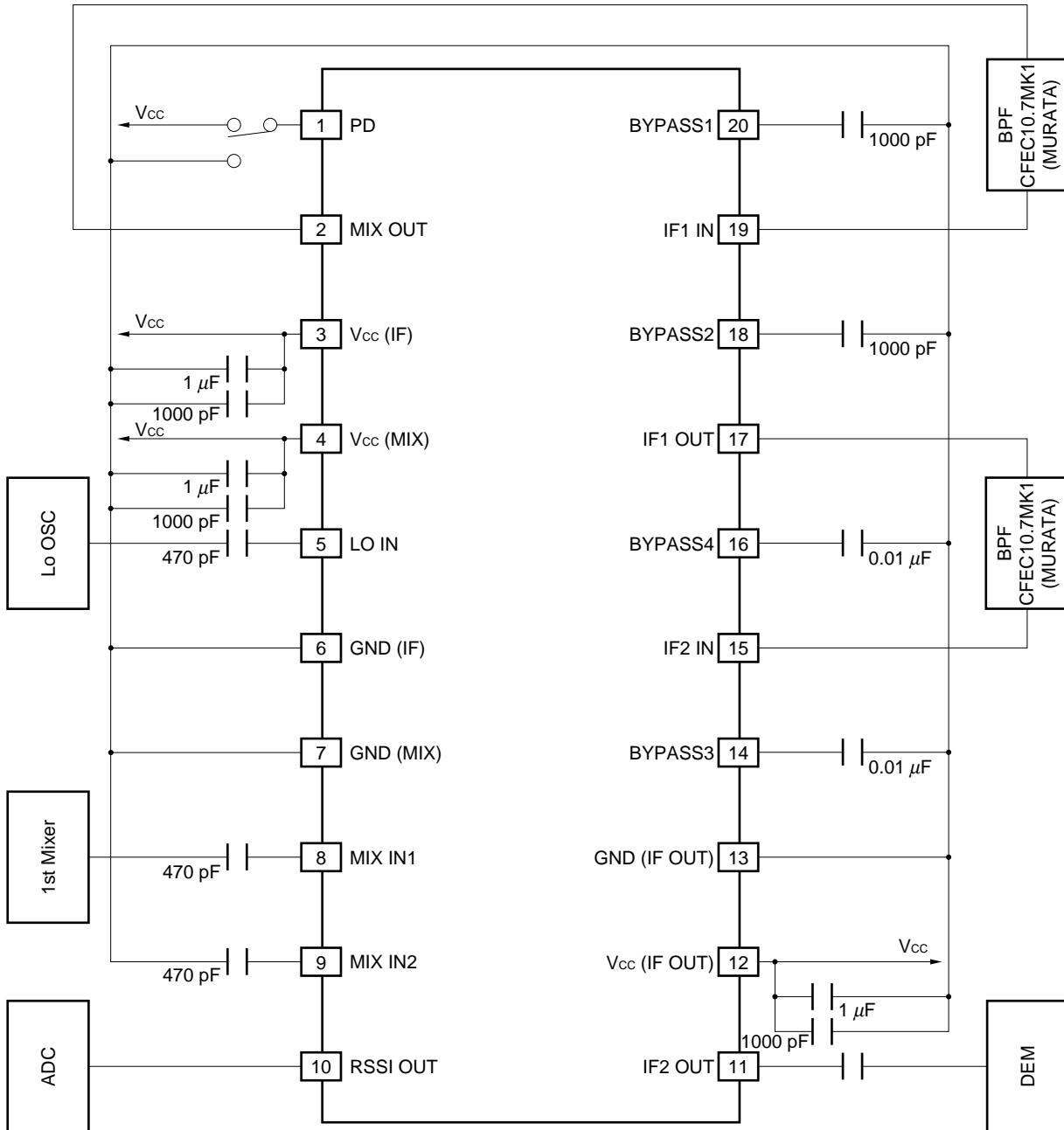


ORDERING INFORMATION

Part Number	Package
μ PC8002GR	20-pin plastic shrink SOP (225 mil)
μ PC8002GR-E1	20-pin plastic shrink SOP (225 mil) Embossed carrier taping (pin 1 is tape unwinding direction)
μ PC8002GR-E2	20-pin plastic shrink SOP (225 mil) Embossed carrier taping (pin 1 is tape winding direction)

The information in this document is subject to change without notice.

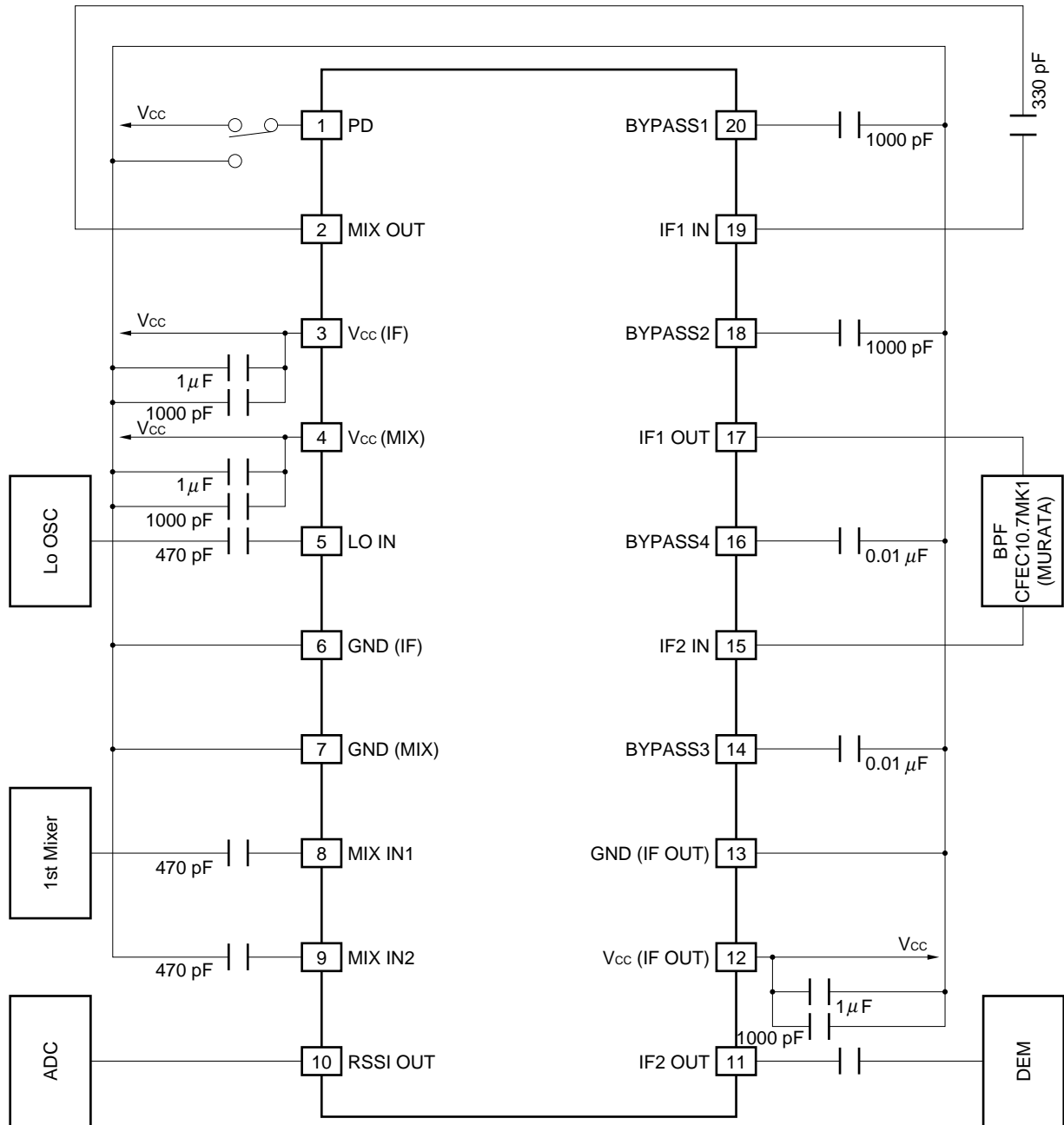
Application Circuit Example 1 (Using 2 BPFs)



Caution Ensure that the pin voltage does not exceed the power supply voltage.

Remark The Vcc pass capacitors (1 μF, 1000 pF) should be located close to the respective Vcc pins. Chip laminated ceramic capacitors (MURATA GRM36 or equivalent) should be used.

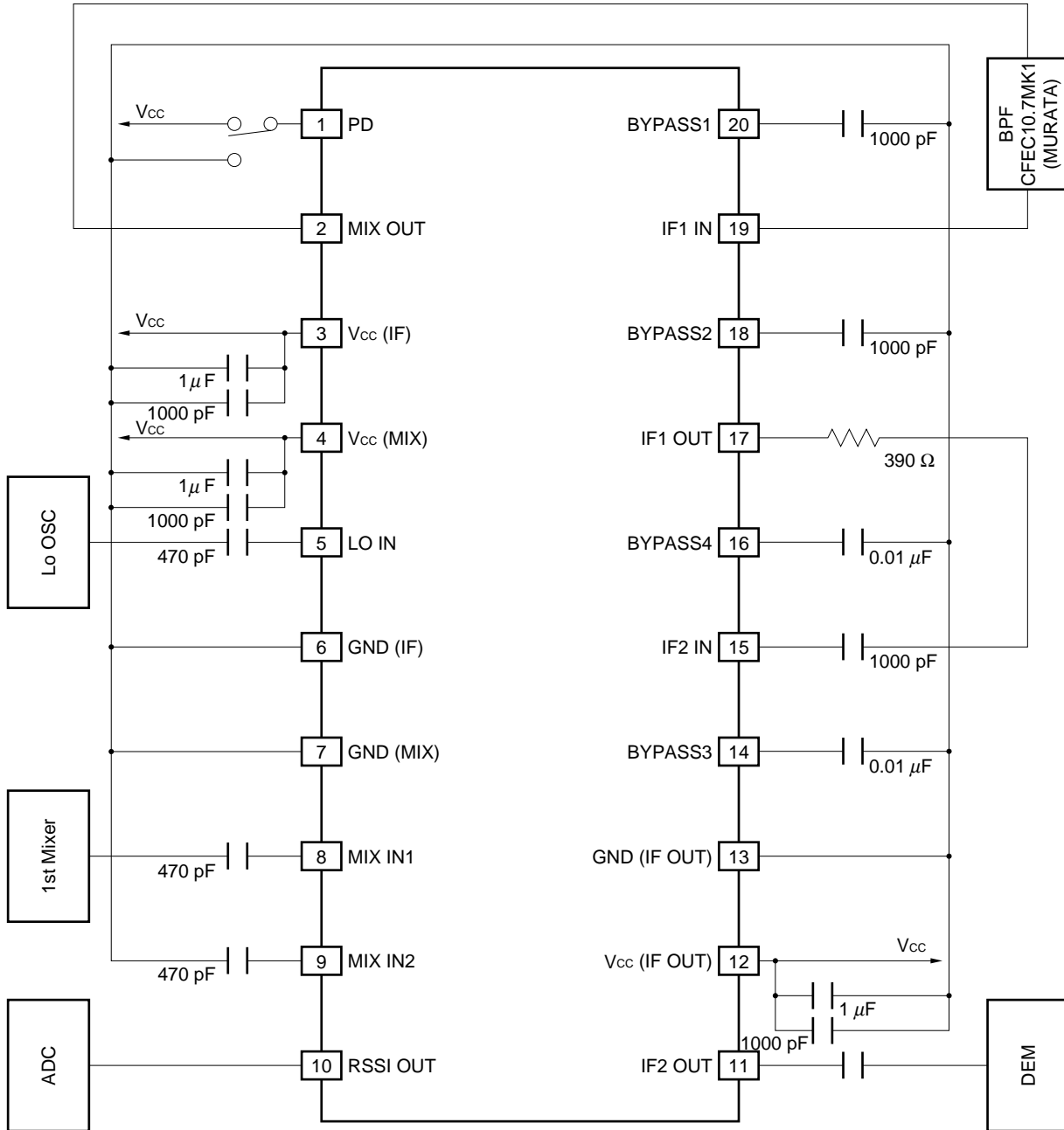
Application Circuit Example 2 (Using 1 BPF)



- Cautions**
1. Ensure that the pin voltage does not exceed the power supply voltage.
 2. With this application circuit, confirm that there is not problem with interfering wave characteristics.

Remark The Vcc pass capacitors (1 μF, 1000 pF) should be located close to the respective Vcc pins. Chip laminated ceramic capacitors (MURATA GRM36 or equivalent) should be used.

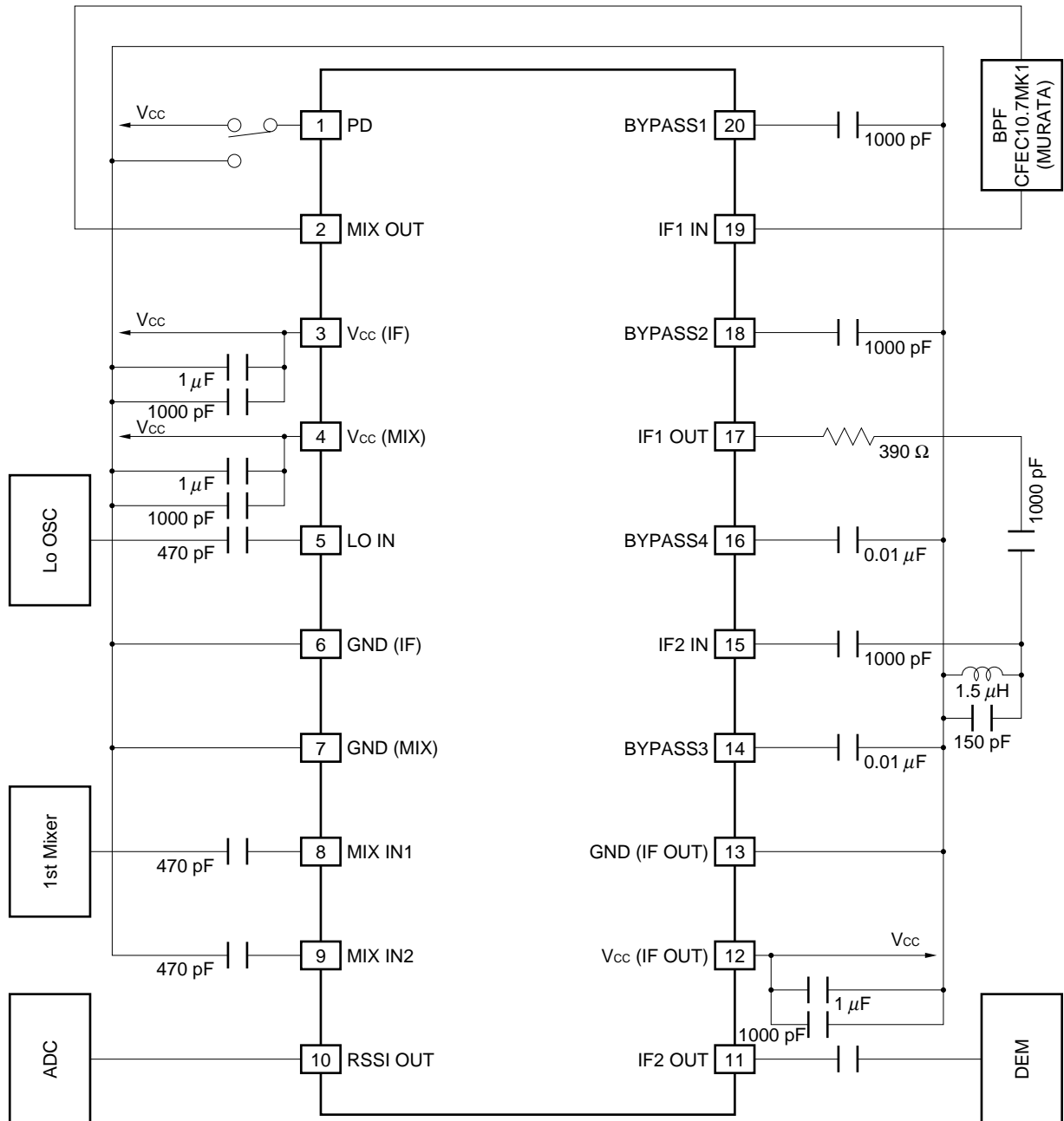
Application Circuit Example 3 (Using 1 BPF)



- Cautions**
1. With this application circuit, good interfering wave characteristics are obtained with a single BPF. However, there is a drop in sensitivity.
 2. Ensure that the pin voltage does not exceed the power supply voltage.

Remark The Vcc pass capacitors (1 μF, 1000 pF) should be located close to the respective Vcc pins. Chip laminated ceramic capacitors (MURATA GRM36 or equivalent) should be used.

Application Circuit Example 4 (Using 1 BPF)



- Cautions**
1. With this application circuit, good interfering wave characteristics are obtained with a single BPF (and sensitivity is better than in Application Circuit Example 3).
 2. Ensure that the pin voltage does not exceed the power supply voltage.

Remark The Vcc pass capacitors (1 μF, 1000 pF) should be located close to the respective Vcc pins. Chip laminated ceramic capacitors (MURATA GRM36 or equivalent) and a chip coil (MURATA LQHIN or equivalent) should be used.

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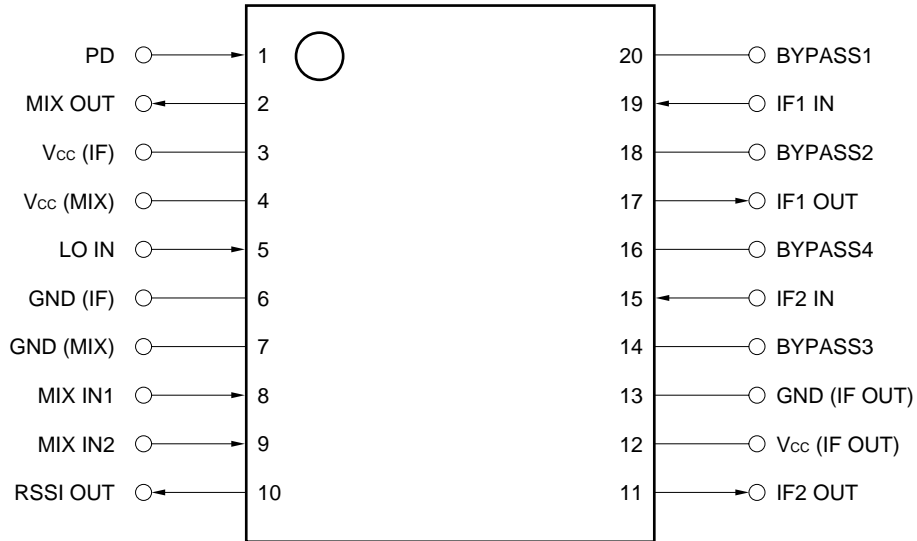
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1. PIN CONFIGURATION AND PIN FUNCTIONS

(1) Pin Configuration (Top View)

- 20-pin plastic shrink SOP (225 mil)



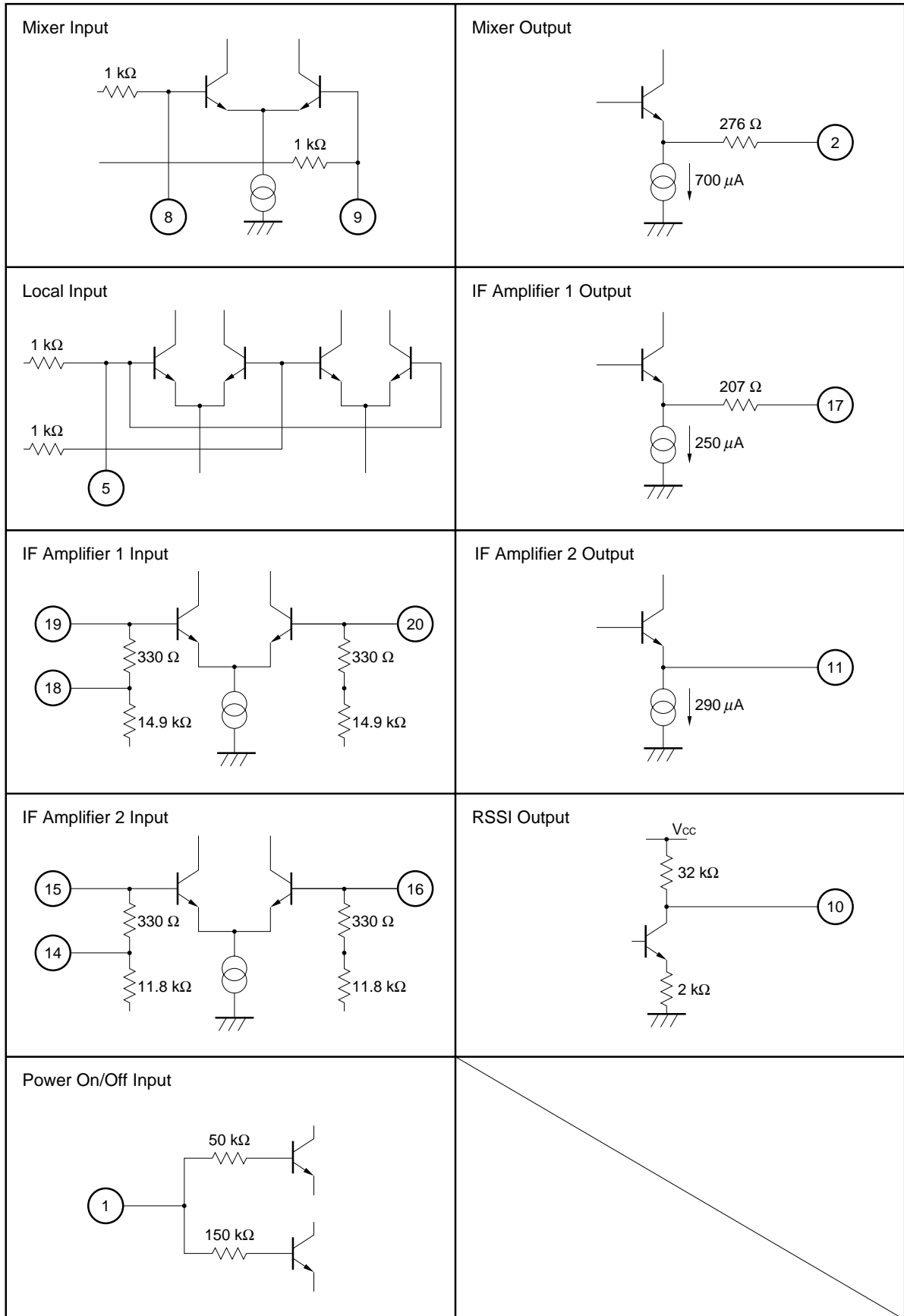
Pin Names

- BYPASS1-BYPASS4 : Bypass
- GND (IF) : Ground (Intermediate Frequency Amp.)
- GND (IF OUT) : Ground (Intermediate Frequency Amp. Output)
- GND (MIX) : Ground (Mixer)
- IF1 IN, IF2 IN : Intermediate Frequency Amp. Input
- IF1 OUT, IF2 OUT : Intermediate Frequency Amp. Output
- LO IN : Local Input
- MIX IN1, MIX IN2 : Mixer Input
- MIX OUT : Mixer Output
- PD : Power Down
- RSSI OUT : Received Signal Strength Indicator Output
- Vcc (IF) : Power Supply (Intermediate Frequency Amp.)
- Vcc (IF OUT) : Power Supply (Intermediate Frequency Amp. Output)
- Vcc (MIX) : Power Supply (Mixer)

(2) Pin Functions

No.	Pin Name	I/O	Function
1	PD	I	Power on/off control signal input
2	MIX OUT	O	Mixer output
3	V _{cc} (IF)	–	IF amplifier and RSSI power supply pin
4	V _{cc} (MIX)	–	Mixer power supply pin
5	LO IN	I	Local input
6	GND (IF)	–	IF amplifier and RSSI ground pin
7	GND (MIX)	–	Mixer ground pin
8	MIX IN1	I	Mixer input
9	MIX IN2	I	Filter capacitor connection
10	RSSI OUT	O	RSSI output
11	IF2 OUT	O	IF amplifier 2 output
12	V _{cc} (IF OUT)	–	IF amplifier output stage power supply pin
13	GND (IF OUT)	–	IF amplifier output stage ground pin
14	BYPASS3	–	Filter capacitor connection (IF2 side)
15	IF2 IN	I	IF amplifier 2 input
16	BYPASS4	–	Filter capacitor connection (IF2 side)
17	IF1 OUT	O	IF amplifier 1 output
18	BYPASS2	–	Filter capacitor connection (IF1 side)
19	IF1 IN	I	IF amplifier 1 input
20	BYPASS1	–	Filter capacitor connection (IF1 side)

2. INPUT/OUTPUT EQUIVALENT CIRCUIT DIAGRAMS



3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Test Condition	Rating	Unit
Power supply voltage	V _{CC}		7	V
Total power dissipation	P _T	T _A = 85 °C	120	mW
Storage temperature	T _{stg}		-40 to +125	°C
Pin voltage	V _{PIN}		V _{CC} +0.2	V

Caution Product quality may suffer if the absolute rating is exceeded for any parameter, even momentarily. In other words, an absolute maximum rating is a value at which the possibility of physical damage to the product cannot be ruled out. Care must therefore be taken to ensure that these ratings are not exceeded during use of the product.

Recommended Operating Ratings (T_A = 25 °C) 0 dBm = 223.6 mV_{rms} (at 50 Ω)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Power supply voltage	V _{CC}		2.7	3.0	5.5	V
Operating ambient temperature	T _A		-30	+25	+85	°C
Mixer input level	V _{MIX}	50 Ω resistance termination	-98		-18	dBm
		LC matching (reference value)	-107		-27	
Local input level	V _{LOC}	50 Ω resistance termination	-5		+5	dBm
		LC matching (reference value)	-20		-10	
IF amplifier input level	V _{IF}		-99		-14	dBm
Mixer input frequency	f _{MIX}			250	500	MHz
Mixer output frequency	f _{OM}		8	10.7	12	MHz
IF amplifier input frequency	f _{IF}		8	10.7	12	MHz
RSSI output load capacitance	C _{O1}			10 ^{Note}		pF
IF2 output load capacitance	C _{OR}				10 ^{Note}	pF

Note Includes all capacitances (board, pattern, etc.) applied to the pin.

Electrical Specifications (T_A = 25 °C, V_{CC} = 3 V)

(1) Mixer Section (f_{MIX} = 250 MHz, f_{LOC} = 239.3 MHz, V_{LOC} = -5 dBm) 0 dBm = 223.6 mV_{rms} (at 50 Ω)
 (Where not specified in the Test Condition, input has 50 Ω termination)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Power supply current	I _{CCM}	No signal		1.7	2.2	mA
Conversion gain	G _C	50 Ω resistance termination	4	8	11.0	dB
		LC matching (reference value)		17.0		
-1 dB compression output level	V _{OM}		-14	-10	-7	dBm
Third order intercept point	IP ₃	Stipulated by output Note 1		-3		dBm
Noise factor	NF			16		dB
		LC matching (reference value)		7		dB
Local separation	I _{SL}	Mixer non-input Note 2	40	54		dB
Mixer input impedance	Z _{INM}			31-j156		Ω
Local input impedance	Z _{INL}			31-j169		Ω
Output resistance	R _{OM}		230	330	430	Ω
Power-on rise time	t _{ONM}	V _{PO} = 3 V ^{Note 3}		8	15	μs
Power-off fall time	t _{OFM}	V _{PO} = 0 V ^{Note 4}		1	3	μs
Power-off power supply current	I _{LM}	V _{PO} = 0 V		0	5	μA

Notes 1. f₁ = 250.3 MHz, f₂ = 250.6 MHz

2. Leakage from local input to mixer output
3. Time until the difference between the local input pin power-on and power-off voltages reaches 90 %
 Power-on input voltage (V_{PO}) rise time: 10 ns
4. Time until the power supply current reaches 10 % of the power-on value
 Power-on input voltage (V_{PO}) fall time: 10 ns

(2) IF Amplifier Section ($f_{IF} = 10.7 \text{ MHz}$) 0 dBm = 223.6 mV_{rms} (at 50 Ω)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Power supply current	I _{CC1}	No signal		1.7	2.3	mA
Limiting sensitivity	S _L	-3 dB point		-100	-97	dBm
IF amplifier phase fluctuation	S _P	V _{IF} = -70 to -14 dBm Note 1		10		deg
IF amplifier output amplitude	V _O	IF2 OUT, V _{IF} = -14 dBm	0.2	0.3	0.4	V _{p-p}
IF amplifier output amplitude rise time	t _R	IF2 OUT, V _{IF} = -14 dBm		8	20	ns
IF amplifier output amplitude fall time	t _F	IF2 OUT, V _{IF} = -14 dBm		15	25	ns
IF amplifier input resistance	R _{in}	IF1 IN, IF2 IN	230	330	430	Ω
IF amplifier input capacitance	C _{in}	IF1 IN, IF2 IN		3.5	6.0	pF
IF amplifier output resistance	R _O	IF1 OUT	230	330	430	Ω
RSSI linearity	L _R	V _{IF} = -94 to -14 dBm			±2	dB
RSSI slope	S _R		18	20	22	mV/dB
RSSI intercept	I _R		-164.7	-148	-134.4	dBm
RSSI output voltage 1	V _{R1}	V _{IF} = -14 dBm	2.58	2.68	2.78	V
RSSI output voltage 2	V _{R2}	V _{IF} = -54 dBm	1.76	1.88	2.0	V
RSSI output voltage 3	V _{R3}	V _{IF} = -94 dBm	0.88	1.08	1.28	V
RSSI output voltage 4	V _{R4}	No signal		0.96	1.23	V
RSSI output temperature stability	S _T	V _{IF} = -94 to -14 dBm Note 2		±2		dB
RSSI output dynamic range	D _R	Note 3	80	90		dB
RSSI rise time	t _{rf1}	V _{IF} = -14 dBm Note 4		1.0	4	μs
RSSI fall time	t _{rf2}	V _{IF} = -14 dBm Note 4		1.6	4	μs
RSSI output ripple	R _R	V _{IF} = -14 dBm			20	mV _{p-p}
RSSI output resistance	R _{OR}		25.6	32	38.4	kΩ
Power-on rise time	t _{ON1}	V _{PO} = 3 V, no signal ^{Note 5}		5	10	μs
Power-off fall time	t _{OF1}	V _{PO} = 0 V ^{Note 6}		1	3	μs
Power-off power supply current	I _{LI}	V _{PO} = 0 V		6	10	μA

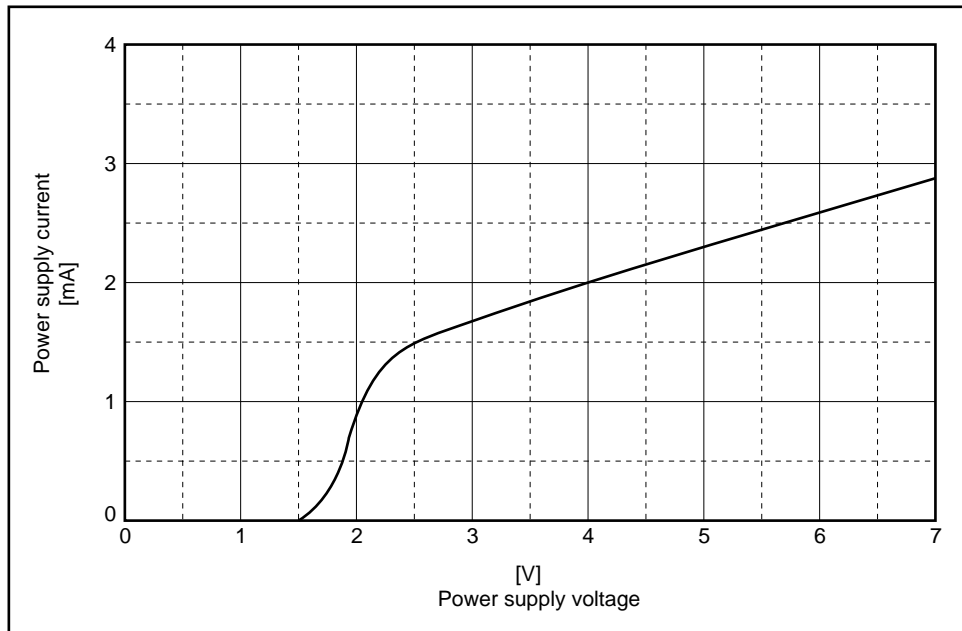
- Notes**
1. Network analyzer RBW = 3 Hz
 2. T_A = -30 °C to +85 °C
 3. Input level range for which drift from the regression expression with V_{IF} = -94 to -14 dBm is ≤ 2 dB
 4. Time until the RSSI output reaches the final value ±10 %
 5. Time until the RSSI output is within ±10 % of the power-on value
Power-on input voltage (V_{PO}) rise time: 10 ns
 6. Time until the power supply current reaches 10 % of the power-on value
Power-on input voltage (V_{PO}) fall time: 10 ns

(3) Power-On/Off Section

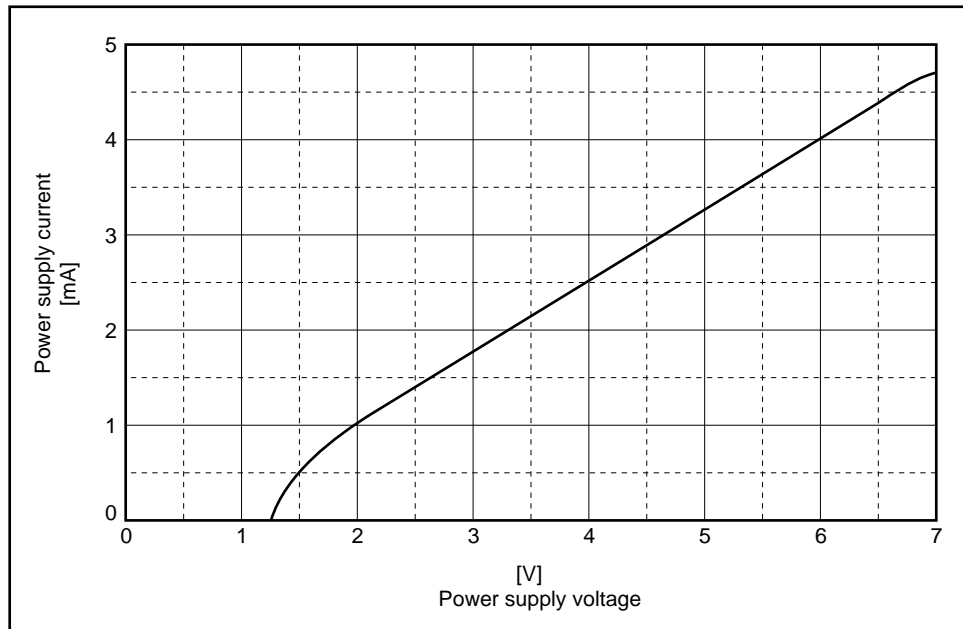
Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Power-on input voltage	V _{ON}	Power-on at V _{ON} or above, V _{CC} or below		1.5	2.4	V
Power-off input voltage	V _{OF}	Power-off at V _{OF} or below, GND or above	0.6	1.2		V
Power-on input current	I _{ON}	V _{PO} = 3 V		40	60	μA

4. CHARACTERISTIC DIAGRAMS

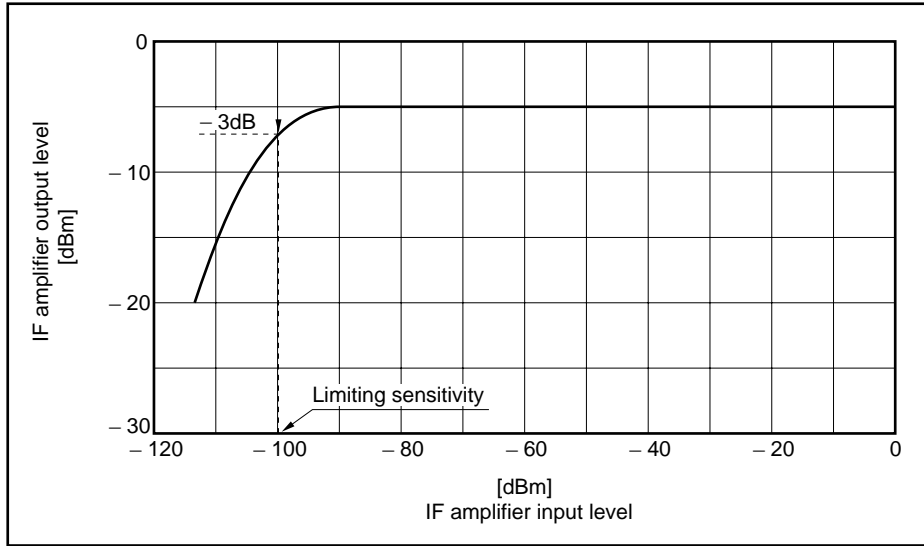
(1) Power supply current vs power supply voltage (IF amplifier section)



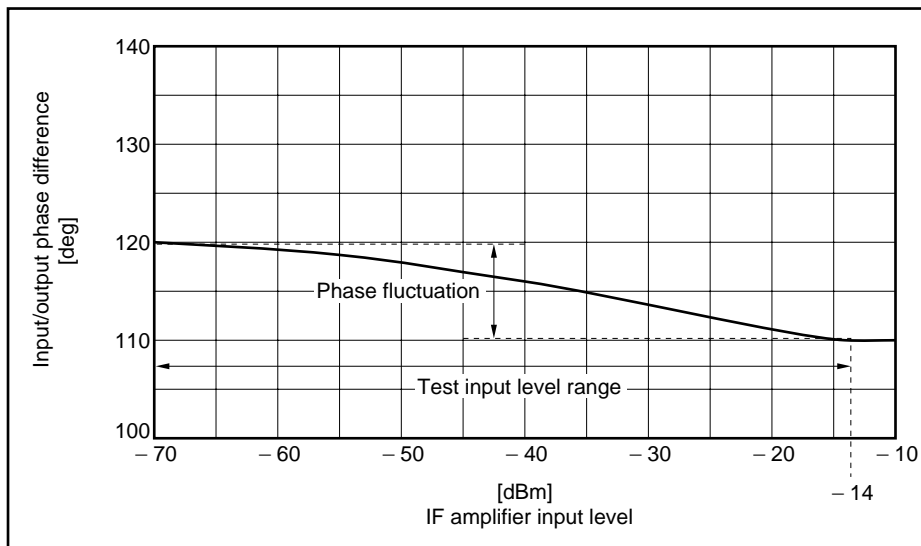
(2) Power supply current vs power supply voltage (Mixer section)



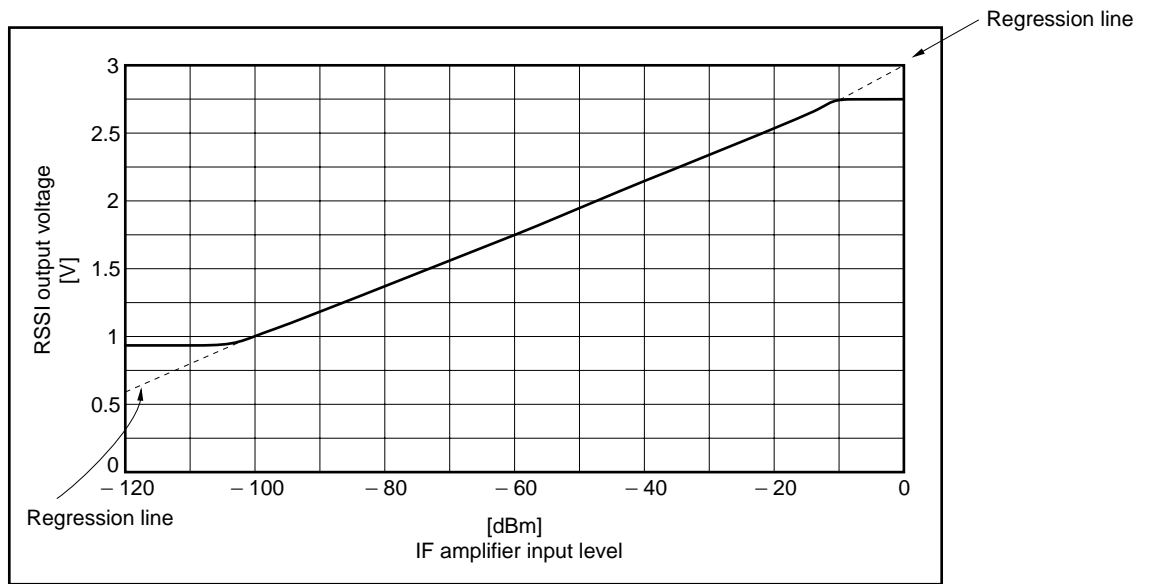
(3) IF amplifier output level vs IF amplifier input level



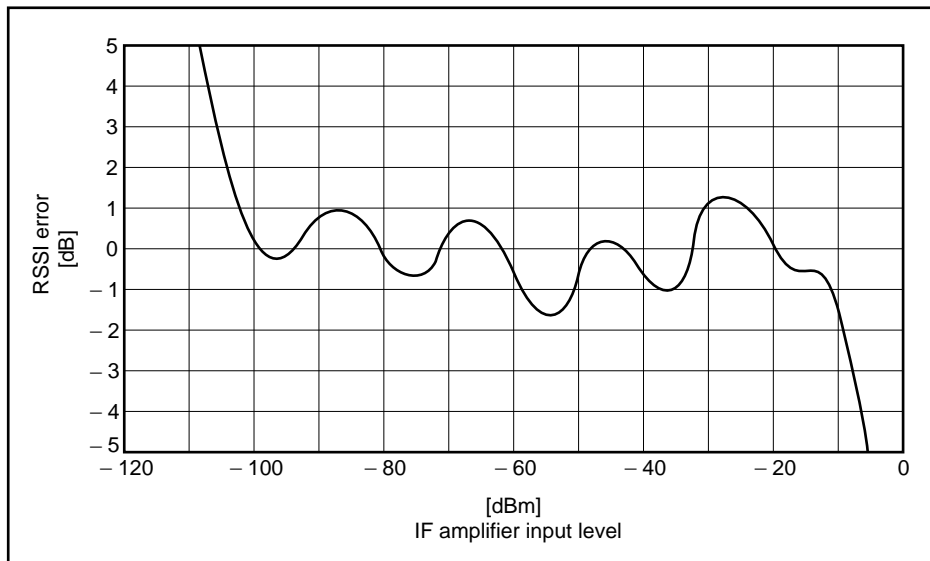
(4) IF amplifier output phase vs IF amplifier input level



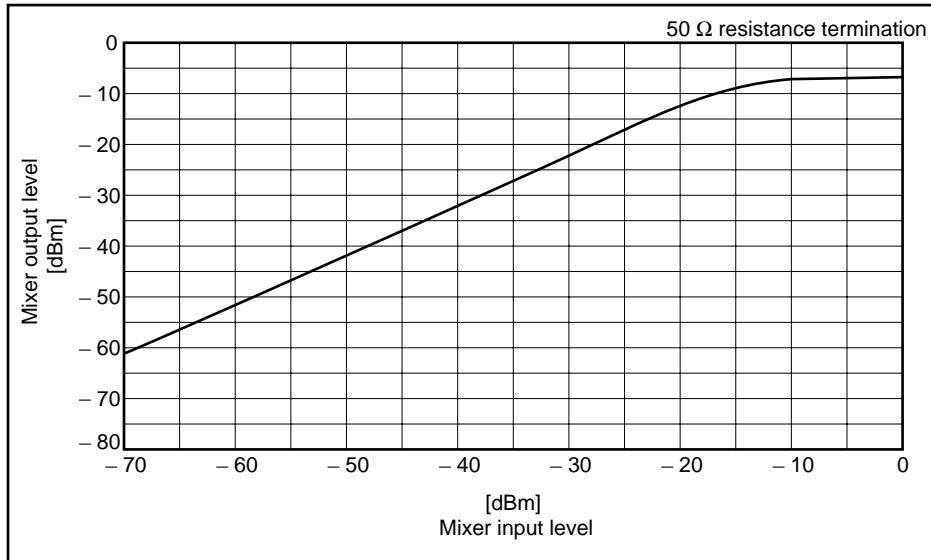
(5) RSSI characteristics (a)



(6) RSSI characteristics (b)

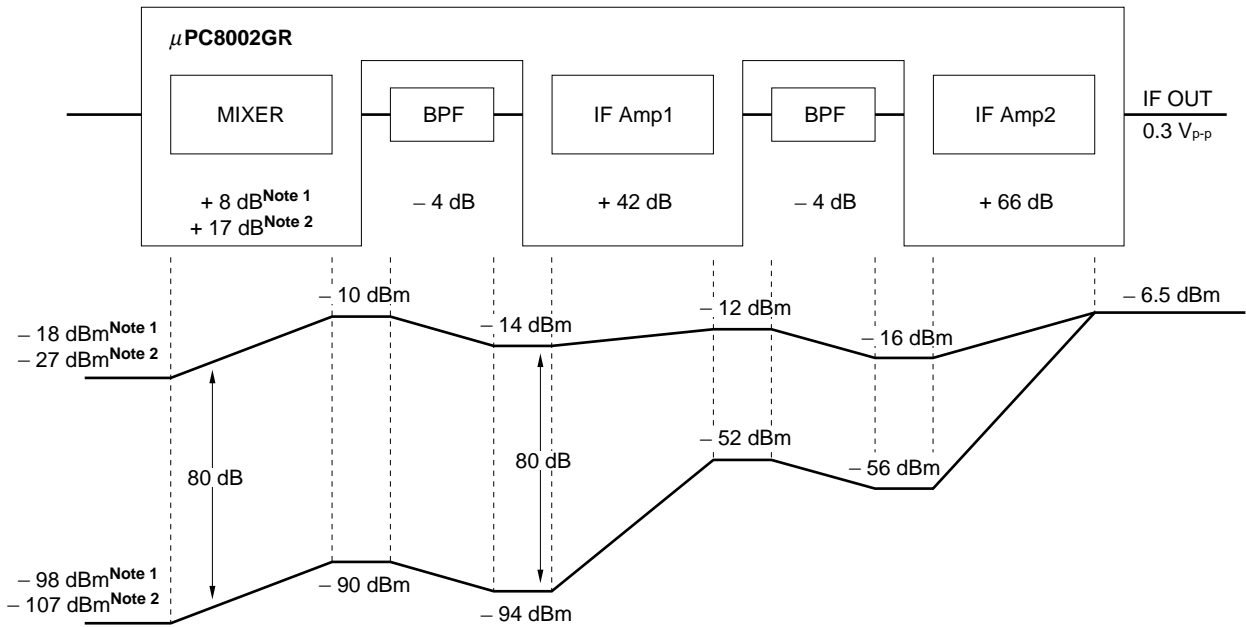


(7) Mixer output level vs mixer input level

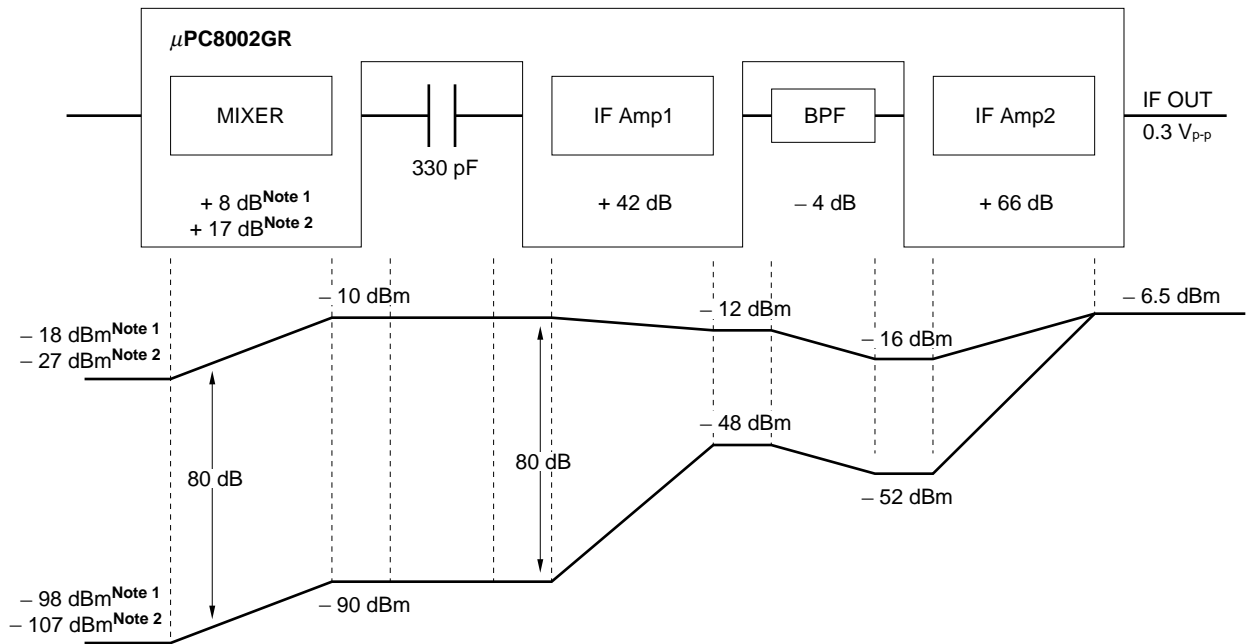


5. LEVEL DIAGRAMS

(1) For Application Circuit 1



(2) For Application Circuit 2

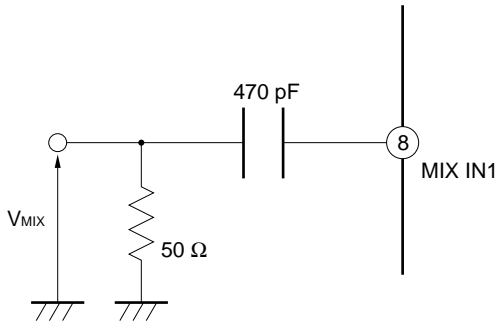


- Notes 1. 50 Ω resistance termination
- 2. LC matching (reference value)

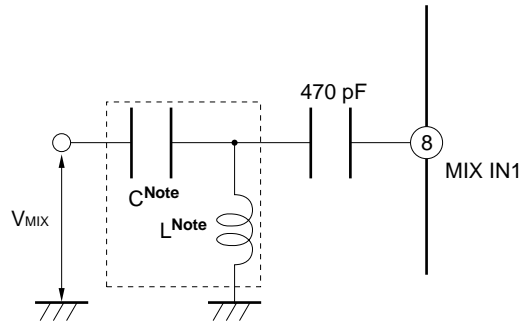
6. TEST METHODS

(1) Mixer input section

(a) With 50 Ω resistance termination

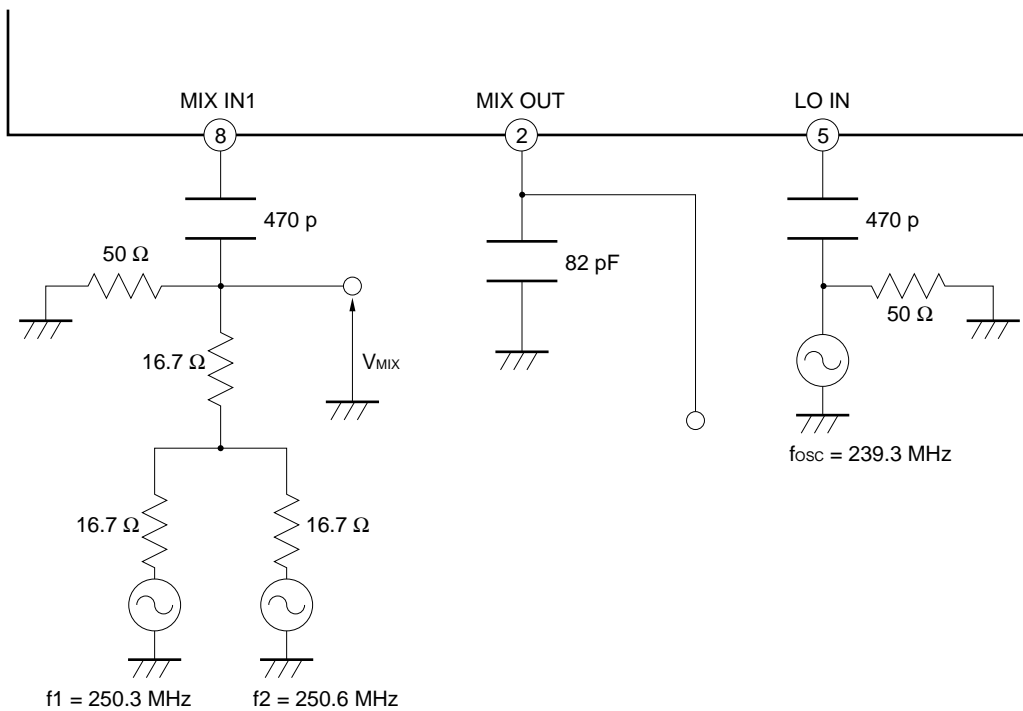


(b) With 50 Ω LC matching



Note Since the values of L and C are affected by the board's parasitic capacitance and inductance, L and C should be adjusted so that the impedance looking at the MIX IN pin side from the signal source is 50 Ω.

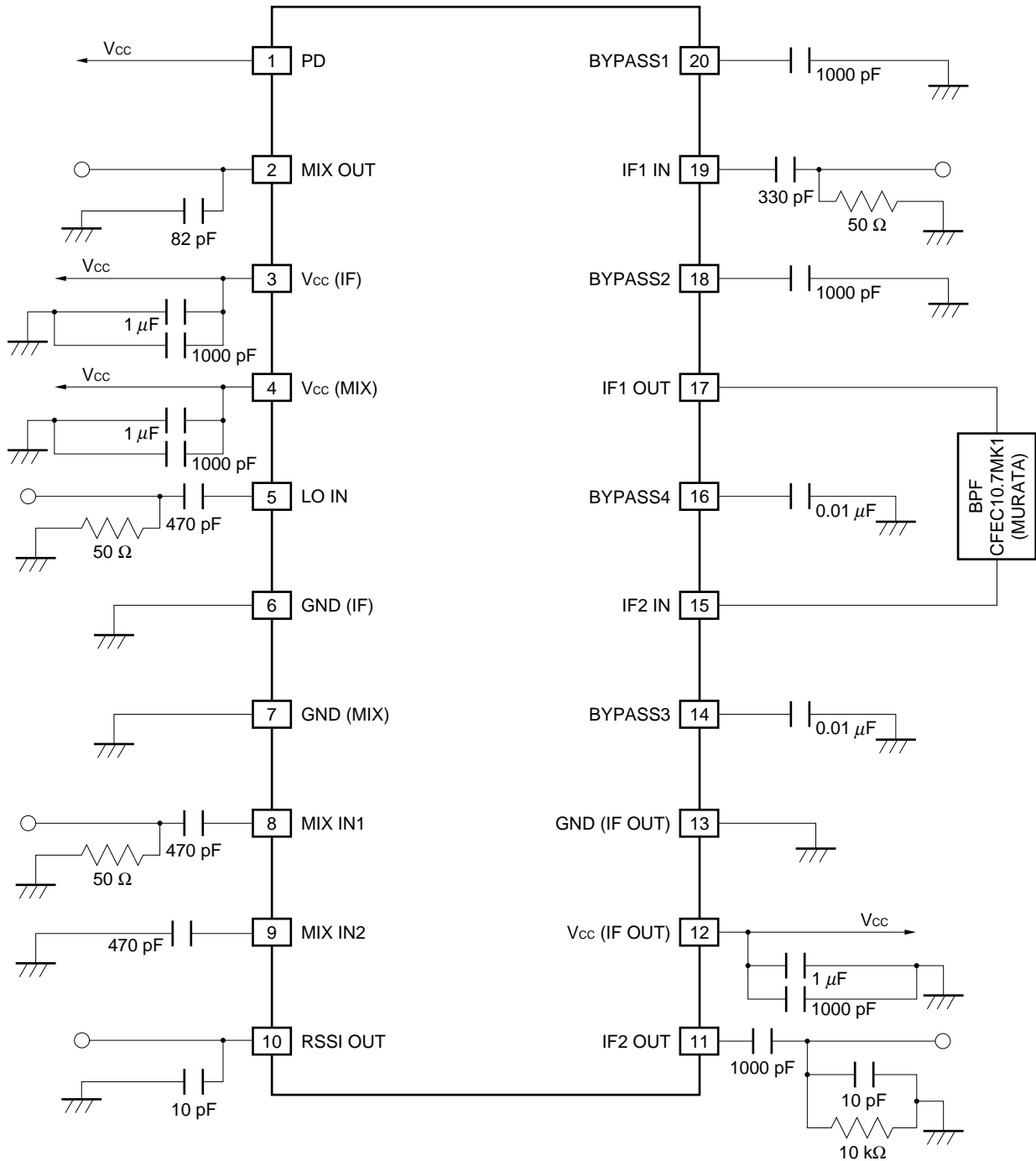
(2) Third order intercept



7. TEST CIRCUIT EXAMPLES

In test circuit example 2 onward, only the portion that differs from test circuit example 1 is shown.

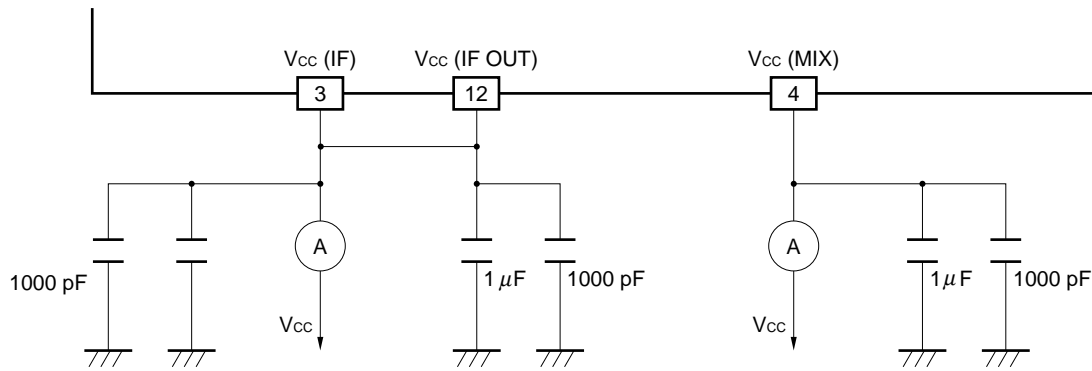
Test Circuit Example 1.



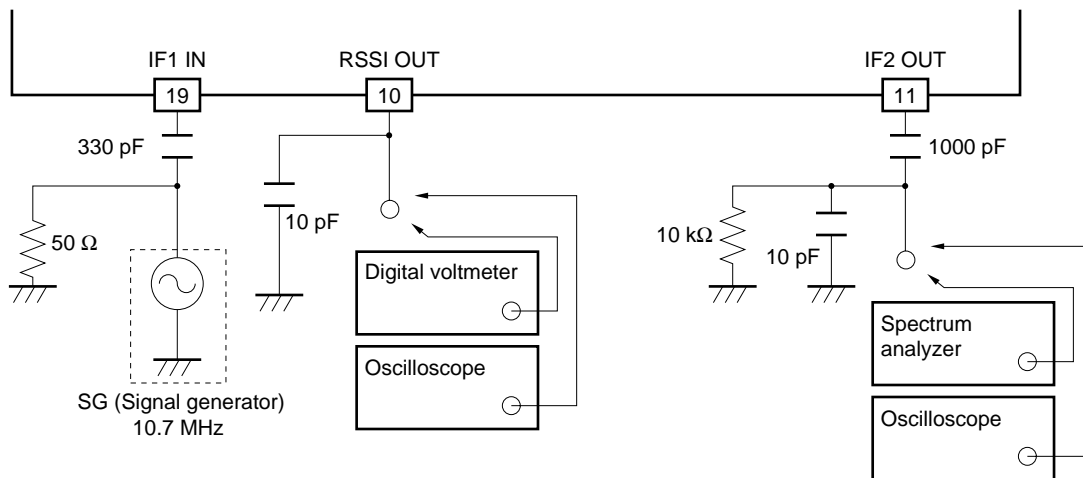
Caution The 10 pF capacitor value for IF2 OUT and RSSI OUT includes all the capacitances (board, pattern, etc.) applied to the pin. Ensure that the recommended load condition (10 pF) is not exceeded for IF2 OUT and RSSI OUT.

Remark Chip laminated ceramic capacitors (MURATA GRM36 or equivalent) should be used.

Test Circuit Example 2. (Power supply current, power-off power supply current)

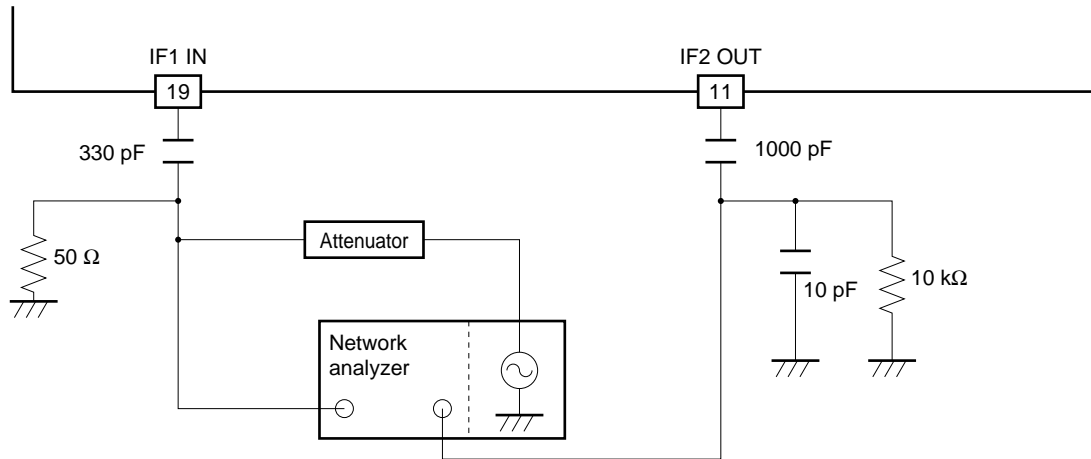


Test Circuit Example 3. (Limiting sensitivity, IF amplifier output amplitude, IF amplifier output amplitude rise time, IF amplifier output amplitude fall time, RSSI linearity, RSSI slope, RSSI intercept, RSSI output voltage, RSSI temperature stability, RSSI output ripple)



Caution The 10 pF capacitor value for IF2 OUT and RSSI OUT includes all the capacitances (board, pattern, etc.) applied to the pin. Ensure that the recommended load condition (10 pF) is not exceeded for IF2 OUT and RSSI OUT.

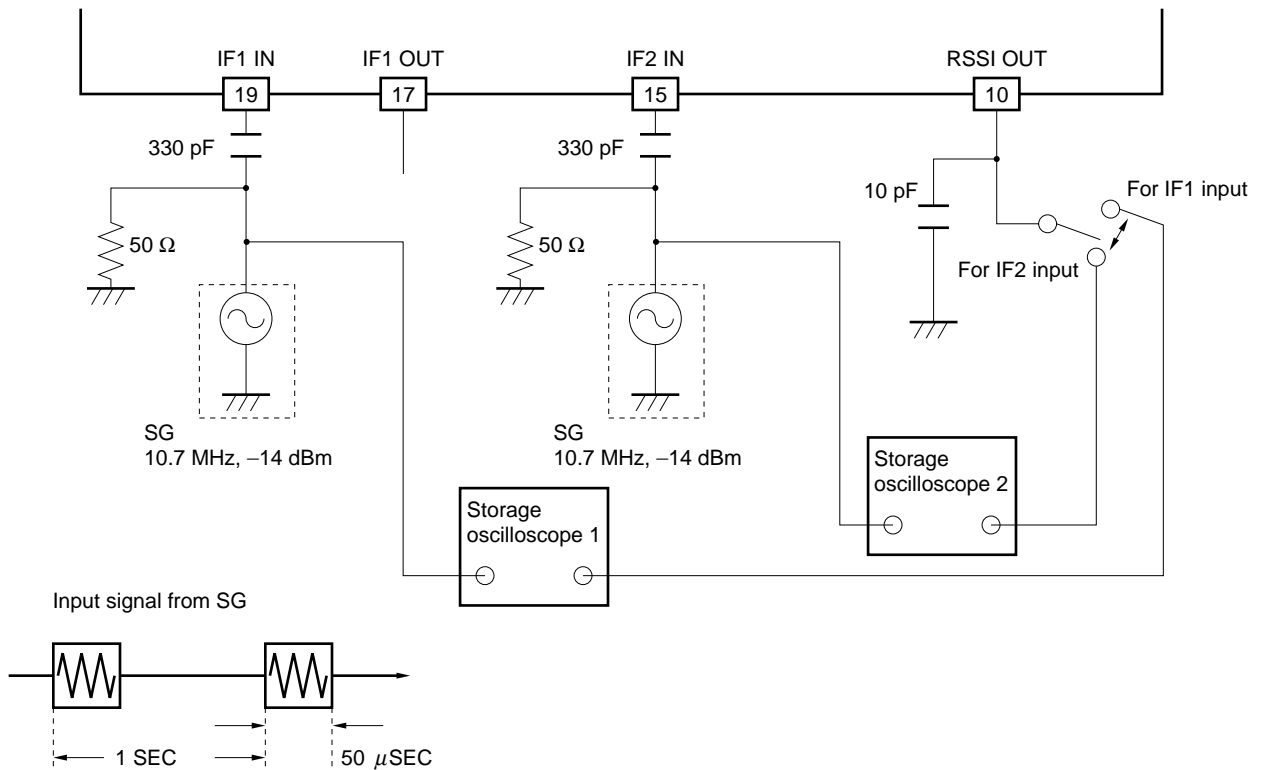
Test Circuit Example 4. (IF amplifier phase fluctuation)



Caution The 10 pF capacitor value for IF2 OUT includes all the capacitance (board, pattern, etc.) applied to the pin. Ensure that the recommended load condition (10 pF) is not exceeded.

Test Circuit Example 5. (RSSI rise time, RSSI fall time)

... Time until RSSI output is within ±10 % of the final value)

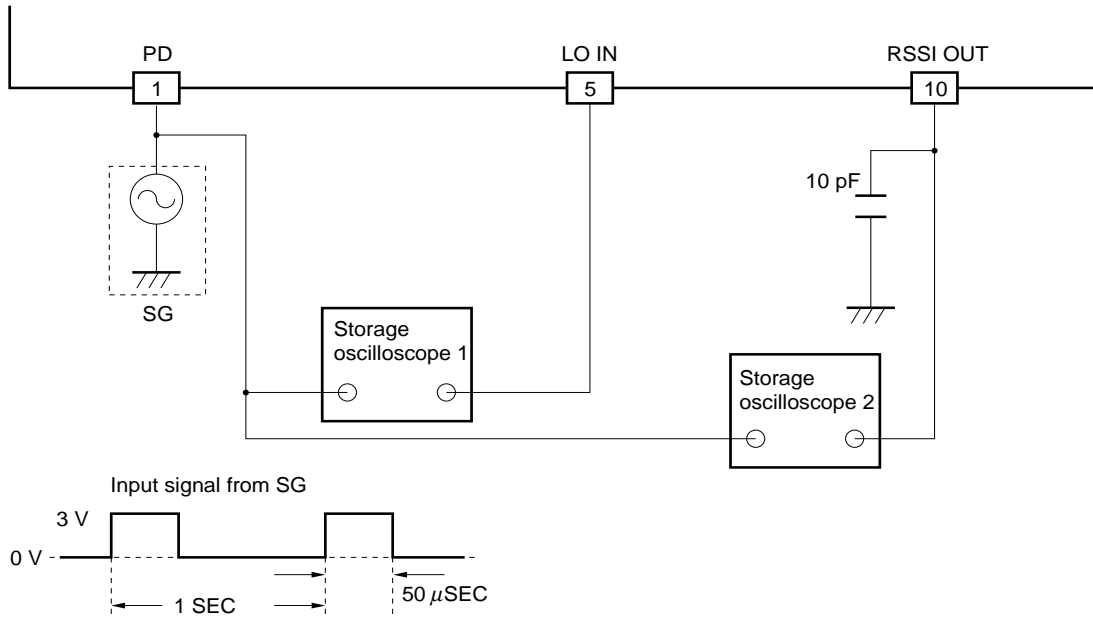


Caution The 10 pF capacitor value for RSSI OUT includes all the capacitances (board, pattern, etc) applied to the pin.

Test Circuit Example 6. (Power-on rise time)

Mixer section : Time until the difference between the local input pin power-on and power-off voltage reaches 90 %

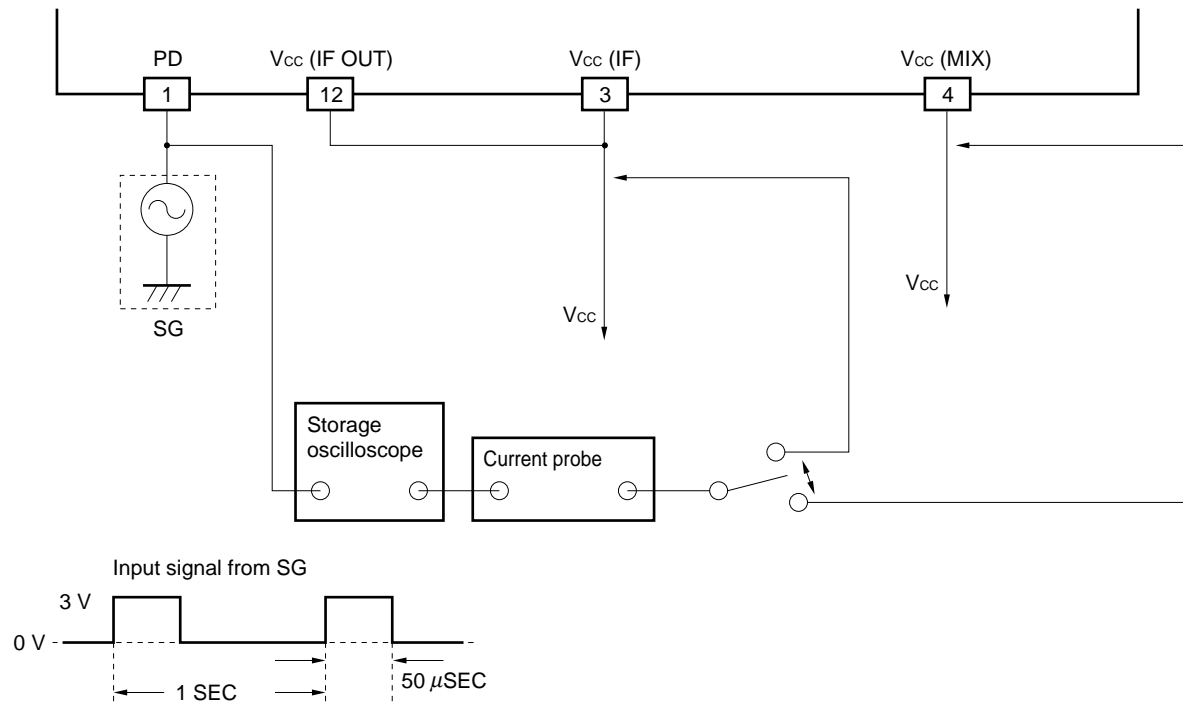
IF section : Time until RSSI output is within ±10 % of the power-on value.



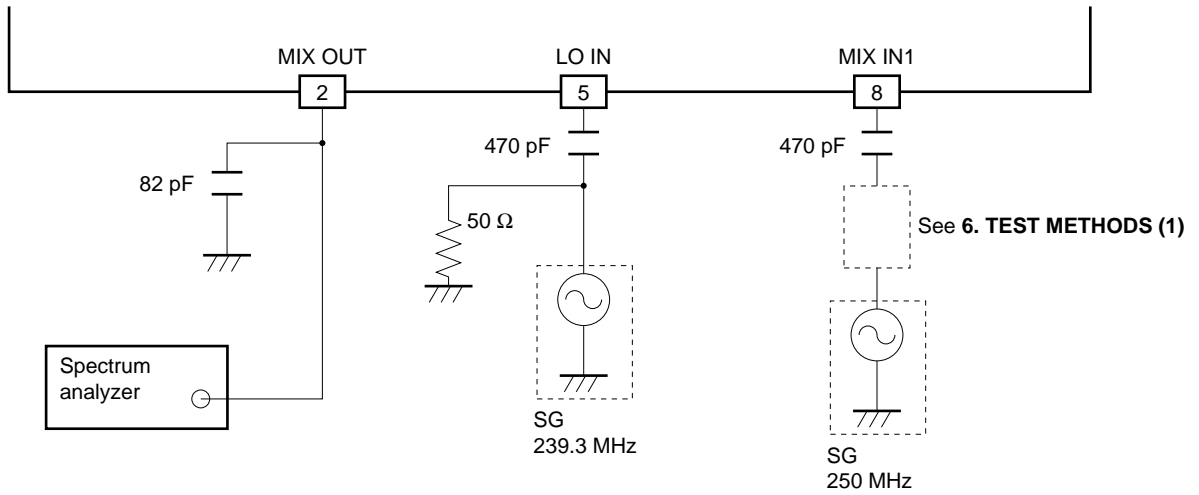
Remark Power-on input voltage (V_{PO}) rise time: 10 ns

Caution The 10 pF capacitor value for RSSI OUT includes all the capacitances (board, pattern, etc.) applied to the pin. Ensure that the recommended load condition (10 pF) is not exceeded.

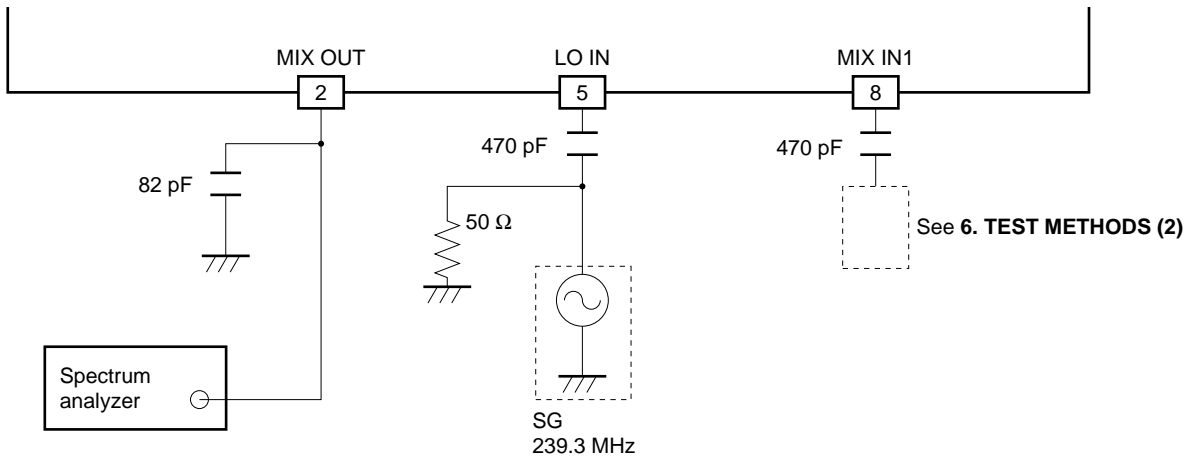
Test Circuit Example 7. (Power-off fall time)



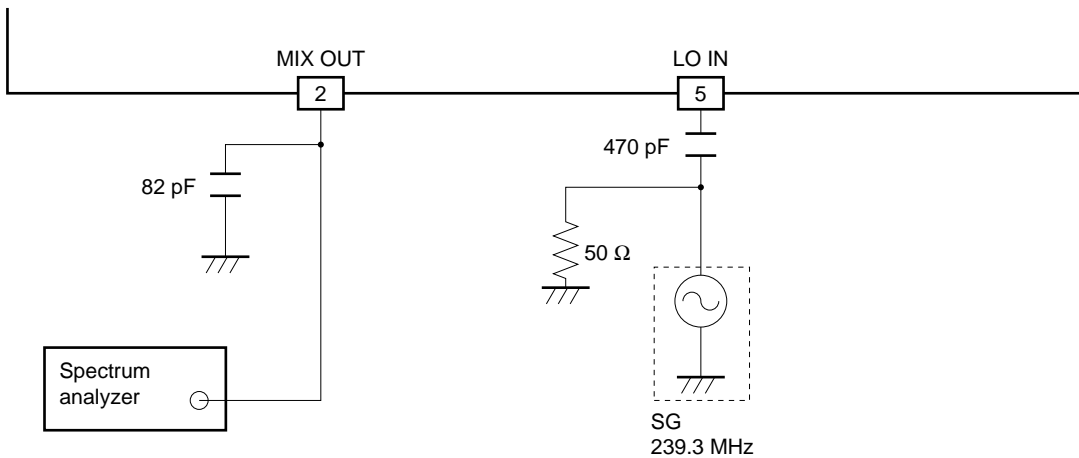
Test Circuit Example 8. (Conversion gain, -1 dB compression level)



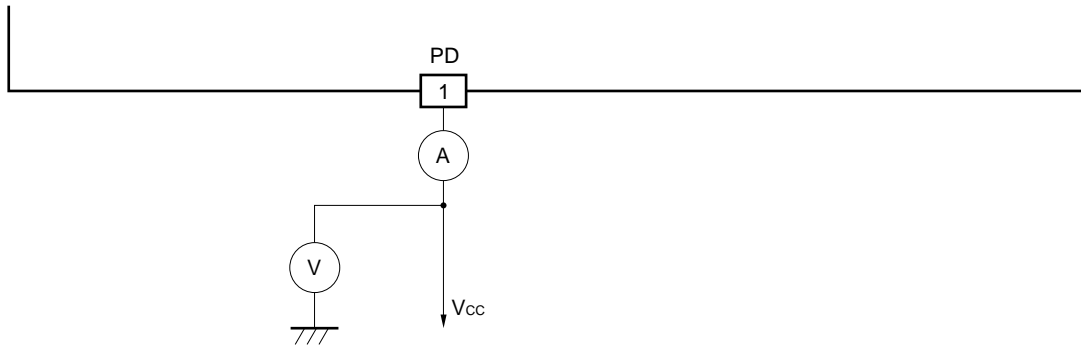
Test Circuit Example 9. (Third order intercept output level)



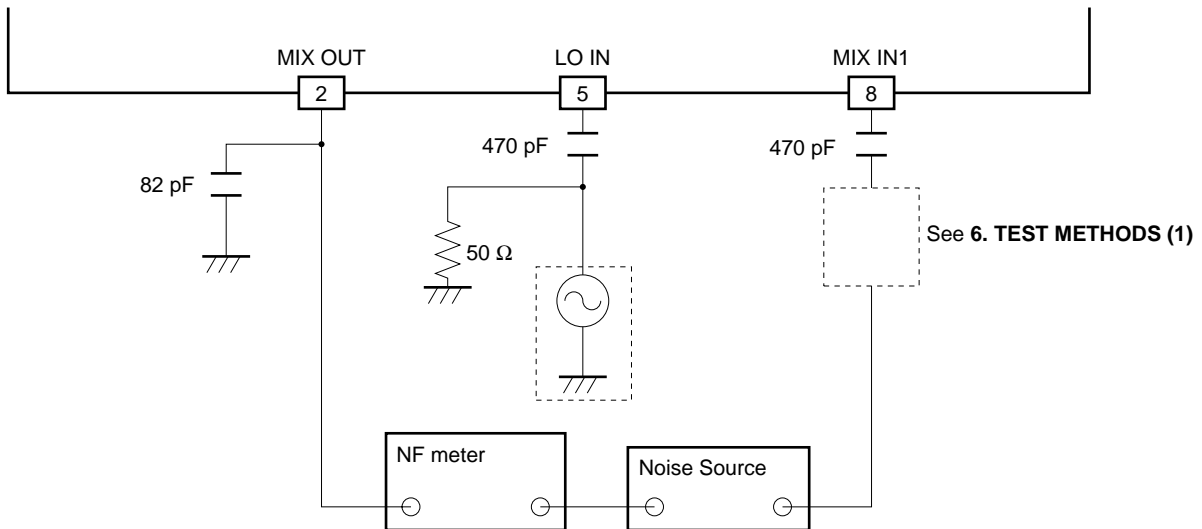
Test Circuit Example 10. (Local separation)



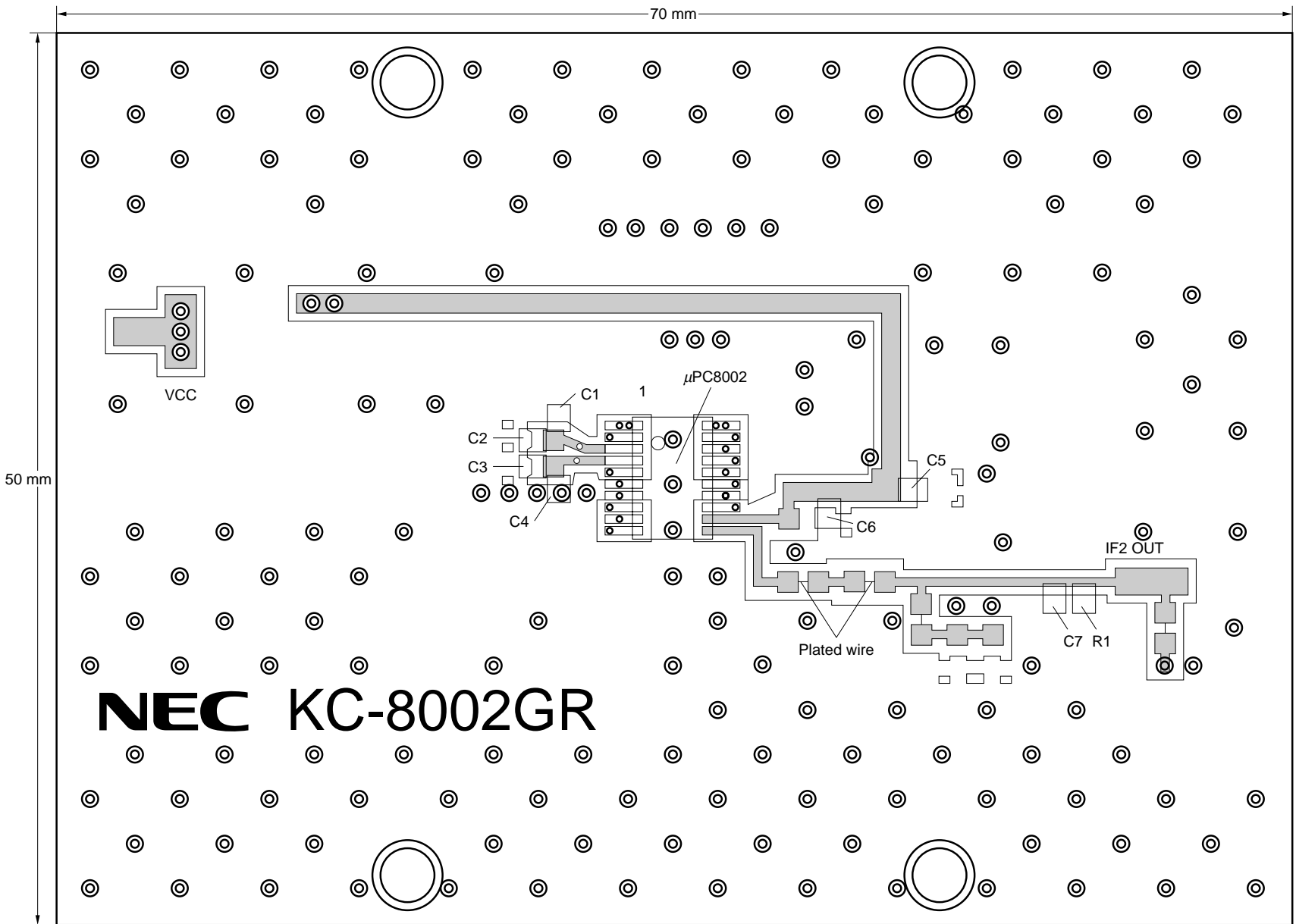
Test Circuit Example 11. (Power-on input voltage, power-off input voltage, power-on input current)



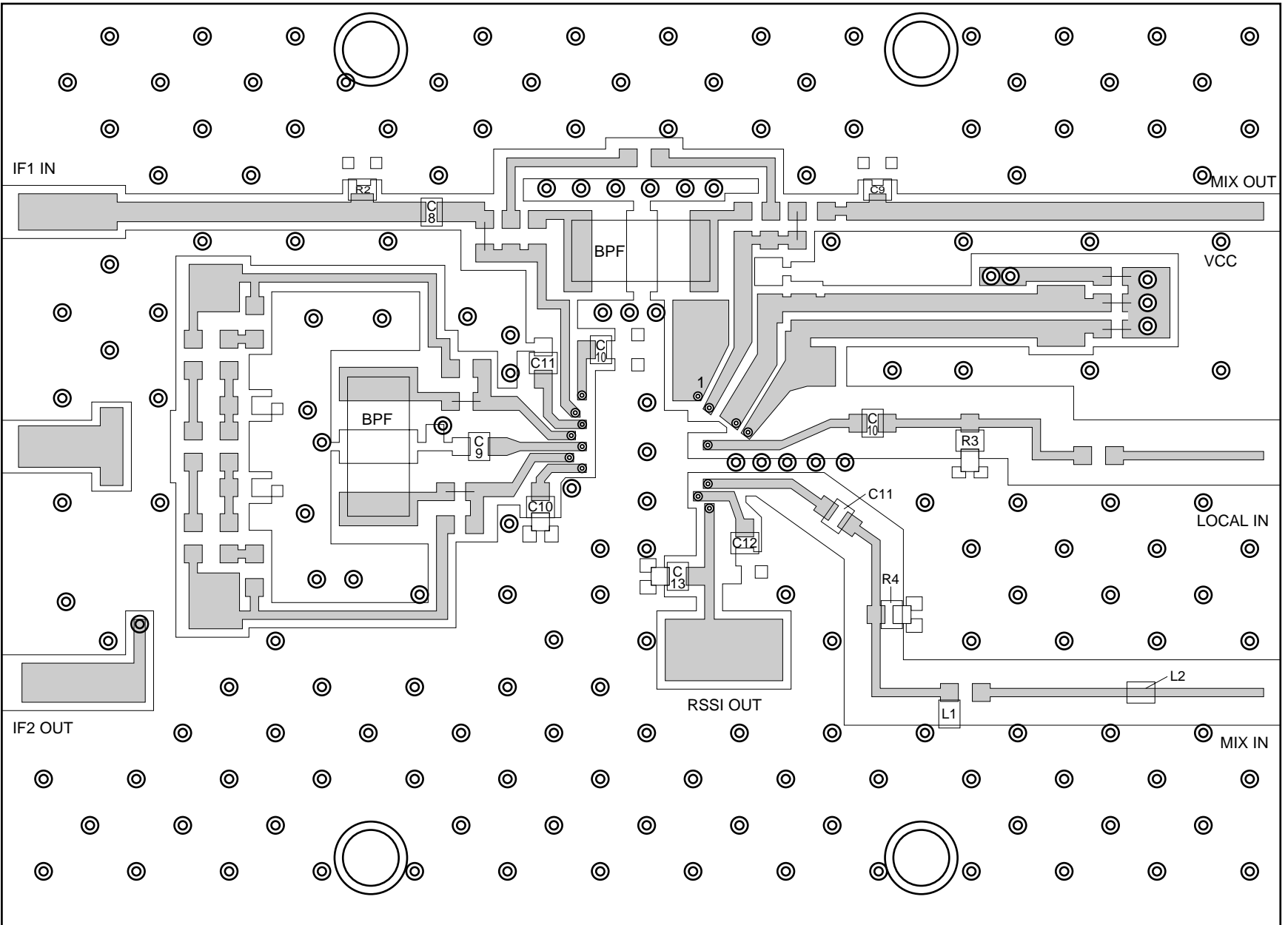
Test Circuit Example 12. (Noise factor)



8. EVALUATION BOARD MOUNTING EXAMPLE



Remark ◎ indicates a through-hole.



Remark ◎ indicates a through-hole.

C1	: 1 μ F	R1	: 10 k Ω
C2	: 1000 pF	R2	: 50 Ω
C3	: 1000 pF	R3	: 50 Ω
C4	: 1 μ F	R4	: 50 Ω
C5	: 1 μ F	L1	: 58 nH (reference value)
C6	: 1000 pF	L2	: 10 nH (reference value)
C7	: 10 pF ^{Note}		
C8	: 330 pF		
C9	: 0.01 μ F		
C10	: 0.01 μ F		
C11	: 470 pF		
C12	: 470 pF		
C13	: 10 pF ^{Note}		

Note For the IF2 OUT and RSSI OUT capacitance values, see **9. WIRING PATTERN CAPACITANCE DIAGRAM (REFERENCE)**.

- Remarks**
1. Both L in the case of LC matching and R in the case of 50 Ω termination are connected to MIX IN. Remove **R4** in the case of LC matching, and **L1** and **L2** in the case of 50 Ω termination.
 2. Change the location of the plated wires according to the evaluation items.
 3. Cut the wiring pattern to connect **L2**.

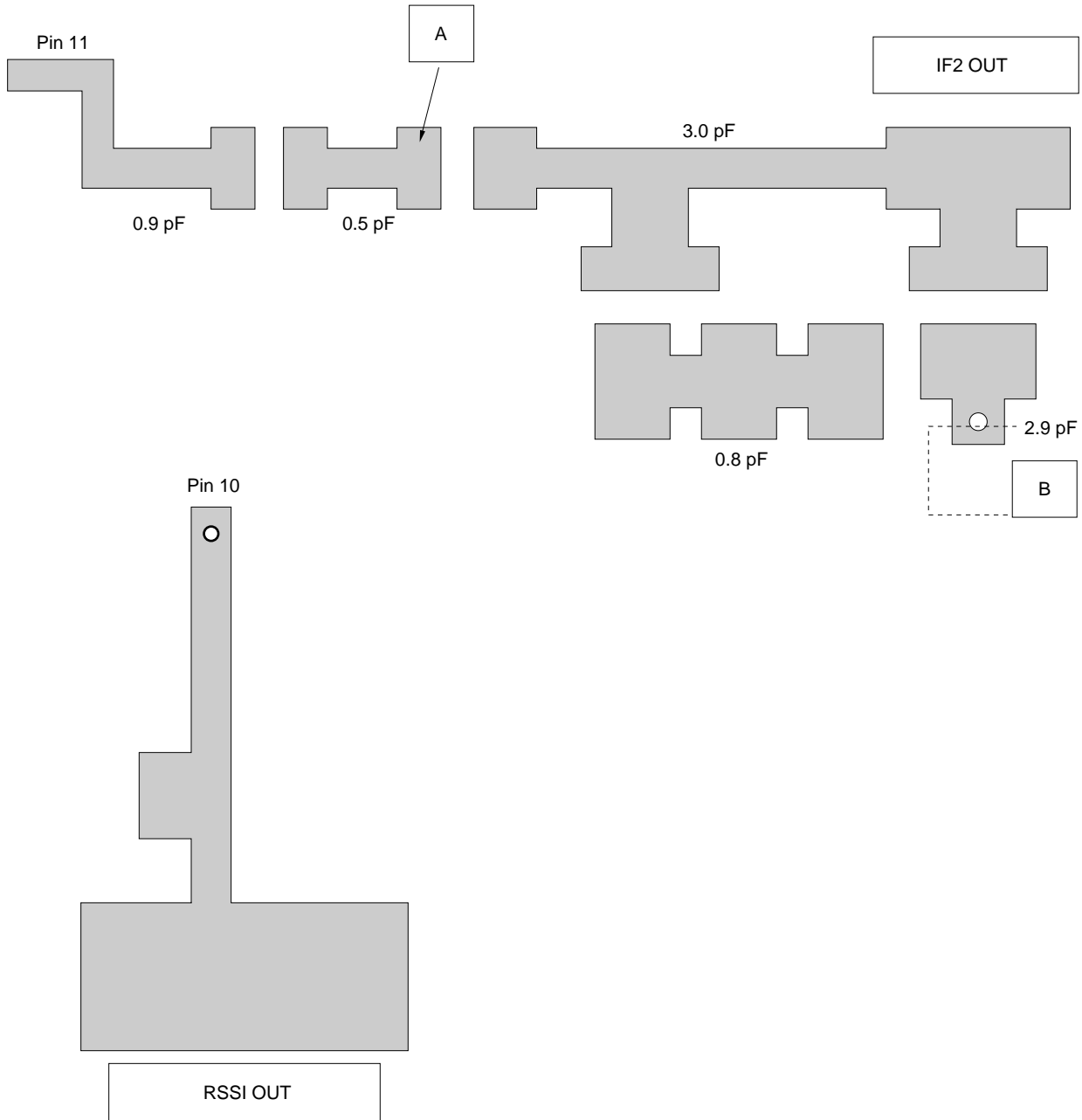
9. WIRING PATTERN CAPACITANCE DIAGRAM (REFERENCE)

The wiring pattern capacitances to ground are shown here.

For pin 11, the capacitance is 8.1 pF when the entire pattern (from pin 11 to point B) is used. In this case, the usable probe input capacitance is 1.9 pF (MAX.).

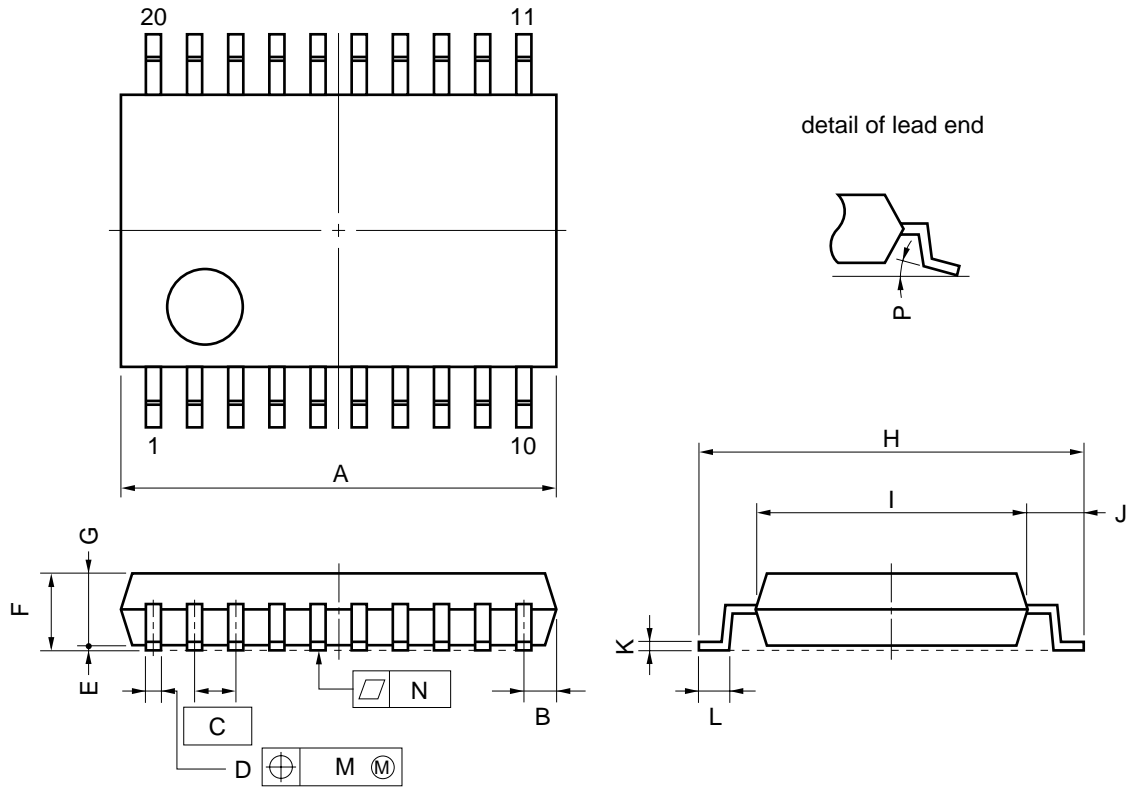
From pin 11 up to point A, the capacitance is 1.4 pF, and therefore an 8.6 pF (MAX.) probe can be used.

For pin 10, the capacitance is 4 pF when the entire pattern is used.



10. PACKAGE DRAWINGS

20 PIN PLASTIC SHRINK SOP (225mil)



NOTE
Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	7.00 MAX.	0.276 MAX.
B	0.575 MAX.	0.023 MAX.
C	0.65 (T.P.)	0.026 (T.P.)
D	0.22 ^{+0.10} _{-0.05}	0.009 ^{+0.004} _{-0.003}
E	0.1±0.1	0.004±0.004
F	1.45 MAX.	0.057 MAX.
G	1.15±0.1	0.045 ^{+0.005} _{-0.004}
H	6.4±0.2	0.252±0.008
I	4.4±0.1	0.173 ^{+0.005} _{-0.004}
J	1.0±0.2	0.039 ^{+0.009} _{-0.008}
K	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.002}
L	0.5±0.2	0.020 ^{+0.008} _{-0.009}
M	0.10	0.004
N	0.10	0.004
P	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}

P20GR-65-225C-1

11. RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

For more details, refer to our document "**SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL**" (C10535E).

Please consult with our sales offices in case other soldering process or condition is used.

TYPE OF SURFACE MOUNT DEVICE

μPC8002GR

Soldering process	Soldering conditions	Symbol
Infrared Ray Reflow	Peak package's surface temperature: 235 °C or below. Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes : MAX.2 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards)	IR35-107-2
VPS	Peak package's temperature: 215 °C or below. Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes : MAX. 2 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards)	VP15-107-2
Partial heating method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (Per side of pin position)	—

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions : 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for " Partial heating method".

[MEMO]

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

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Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.