

BIPOLAR ANALOG INTEGRATED CIRCUITS

μ PC8128TA, μ PC8151TA, μ PC8152TA

SILICON MMIC LOW CURRENT AMPLIFIERS FOR CELLULAR/CORDLESS TELEPHONES

DESCRIPTION

The μ PC8128TA, μ PC8151TA and μ PC8152TA are silicon monolithic integrated circuits designed as buffer amplifiers for cellular / cordless telephones. These amplifiers can realize low current consumption with external chip inductor (example: 1005 size) which can not be realized on internal 50 Ω wideband matched IC. These low current amplifiers operate on 3.0 V.

These ICs are manufactured using NEC's 20 GHz fr NESAT™ III silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, these ICs have excellent performance, uniformity and reliability.

FEATURES

- Low current consumption : μ PC8128TA ; $I_{CC} = 2.8$ mA TYP. @ $V_{CC} = 3.0$ V
 : μ PC8151TA ; $I_{CC} = 4.2$ mA TYP. @ $V_{CC} = 3.0$ V
 : μ PC8152TA ; $I_{CC} = 5.6$ mA TYP. @ $V_{CC} = 3.0$ V
- Supply voltage : $V_{CC} = 2.4$ to 3.3 V
- High efficiency : μ PC8128TA ; $P_{O(1\text{ dB})} = -4.0$ dBm TYP. @ $f = 1$ GHz
 : μ PC8151TA ; $P_{O(1\text{ dB})} = +2.5$ dBm TYP. @ $f = 1$ GHz
 : μ PC8152TA ; $P_{O(1\text{ dB})} = -4.5$ dBm TYP. @ $f = 1$ GHz
- Power gain variation : μ PC8128TA, 8151TA ; $G_P = 12.5$ dB TYP. @ $f = 1$ GHz
 : μ PC8152TA ; $G_P = 23.0$ dB TYP. @ $f = 1$ GHz
- Operating frequency : 100 to 1 900 MHz (Output port LC matching)
- Excellent isolation : μ PC8128TA ; ISL = 39 dB TYP. @ $f = 1$ GHz
 : μ PC8151TA ; ISL = 38 dB TYP. @ $f = 1$ GHz
 : μ PC8152TA ; ISL = 40 dB TYP. @ $f = 1$ GHz

APPLICATION

- Buffer Amplifiers on 800 to 1 900 MHz cellular / cordless telephones

Caution Electro-static sensitive devices

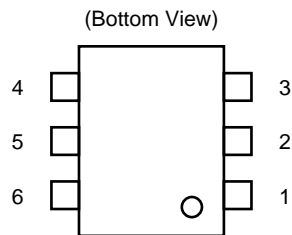
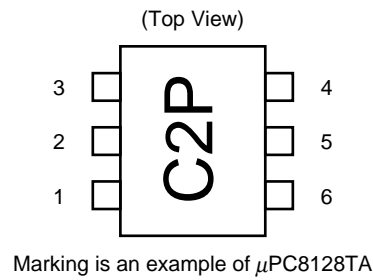
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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

ORDERING INFORMATION

Part Number	Package	Marking	Feature	Supplying Form
μ PC8128TA-E3	6-pin minimold	C2P	2.8 mA Low I _{CC}	Embossed tape 8 mm wide. 1, 2, 3 pins face the perforation side of the tape. Qty 3 kpcs/reel.
μ PC8151TA-E3		C2U	4 mA High P _O	
μ PC8152TA-E3		C2V	5 mA High G _P	

Remark To order evaluation samples, please contact your local NEC sales office.
(Part number for sample order: μ PC8128TA, μ PC8151TA, μ PC8152TA)

PIN CONNECTIONS



Pin No.	Pin Name
1	INPUT
2	GND
3	GND
4	OUTPUT
5	GND
6	V _{CC}

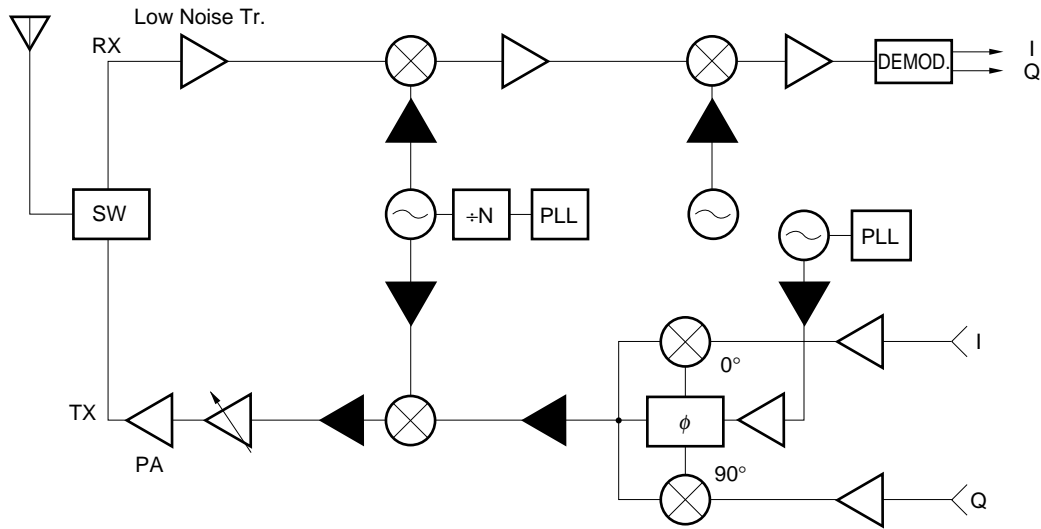
PRODUCT LINE-UP ($T_A = +25\text{ }^\circ\text{C}$, $V_{CC} = V_{out} = 3.0\text{ V}$, $Z_S = Z_L = 50\ \Omega$)

Parameter Part No.	I _{cc} (mA)	1.00 GHz output port matching frequency			1.66 GHz output port matching frequency			1.90 GHz output port matching frequency			Package	Marking
		G _P (dB)	ISL (dB)	P _O (1 dB) (dB)	G _P (dB)	ISL (dB)	P _O (1 dB) (dB)	G _P (dB)	ISL (dB)	P _O (1 dB) (dB)		
μ PC8128TA	2.8	12.5	39	-4.0	13	39	-4.0	13	37	-4.0	6-pin minimold	C2P
μ PC8128TB											6-pin super minimold	
μ PC8151TA	4.2	12.5	38	+2.5	15	36	+1.5	15	34	+0.5	6-pin minimold	C2U
μ PC8151TB											6-pin super minimold	
μ PC8152TA	5.6	23	40	-4.5	19.5	36	-8.5	17.5	35	-8.5	6-pin minimold	C2V
μ PC8152TB											6-pin super minimold	

Remark Typical performance. Please refer to ELECTRICAL CHARACTERISTICS in detail.

SYSTEM APPLICATION EXAMPLE

Location examples in digital cellular



These ICs can be added to your system around ▲ parts, when you need more isolation or gain. The application herein, however, shows only examples, therefore the application can depend on your kit evaluation.

PIN EXPLANATION

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V) ^{Note}	Function and Applications	Internal Equivalent Circuit
1	INPUT	–	0.9 ----- 1.06 ----- 0.80	Signal input pin. A internal matching circuit, configured with resistors, enables 50 Ω connection over a wide band. This pin must be coupled to signal source with capacitor for DC cut.	<p>μPC8128TA, μPC8151TA</p>
2 3 5	GND	0	–	Ground pin. This pin should be connected to system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. All the ground pins must be connected together with wide ground pattern to decrease impedance difference.	<p>μPC8152TA</p>
4	OUTPUT	voltage as same as V_{cc} through external inductor	–	Signal output pin. This pin is designed as collector output. Due to the high impedance output, this pin should be externally equipped with LC matching circuit to next stage. For L, a size 1005 chip in-ductor can be chosen.	
6	V_{cc}	2.4 to 3.3	–	Power supply pin. This pin should be externally equipped with bypass capacitor to minimize its impedance.	

Note Pin voltage is measured at $V_{cc} = 3.0$ V. Above: μ PC8128TA, Center: μ PC8151TA, Below: μ PC8152TA

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V _{CC}	T _A = +25 °C, Pin 4, Pin 6	3.6	V
Total Circuit Current	I _{CC}	T _A = +25 °C	15	mA
Total Power Dissipation	P _D	Mounted on double sided copper clad 50 × 50 × 1.6 mm epoxy glass PWB (T _A = +85 °C)	280	mW
Operating Ambient Temperature	T _A		-40 to +85	°C
Storage Temperature	T _{stg}		-55 to +150	°C
Input Power	P _{in}	T _A = +25 °C	+5	dBm

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Supply Voltage	V _{CC}	2.4	3.0	3.3	V	The same voltage should be applied to pin 4 and pin 6.
Operating Ambient Temperature	T _A	-40	+25	+85	°C	
Operating Frequency	f	0.1	-	1.9	GHz	Matched output port with external LC

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $T_A = +25\text{ }^\circ\text{C}$, $V_{CC} = V_{out} = 3.0\text{ V}$, $Z_s = Z_L = 50\ \Omega$, at LC matched frequency)

Parameter	Symbol	Test Conditions	μ PC8128TA			μ PC8151TA			μ PC8152TA			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Circuit Current	I_{CC}	No signal	1.8	2.8	3.8	2.8	4.2	5.8	4.2	5.6	7.1	mA
Power Gain	G_P	f = 1.00 GHz	9.5	12.5	14.5	9.5	12.5	14.5	20	23	25	dB
		f = 1.66 GHz	10	13	15	12	15	17	16.5	19.5	21.5	
		f = 1.90 GHz	10	13	15	12	15	17	14.5	17.5	19.5	
Isolation	ISL	f = 1.00 GHz	34	39	–	33	38	–	35	40	–	dB
		f = 1.66 GHz	34	39	–	31	36	–	33	38	–	
		f = 1.90 GHz	32	37	–	29	34	–	30	35	–	
Gain 1 dB Compression Output Power	$P_{O(1\text{ dB})}$	f = 1.00 GHz	–7.5	–4.0	–	–1.0	+2.5	–	–7.5	–4.5	–	dBm
		f = 1.66 GHz	–8.5	–4.0	–	–2.5	+1.5	–	–11.5	–8.5	–	
		f = 1.90 GHz	–8.5	–4.0	–	–3.0	+0.5	–	–11.5	–8.5	–	
Saturated Output Power ^{Note} ($P_{in} = -6\text{ dBm}$)	$P_{O(sat)}$	f = 1.00 GHz	–	–	–	–	–	–	–2.5	+0.5	–	dBm
		f = 1.66 GHz	–	–	–	–	–	–	–5.5	–2.5	–	
		f = 1.90 GHz	–	–	–	–	–	–	–6.0	–3.0	–	
Noise Figure	NF	f = 1.00 GHz	–	6.0	7.5	–	6.0	7.5	–	3.5	5.0	dB
		f = 1.66 GHz	–	6.0	7.5	–	6.0	7.5	–	4.0	5.5	
		f = 1.90 GHz	–	6.0	7.5	–	6.0	7.5	–	4.5	6.0	
Input Return Loss (Without matching circuit)	RL_{in}	f = 1.00 GHz	2	5	–	2	5	–	8.5	11.5	–	dB
		f = 1.66 GHz	2	5	–	1	4	–	7.5	10.5	–	
		f = 1.90 GHz	2.5	5.5	–	1	4	–	8.5	11.5	–	

Note Saturated output power is specified only in μ PC8152TA which has flat saturated region.

STANDARD CHARACTERISTICS (Unless otherwise specified, $T_A = +25\text{ }^\circ\text{C}$, $V_{CC} = V_{out} = 3.0\text{ V}$, $Z_s = Z_L = 50\ \Omega$, at LC matched frequency)

Parameter	Symbol	Conditions	Reference Value			Unit
			μ PC8128TA	μ PC8151TA	μ PC8152TA	
Output Return Loss (With external matching circuit)	RL_{out}	f = 1.00 GHz	10	10	15	dB
		f = 1.66 GHz	25	18	7.5	
		f = 1.90 GHz	14	12	7	
3rd Order Intermodulation Distortion ($P_{O(each)} = -20\text{ dBm}$)	IM_3	$f_1 = 1.000\text{ GHz}$, $f_2 = 1.001\text{ GHz}$	–50	–62	–51	dBc
		$f_1 = 1.660\text{ GHz}$, $f_2 = 1.661\text{ GHz}$	–46	–56	–43	
		$f_1 = 1.900\text{ GHz}$, $f_2 = 1.901\text{ GHz}$	–46	–54	–42	

TEST CIRCUIT

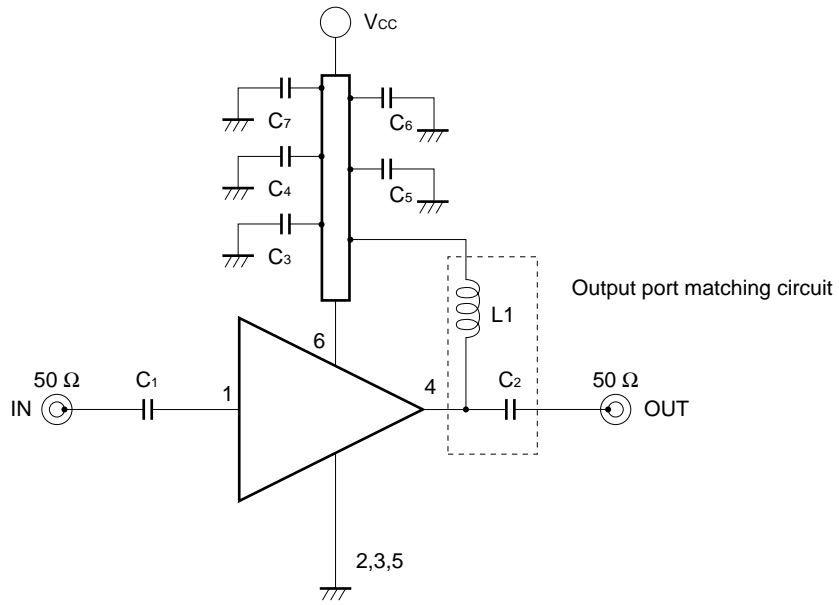
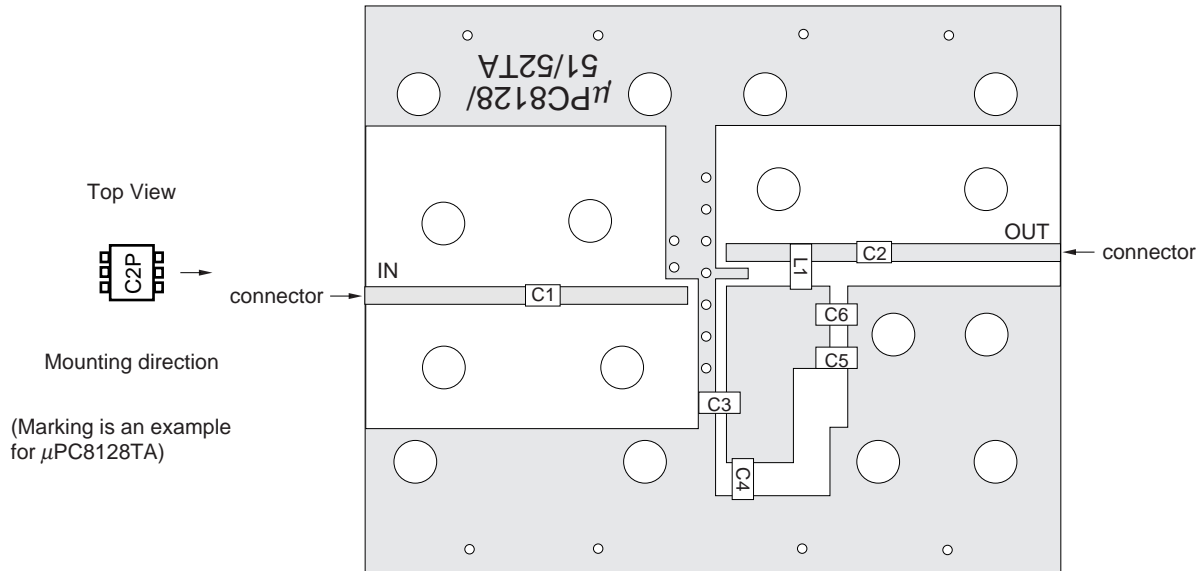


ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD

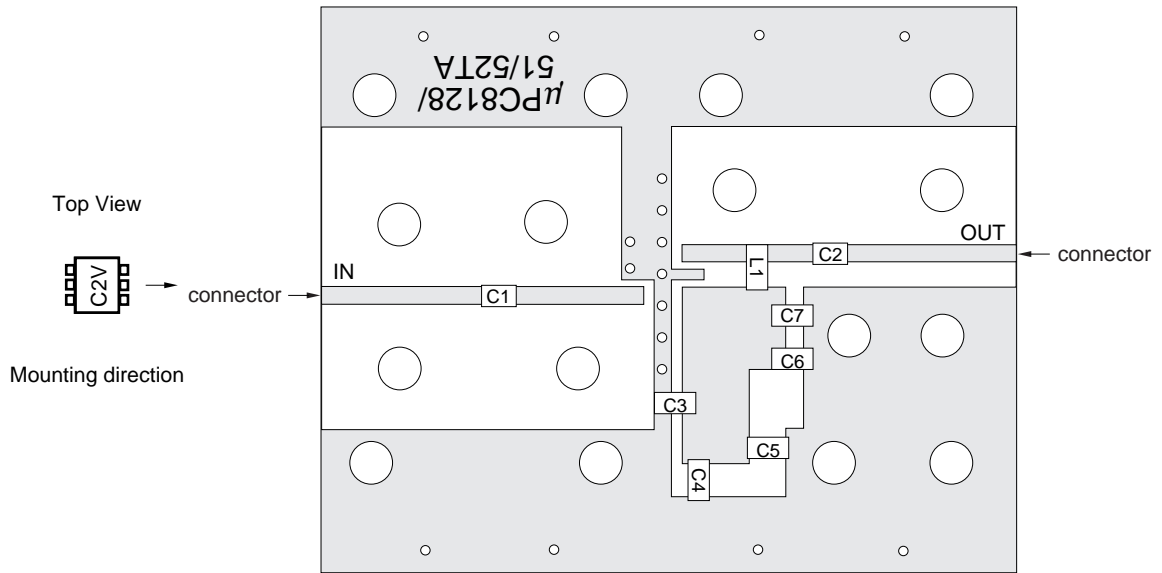
μ PC8128TA/ μ PC8151TA



COMPONENT LIST

	1.00 GHz output port matching	1.66 GHz output port matching	1.90 GHz output port matching
C1, C3 to C6	1 000 pF	1 000 pF	1 000 pF
C2	1.0 pF	0.75 pF	0.75 pF
L1	8.2 nH	3.3 nH	2.7 nH

μ PC8152TA



COMPONENT LIST

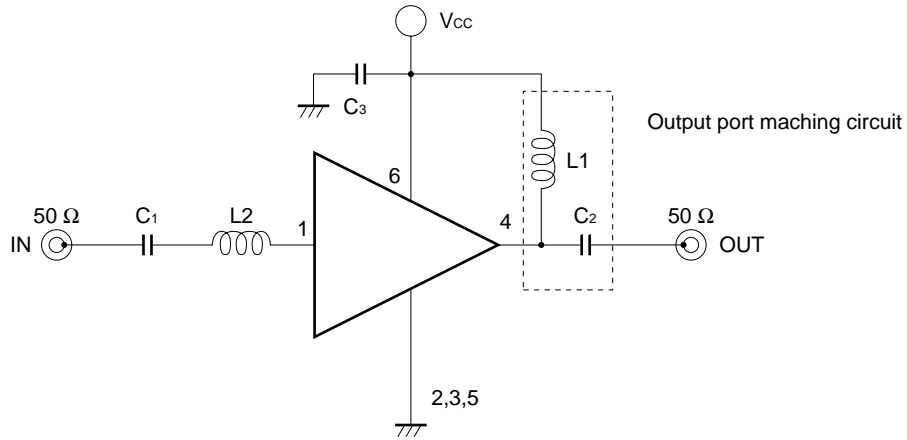
	1.00 GHz output port matching	1.66 GHz output port matching	1.90 GHz output port matching
C1, C3 to C7	1 000 pF	1 000 pF	1 000 pF
C2	1.5 pF	1.0 pF	1.5 pF
L1	8.2 nH	2.7 nH	1.8 nH

NOTES (μ PC8128TA, μ PC8151TA, μ PC8152TA in common)

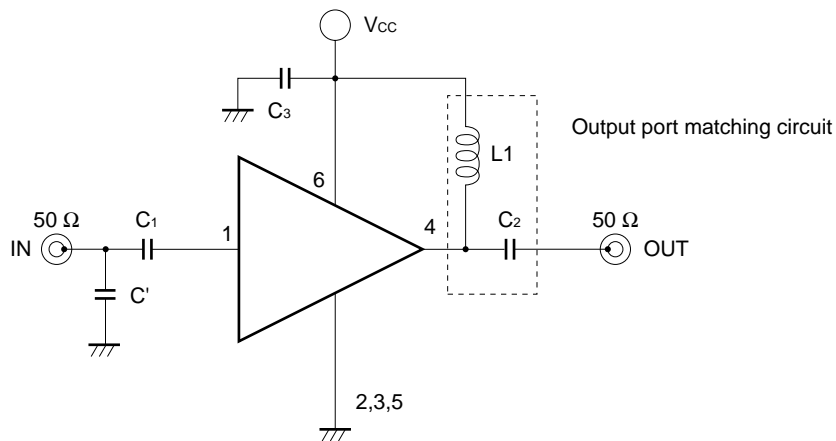
1. 42 × 35 × 0.4 mm double sided copper clad polyimide board.
2. Back side: GND pattern
3. Solder plated on pattern
4. ○ ○ ○ : Through holes

EXAMPLE OF APPLICATION CIRCUIT (μ PC8128TA, μ PC8151TA)

In improving R_{Lin} of μ PC8128TA and μ PC8151TA at 1.0 GHz, L2 should be attached.

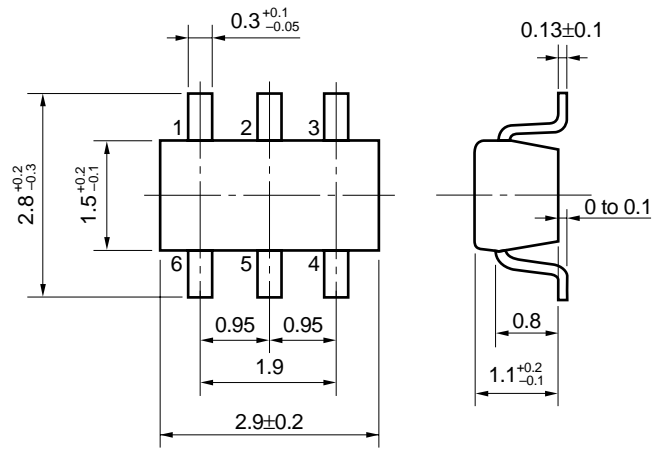


In improving R_{Lin} of μ PC8128TA and μ PC8151TA at 1.66 to 1.9 GHz, C' should be attached.



PACKAGE DIMENSIONS

6 PIN MINIMOLD (UNIT: mm)



NOTES ON CORRECT USE

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired oscillation). All the ground pins must be connected together with wide ground pattern to decrease impedance difference.
- (3) The bypass capacitor should be attached to V_{cc} line.
- (4) The inductor (L) should be attached between output and V_{cc} pins. The L and series capacitor (C2) values should be adjusted for applied frequency to match impedance to next stage.
- (5) The DC capacitor must be attached to input pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235 °C or below Time: 30 seconds or less (at 210 °C) Count: 3, Exposure limit: None ^{Note}	IR35-00-3
VPS	Package peak temperature: 215 °C or below Time: 40 seconds or less (at 200 °C) Count: 3, Exposure limit: None ^{Note}	VP15-00-3
Wave Soldering	Soldering bath temperature: 260 °C or below Time: 10 seconds or less Count: 1, Exposure limit: None ^{Note}	WS60-00-1
Partial Heating	Pin temperature: 300 °C Time: 3 seconds or less (per side of device) Exposure limit: None ^{Note}	—

Note After opening the dry pack, keep it in a place below 25 °C and 65 % RH for the allowable storage period.

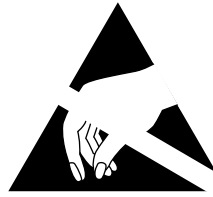
Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document **SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E)**.

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ATTENTION

OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

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