NEC

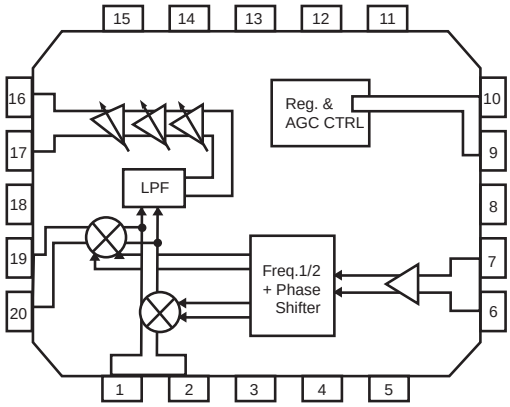
TX-IF SiMMIC FOR W-CDMA AGC + I/Q MODULATOR

UPC8195K

FEATURES

- **TX-IF:**
  380 MHz
- **LOW POWER CONSUMPTION:**
  V_{CC}= 3.0 V
- **SMALL 20 PIN QFN PACKAGE:**
  Flat lead style for better performance
- **TAPE AND REEL PACKAGING AVAILABLE**

BLOCK DIAGRAM



DESCRIPTION

The UPC8195K is a Silicon Microwave Monolithic Integrated Circuit designed as a transmitter/TX section for W-CDMA. The UPC8195K is a TX-IF IC including IF-AGC amplifier and modulator. This IC is suitable for kit-use for W-CDMA IF section.

This IC was developed using NEC's new ultra high seed silicon bipolar process.

NEC's stringent quality assurance and test procedures ensure the highest reliability and perormance.

APPLICATIONS

- **W-CDMA**

ELECTRICAL CHARACTERISTICS (unless otherwise specified, T_A = 25°C, V_{CC} = 3.0 V, fIF = 380 MHz, fLO = 760 MHz, PLO = -15 dBm, fI/Q =10 kHz, 400 mVp-p balanced sine-wave)

PART NUMBER PACKAGE OUTLINE			UP8195K QFN-20		
SYMBOLS	**PARAMETERS AND CONDITIONS**	**UNITS**	**MIN**	**TYP**	**MAX**
I_{CC}	Circuit Current, no input signals At power saving mode	mA μA	– –	25.5 –	30 1
P_{OUT}	Output Power, V_{CONT}= 2.3 V, I/Q = 400mVp-p balanced V_{CONT}= 0.3 V, I/Q = 400mVp-p balanced	dBm	-17 –	-13 -88	– -83
LoL	Local Leakage, V_{CONT}= 2.3 V, I/Q = 400mVp-p balanced	dBc	–	–	-30
I_{mR}	Image Rejection, V_{CONT}= 2.3 V, I/Q = 400mVp-p balanced	dBc	–	–	-30
$T_{PS(Rise)}$	Rise time from power-saving mode	us	–	–	10
$V_{PS(Rise)}$	Rising voltage from power-saving mode	V	2.2	–	–
$V_{PS(fall)}$	Falling voltage from power-saving mode	V	–	–	0.5

STANDARD CHARACTERISTICS FOR REFERENCE (unless otherwise specified, T_A = 25°C, V_{CC} = 3.0 V, fIF = 380 MHz, fLO = 760 MHz, PLO = -15 dBm, fI/Q =10 kHz, 400 mVp-p balanced sine-wave)

PART NUMBER PACKAGE OUTLINE			UP8195K QFN-20		
SYMBOLS	**PARAMETERS AND CONDITIONS**	**UNITS**	**MIN**	**TYP**	**MAX**
NF_{L1}	Output Noise Level 1, Pout = -25 dBm, fIF±20MHz	dBm/Hz	–	-147	–
NF_{L2}	Output Noise Level 2, Pout = -65 dBm, fIF±20MHz	dBm/Hz	–	-160	–
GF	Gain Flatness, fIF±2.5MHz	dB	–	–	0.25
EVM	Error Vector Magnitude, I/Q = 3.84 Msps QPSK	%rms	–	3	–
ACPR	Adjacent Channel Power Ratio, fIF±5 MHz, I/Q=3.84 Msps QPSK	dBc	–	-55	–

ABSOLUTE MAXIMUM RATINGS[1] (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CC}	Supply Voltage	V	4.0
V_{PS}, V_{CONT}	Applied Voltage	V	-0.3 to V_{CC}+0.3
T_A	Ope rating Ambient Temperature	°C	-40 to +85
T_{STG}	Storage Temperature	°C	-55 to +150
P_D	Power Dissipation	mW	309

Notes:
1. Operation in excess of any one of these parameters may result in permanent damage.

RECOMMENDED OPERATING CONDITIONS

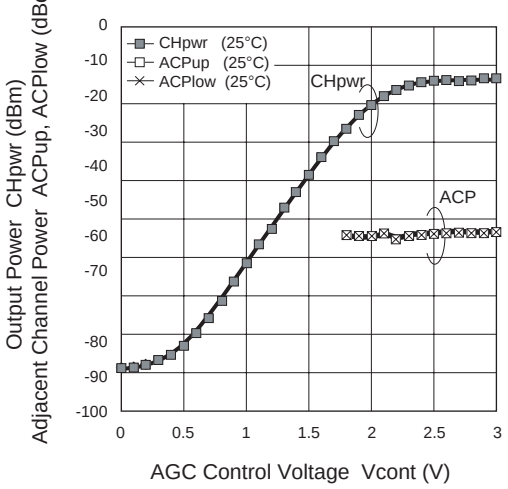
SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{CC}	Supply Voltage	V	2.7	3.0	3.3
T_A	Operating Ambient Temperature	°C	-25	+25	+85
fIF	IF Frequency	MHz	–	380	–
f_{LO}	Local Frequency	MHz	–	760	–
P_{LO}	Local input Level	dBm	-18	-15	-12
ZIF	IF output impedance, Balanced output internal resistance	kΩ	–	1	–
VI/Q	I/Q Maximum Input Voltage	V	–	0.4	1

ORDERING INFORMATION

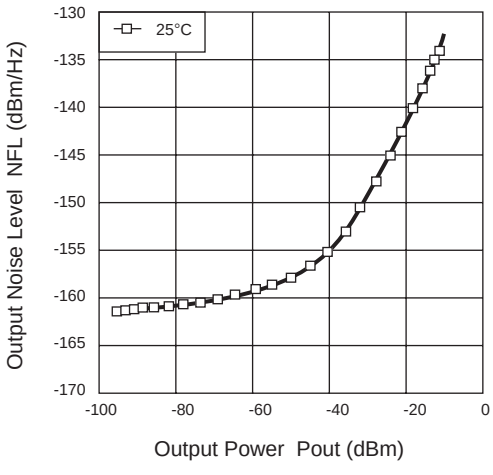
Part Number	Package
UPC8195K-E1	20 Pin plastic QFN

TYPICAL PERFORMANCE CURVES (T_A = 25°C)

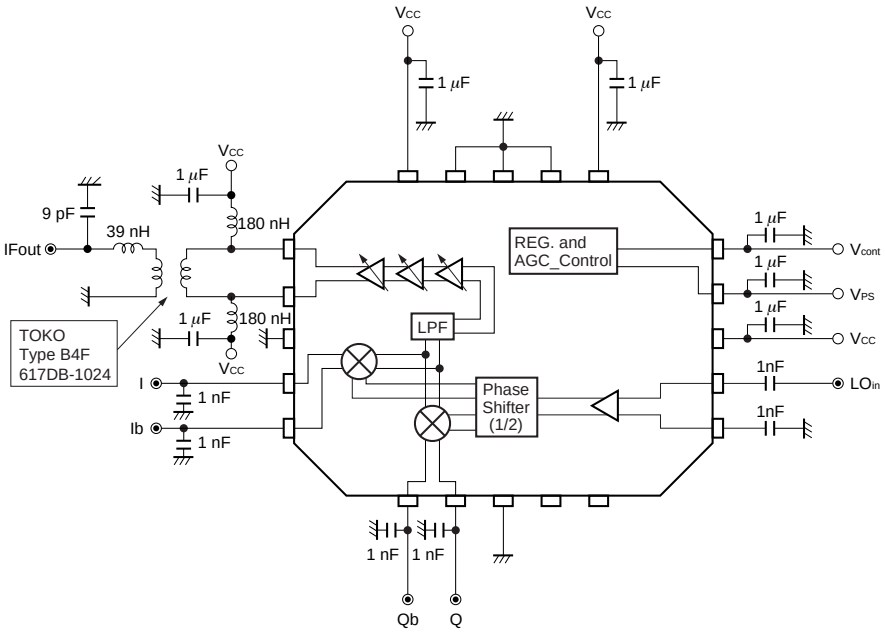
OUTPUT POWER, ADJACENT CHANNEL POWER vs. AGC CONTROL VOLTAGE



OUTPUT NOISE LEVEL vs. OUTPUT POWER



MEASUEMENT CIRCUIT (Units in mm)

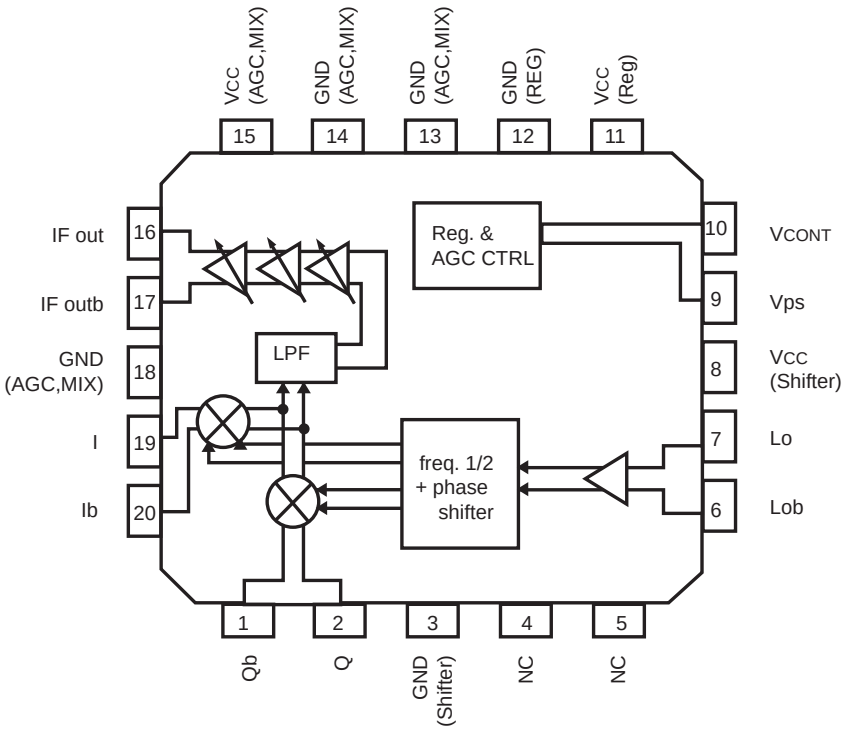


Remarks 1. ◉ : AC connector

○ : DC terminal

2. In the case of ACPR, output noise level, EVM measurement, 1 nF capacitors of I, Ib, Q, Qb are removed.

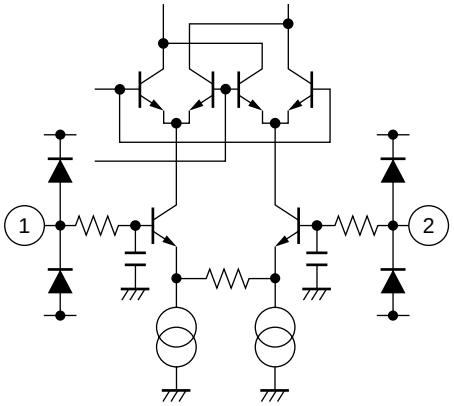
BLOCK DIAGRAM (Units in mm)



PASSW

- UPC8191K: Mix = two pieces of Divide-by-2 F/F phase shifter (=3/4). Pin 4, 5 are for exteranl Tank circuit.
- UPC8195K: Only one piece of Divide-by-2 F/F phase shifter (=1/2). Pin 4, 5 are non -connection.

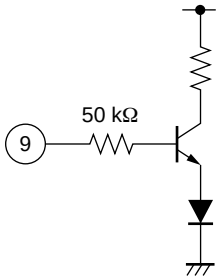
PIN FUNCTIONS (Pin Voltage is measured at V_{CC} = 2.85 V)

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Applied Voltage (V)</th><th>Pin Voltage (V)</th><th>Functions and Applications</th><th>Internal Equivalent Circuits</th></tr>
<tr><td>1</td><td>Qb</td><td>V_{CC}/2</td><td>-</td><td rowspan="2">Q signal input pin.
Apply bias voltage externally.
Maximum balance input voltage is
1 000 mV_{p-p} (balance).</td><td rowspan="2"> 
</td></tr>
<tr><td>2</td><td>Q</td><td>V_{CC}/2</td><td>-</td></tr>
<tr><td>3</td><td>GND (Shifter)</td><td>0</td><td>-</td><td>Ground pin of I/Q modulator.
This pin should be grounded with minimum inductance.
Form the ground pattern as widely as possible to minimize ground impedance.</td><td>–</td></tr>
<tr><td>4
5</td><td>N.C.</td><td>0</td><td>-</td><td>No connection

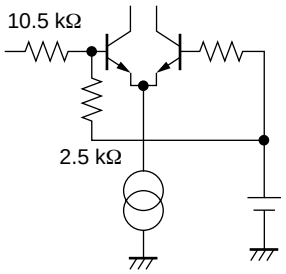
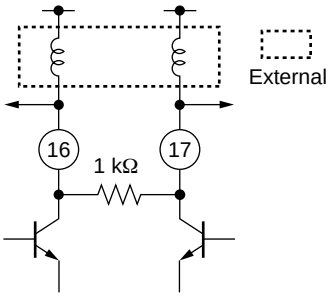
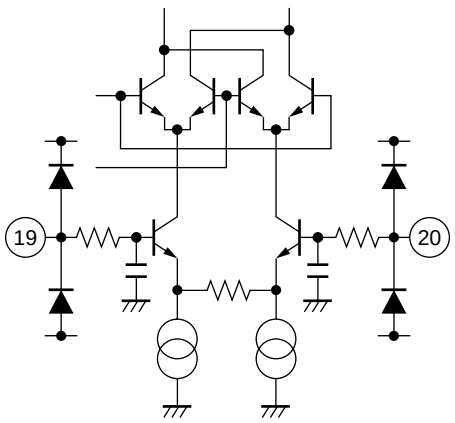
This pin is not connected to internal circuit

This pin should be opened or grounded.</td><td>–</td></tr>
<tr><td>6</td><td>LOb</td><td>0</td><td>2.02</td><td>Bypass pin of local signal input for I/Q modulator.

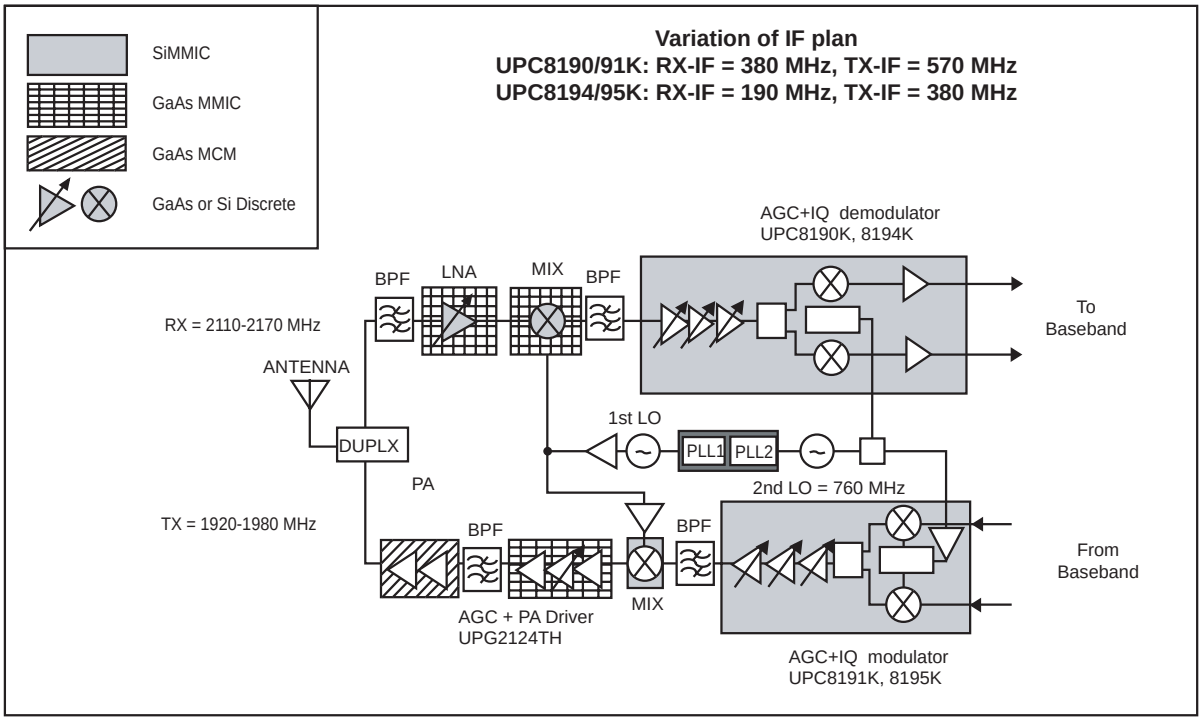
In the case of single local input,
this pin must be decoupled with capacitor
ex. 1 000 pF.</td><td>–</td></tr>
<tr><td>7</td><td>LO</td><td>0</td><td>2.02</td><td>Local signal input of I/Q modulator.
The DC cut capacitor ex. 1 000 pF
must be attaced to this pin.</td><td>–</td></tr>
<tr><td>8</td><td>V_{CC} (Shifter)</td><td>2.7 to 3.3</td><td>-</td><td>Supply voltage pin of I/Q modulator.</td><td>–</td></tr>
<tr><td>9</td><td>V_{PS}</td><td>0 to 3.0</td><td>-</td><td>Power saving pin of I/Q modulator + AGC amplifier.

This pin modulator can control
Active/Sleep state with bias as follows.
<table>
<tr><th>V_{PS} (V)</th><th>State</th></tr>
<tr><td>0 to 0.5</td><td>Sleep Mode</td></tr>
<tr><td>2.2 to 3</td><td>Active Mode</td></tr>
</table></td><td> 
</td></tr>
</table>

PIN FUNCTIONS (Pin Voltage is measured at Vcc = 2.85 V)

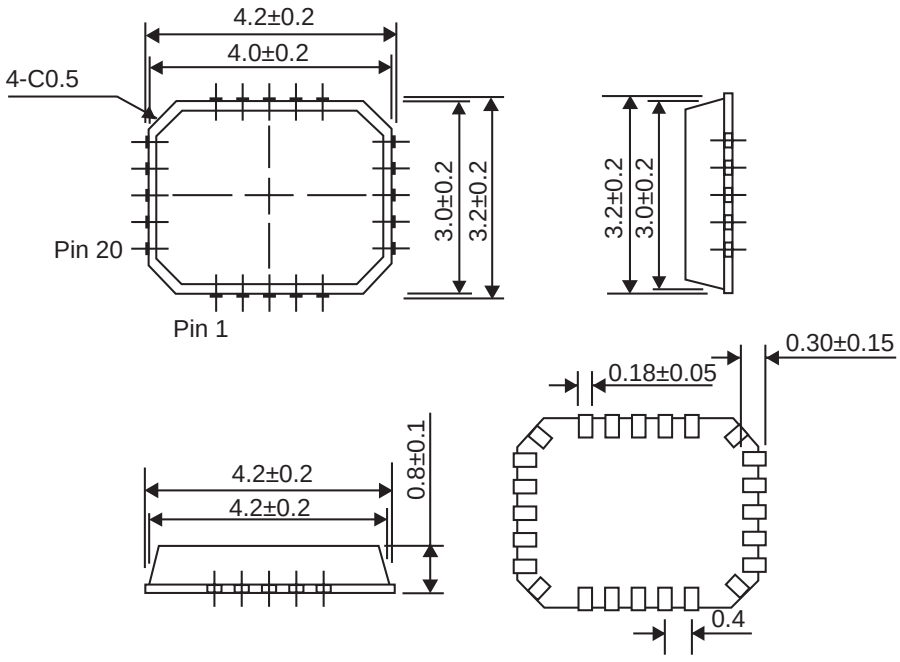
Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V)	Functions and Applications	Internal Equivalent Circuits
10	Vcont	0 to 3.0	-	Gain control pin of AGC amplifier. Variable gains are available in accordance with applied voltage between 0 to 3.0 V.	
11	Vcc (REG.)	2.7 to 3.3	-	Supply voltage pin of internal regulator.	–
12	GND (REG.)	0	-	Ground pin internal regulator. This pin should be grounded with minimum inductance. Form the ground pattern as widely as possible to minimize ground impedance.	–
13 14 18	GND (AGC, MIX)	0	-	Ground pin of AGC amplifier + I/Q Mixer. This pin should be grounded with minimum inductance. Form the ground pattern as widely as possible to minimize ground impedance.	–
15	Vcc (AGC , MIX)	2.7 to 3.3	-	Supply voltage pin of AGC amplifier + I/Q Mixer.	–
16	IFout	2.7 to 3.3	-	IF output pin. The inductor must be attached between Vcc and output pin due to open collector. Output frequency is 570 MHz which is 3/4 of local signal frequency 760 MHz.	
17	IFoutb	2.7 to 3.3	-	Balance output of IFout pin. The inductor must be attached between Vcc and output pin due to open collector.	
19	I	Vcc/2	-	I signal input pin. Apply bias voltage externally. Maximum balance input voltage is 1 000 mVP-P (balance).	
20	Ib	Vcc/2	-		

APPLICATION EXAMPLE: W-CDMA



OUTLINE DIMENSIONS (Units in mm)

Package Outline QFN-20



Life Support Applications
These NEC products are not intended for use in life support devices, appliances, or systems where the malfunction of these products can reasonably be expected to result in personal injury. The customers of CEL using or selling these products for use in such applications do so at their own risk and agree to fully indemnify CEL for all damages resulting from such improper use or sale.