

1.5 V/1.0 A GENERAL-PURPOSE
CMOS REGULATOR

DESCRIPTION

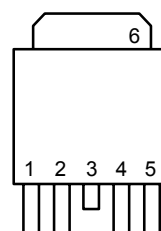
μ PD12115 is a general-purpose CMOS regulator which has 1.5 V output voltage and 1.0 A output current capacity. This product is suitable for low power-supply-voltage LSI etc. By ON/OFF function, the power consumption can be kept low level at the time of off-state.

FEATURES

- Output Current: 1.0 A
- Output Voltage: 1.5 V (Fixed type)
- Output Voltage Tolerance: $V_o \pm 2.0\%$ ($T_J = 25^\circ\text{C}$)
- Dropout Voltage: $V_{DIF} = 1.0 \text{ V MAX.}$ ($I_o = 1.0 \text{ A}$)
- Quiescent Current: $150 \mu\text{A TYP.}$ ($I_o = 0 \text{ A}$)
- Standby Current: $1 \mu\text{A}$
- Available for laminated ceramic capacitor: (Electric capacity $10 \mu\text{F}$ or higher)
- On-chip over-current protection circuit
- On-chip thermal shut down circuit

PIN CONFIGURATION (Marking Side)

5-PIN TO-252 (5-PIN MP-3ZK)



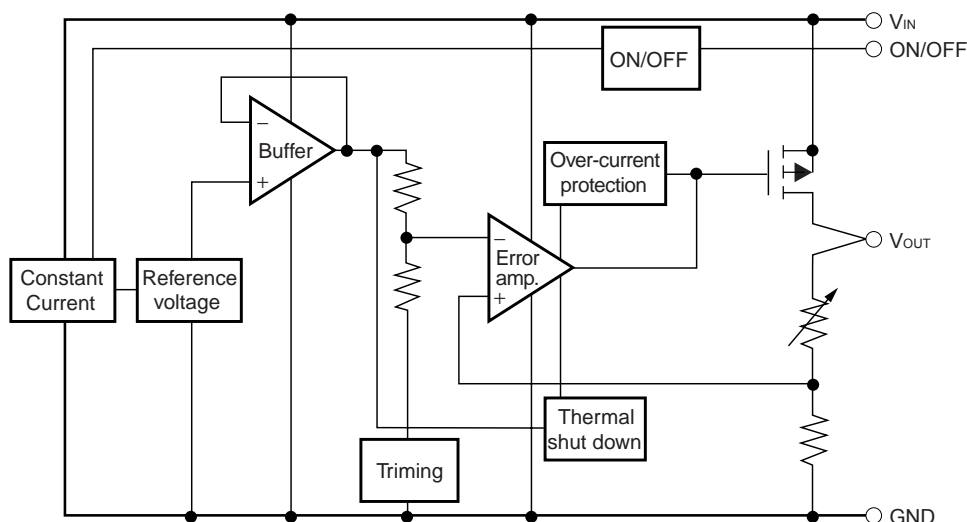
1. INPUT
2. ON/OFF
3. GND ^{Note}
4. NC
5. OUTPUT
6. GND (Fin)

Note No.3 pin is cut and can not be connected to substrate. No.6 is Fin and common to GND pin.

APPLICATIONS

This regulator is suitable for low power-supply-voltage LSI which is used in digital appliances etc.

BLOCK DIAGRAM



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ORDERING INFORMATION

Part Number	Package	Output Voltage	Type	Marking
μPD12115T1F	5-PIN TO-252 (5-PIN MP-3ZK)	1.5 V	Fixed	12115

Remark Since it is the tape-packaged product, “-E1” or “-E2” is added to the end of its product name.

Part Number	Package	Package Type
μPD12115T1F-E1-AT ^{Note}	5-PIN TO-252 (5-PIN MP-3ZK)	<ul style="list-style-type: none"> • 16 mm wide embossed taping • Pin 1 on draw-out side • 2,500 pcs/reel
μPD12115T1F-E2-AT ^{Note}	5-PIN TO-252 (5-PIN MP-3ZK)	<ul style="list-style-type: none"> • 16 mm wide embossed taping • Pin 1 at take-up side • 2,500 pcs/reel

Note Pb-free (This product does not contain Pb in the external electrode and other parts.)

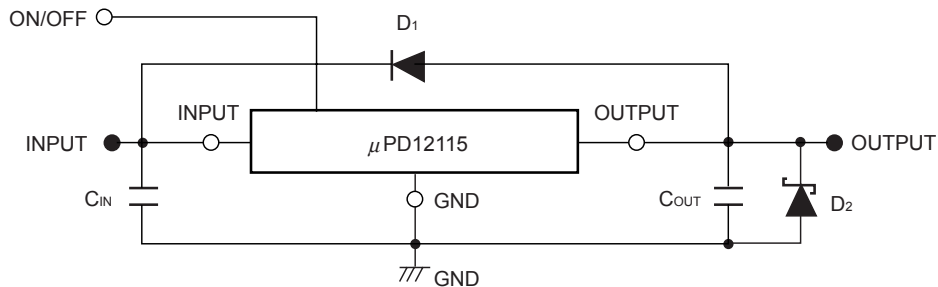
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Rating	Unit
Input Voltage	V _{IN}	-0.3 to +6.0	V
ON/OFF Pin Voltage	V _{ON/OFF}	-0.3 to V _{IN}	V
Internal Power Dissipation (T _C = 25°C) ^{Note}	P _T	10	W
Operating Ambient Temperature	T _A	-40 to +85	°C
Operating Junction Temperature	T _J	-40 to +150	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Thermal Resistance (junction to ambient)	R _{th(J-A)}	125	°C/W
Thermal Resistance (junction to case)	R _{th(J-C)}	12.5	°C/W

Note Internally limited. When the operating junction temperature rises above 150°C, the internal circuit shuts down the output voltage.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

TYPICAL CONNECTION



C_{IN} : 0.1 μF or higher. Be sure to connect C_{IN} to prevent parasitic oscillation. Set this value according to the length of the line between the regulator and the INPUT pin. Use of a film capacitor or other capacitor with first-rate voltage and temperature characteristics is recommended. If using a laminated ceramic capacitor, it is necessary to ensure that C_{IN} is 0.1 μF or higher for the voltage and temperature range to be used.

C_{OUT}: 10 μF or higher. Be sure to connect C_{OUT} to prevent oscillation and improve excessive load regulation. Place C_{IN} and C_{OUT} as close as possible to the IC pins (within 1 to 2 cm). Also, in case of using a laminated ceramic capacitor, please note following items.

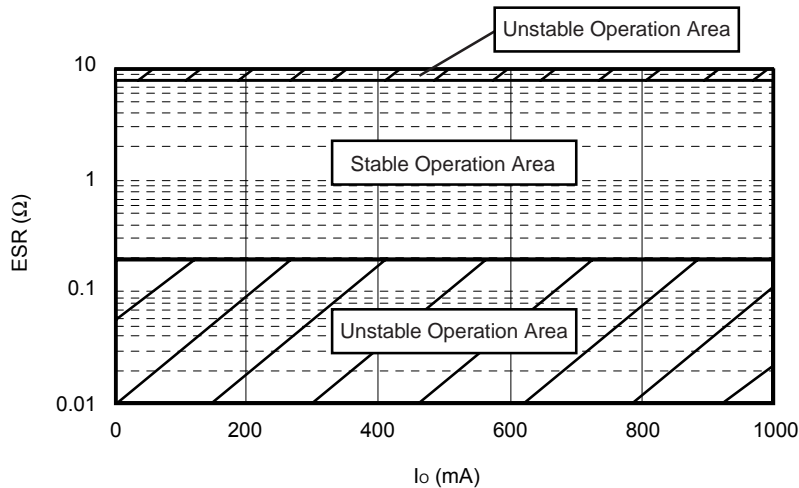
- It is necessary to ensure that C_{OUT} is 10 μF or higher for the voltage and temperature range to be used.
- In case of using laminated ceramic capacitor, it is easy to become state of parasitic oscillation. Because ESR of laminated ceramic capacitor is very low. Therefore, the capacitor and load condition (output current) which fulfill the condition of the stable operation area of ESR shown below are recommended.
- Stable Operation Area as below is regulated under condition of which this product is not on a substrate. Therefore impedance on substrate is not considered.

D₁ : If the OUTPUT pin has a higher voltage than the INPUT pin, connect a diode.

D₂ : If the OUTPUT pin has a lower voltage than the GND pin, connect a Schottky barrier diode.

Caution Make sure that no external voltage is applied to the OUTPUT pin.

μPD12115 C_{OUT} ESR Stable Operation Area



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Input Voltage	V _{IN}	2.5		5.5	V
ON/OFF Pin Voltage	V _{ON/OFF}	0		V _{IN}	V
Output Current	I _o	0		1.0	A
Operating Ambient Temperature	T _A	-40		+85	°C
Operating Junction Temperature	T _J	-40		+125	°C

Caution1. Turn on V_{IN} and V_{ON/OFF} at the same time, or turn on V_{IN} first and then V_{ON/OFF}.

Turn off V_{IN} and V_{ON/OFF} at the same time, or turn off V_{ON/OFF} first and then V_{IN}.

2. If absolute maximum rating is not exceeded, you can used this product above the recommended operating range. However, since a margin with absolute maximum rating decreases, please use this product after sufficient evaluation.

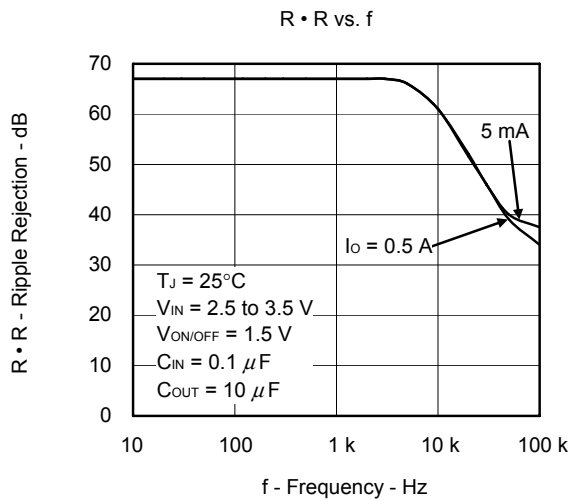
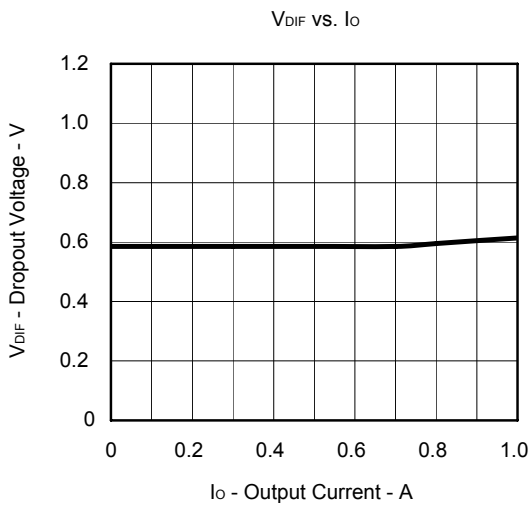
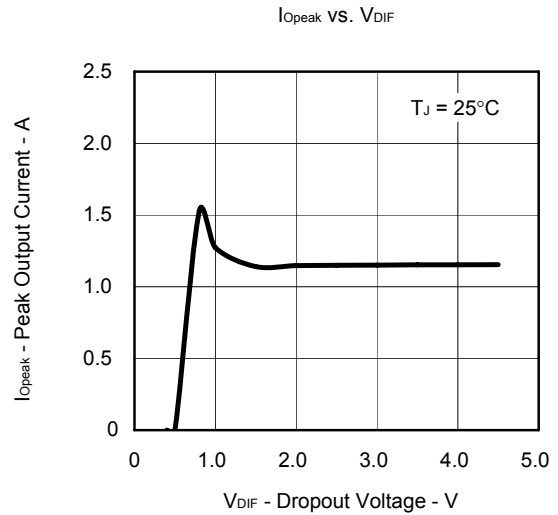
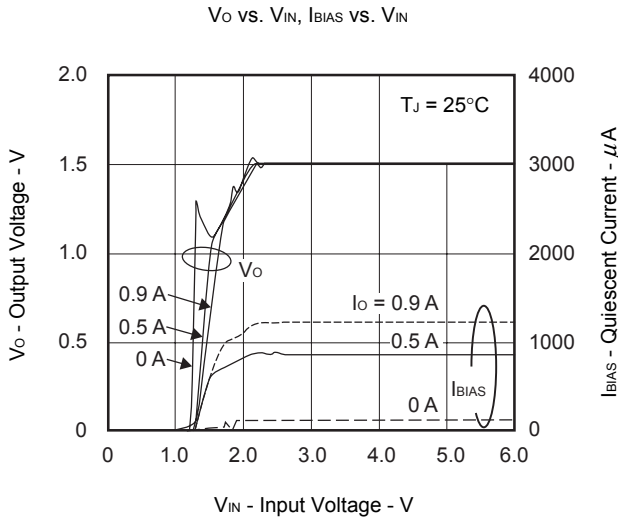
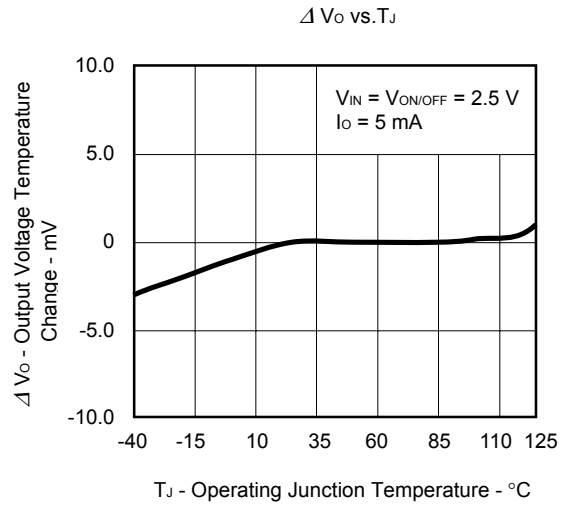
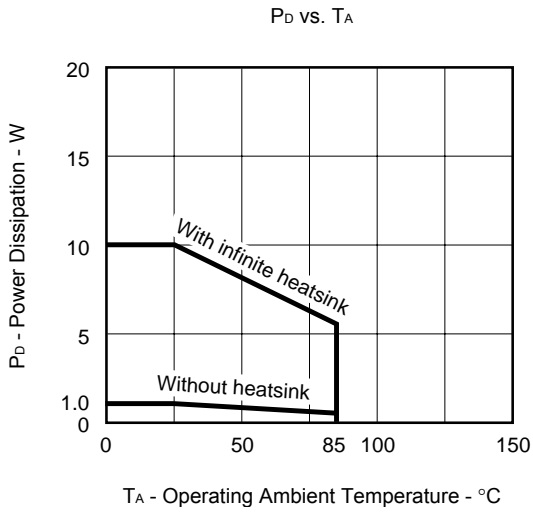
ELECTRICAL CHARACTERISTICS

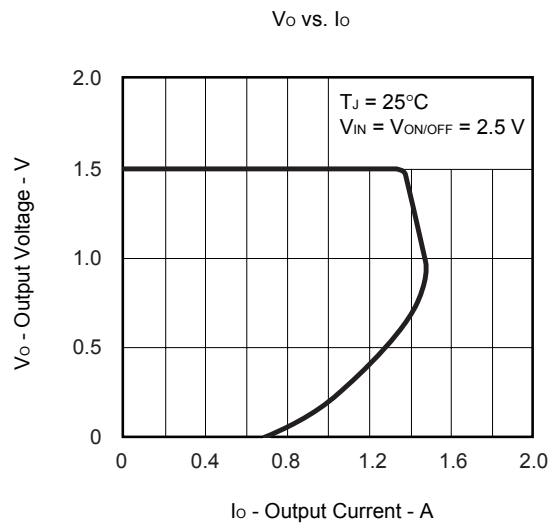
(T_J = 25°C, V_{IN} = V_{ON/OFF} = 2.5 V, I_O = 0.5 A, C_{IN} = 0.1 μF, C_{OUT} = 10 μF, unless otherwise specified)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output Voltage	V _{O1}	–	1.47	1.5	1.53	V
	V _{O2}	2.5 V ≤ V _{IN} ≤ 5.5 V, 0 A ≤ I _O ≤ 1.0 A	(1.455)	–	(1.545)	V
Line Regulation	REG _{IN}	2.5 V ≤ V _{IN} ≤ 5.5 V	–	1	15	mV
Load Regulation	REG _L	0 A ≤ I _O ≤ 1.0 A	–	1	15	mV
Quiescent Current	I _{BIAS1}	I _O = 0 A	–	150	300	μA
	I _{BIAS2}	I _O = 1.0 A	–	(1600)	(3000)	μA
Quiescent Current Change	ΔI _{BIAS1}	2.5 V ≤ V _{IN} ≤ 5.5 V	–	(10)	(300)	μA
	ΔI _{BIAS2}	0 A ≤ I _O ≤ 1.0 A	–	(1450)	(3000)	μA
Output Noise Voltage	V _n	10 Hz ≤ f ≤ 100 kHz	–	165	–	μV _{r.m.s.}
Ripple Rejection	R • R	f = 1 kHz, 2.5 V ≤ V _{IN} ≤ 3.5 V	–	65	–	dB
Dropout Voltage	V _{DIF}	I _O = 1.0 A	–	0.6	1.0	V
Short Circuit Current	I _{Oshort}	–	–	0.7	–	A
Peak Output Current	I _{Opeak}	–	1.0	–	–	A
Temperature Coefficient of Output Voltage	ΔV _O /ΔT	I _O = 5 mA, 0°C ≤ T _J ≤ 125°C	–	0.02	–	mV/°C
ON-state Voltage	V _{ON}	I _O = 0 A	1.5	–	V _{IN}	V
OFF-state Voltage	V _{OFF}	I _O = 0 A	–	–	0.5	V
ON-state ON/OFF Pin Current	I _{ON}	I _O = 0 A	–	–	2	μA
Standby Current	I _{BIAS(OFF)}	V _{ON/OFF} = 0 V	–	–	1	μA

Remark Values in parentheses are product design values, and are thus provided as reference values.

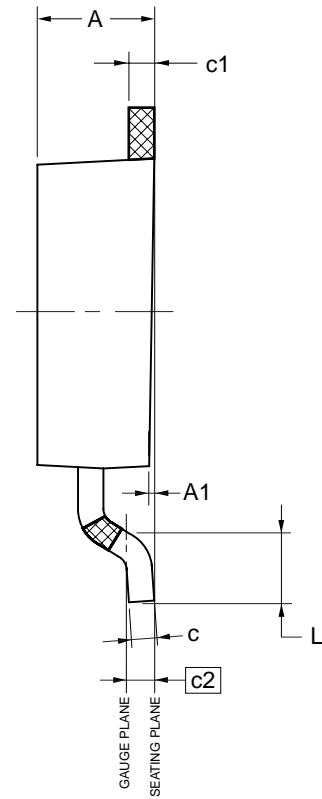
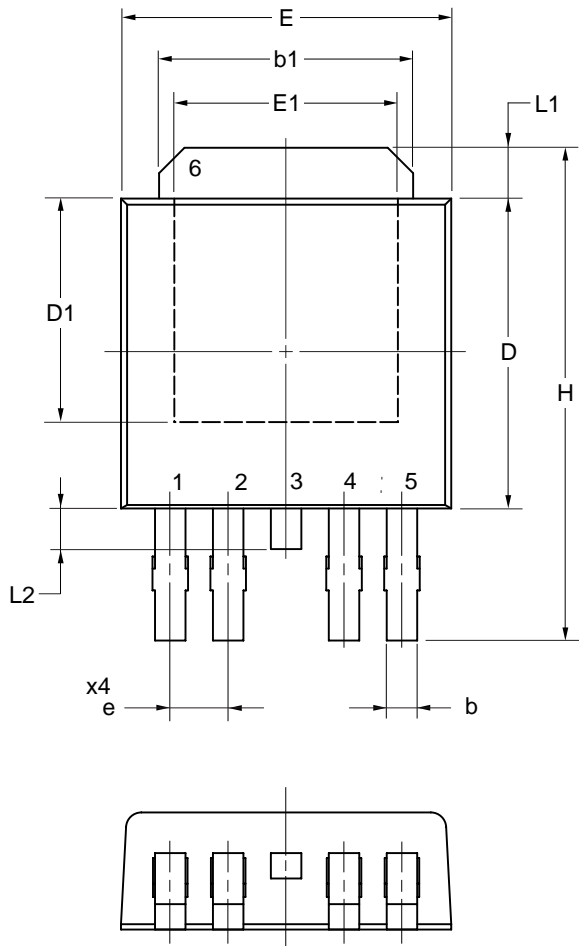
TYPICAL CHARACTERISTICS





PACKAGE DRAWING (Unit: mm)

5-PIN TO-252 (MP-3ZK)



(UNIT:mm)

ITEM	DIMENSIONS
D	6.10±0.20
D1	4.4TYP(4.0MIN)
E	6.50±0.20
E1	4.4TYP(4.3MIN)
H	9.8TYP(10.3MAX)
A	2.30±0.10
A1	0 to 0.25
b	0.60±0.10
b1	5.0
c	0.50±0.10
c1	0.50±0.10
c2	0.508
e	1.14
L	1.52±0.12
L1	1.0
L2	0.80

P5T1F-114-1

NOTE

1. No Plating area

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RECOMMENDED MOUNTING CONDITIONS

The μPD12115 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

μPD12115T1F-AT ^{Note}: 5-PIN TO-252 (5-PIN MP-3ZK)

Process	Conditions	Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds MAX. (at 220°C or higher), Count: Three times, Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended.	IR60-00-3
Partial Heating Method	Pin temperature: 350°C or below, Heat time: 3 seconds or less (per each side of the device).	P350

Note Pb-free (This product does not contain Pb in the external electrode and other parts.)

Caution Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

REFERENCE DOCUMENTS

USER'S MANUAL USAGE OF THREE TERMINAL REGULATORS Document No.G12702E
 INFORMATION VOLTAGE REGULATOR OF SMD Document No.G11872E
 SEMICONDUCTOR DEVICE MOUNT MANUAL <http://www.necel.com/pkg/en/mount/index.html>

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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