DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD121A10

2-POWER SUPPLY INPUT METHOD 1.0 V/2.0 A REGULATOR

DESCRIPTION

μPD121A10 is the CMOS regulator which can output 2.0 A current. This regulator is suitable for power supply for 1.0 V ASIC core, for example our companies' CB-90 (90 nm process LSI) etc. The dropout voltage is made small (0.7 V MAX. (I_O = 1.0 A) by dividing bias voltage (V_{DD}) from input voltage (V_{IN}). Therefore this product can output under the conditions, $V_{IN} \geq 1.62$ V ($V_{DD} \geq 4.0$ V). Output voltage can be adjustable between 0.95 and 1.15 V.

FEATURES

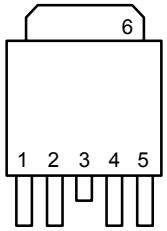
- Output Current: 2.0 A
- Output Voltage: 0.95 to 1.15 V
- Bias Voltage: 4.0 to 5.5 V
- Reference Voltage Tolerance: $V_{REF} \pm 10$ mV (T_J = 25°C)
- Low Dropout Voltage: V_{DIF} = 0.7 V MAX. (I_O = 1.0 A)
- On-chip over-current protection circuit
- On-chip thermal shut down circuit

APPLICATIONS

This regulator is suitable for low power supply voltage IC, for example core of CB-90 (90 nm process LSI) etc.

PIN CONFIGURATION (Marking Side)

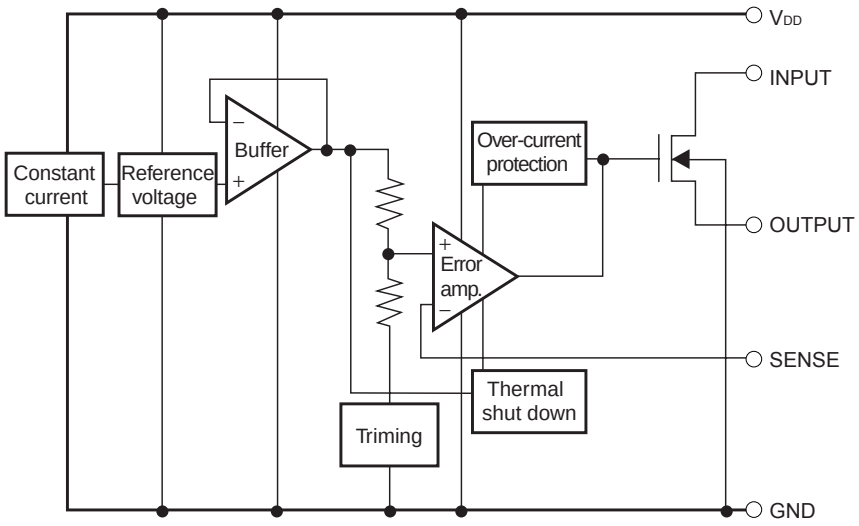
5-PIN TO-252 (5-PIN MP-3ZK)



1. INPUT
2. V_{DD} (ON/OFF)
3. GND **Note**
4. SENSE
5. OUTPUT
6. GND (Fin)

Note No.3 pin is cut and can not be connected to substrate. No.6 is Fin and common to GND pin.

BLOCK DIAGRAM



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ORDERING INFORMATION

Part Number	Package	Reference Voltage	Output Voltage	Marking
μPD121A10T1F	5-PIN TO-252 (5-PIN MP-3ZK)	0.6 V	0.95 to 1.15 V	121A10

Remark Since it is the tape-packaged product, "-E1" or "-E2" is added to the end of its product name.

Part Number [Note]	Package	Package Type
μPD121A10T1F-E1-AT	5-PIN TO-252 (5-PIN MP-3ZK)	• 16 mm wide embossed taping • Pin 1 on draw-out side • 2,500 pcs/reel
μPD121A10T1F-E2-AT	5-PIN TO-252 (5-PIN MP-3ZK)	• 16 mm wide embossed taping • Pin 1 at take-up side • 2,500 pcs/reel

Note Pb-free (This product does not contain Pb in the external electrode and other parts.)

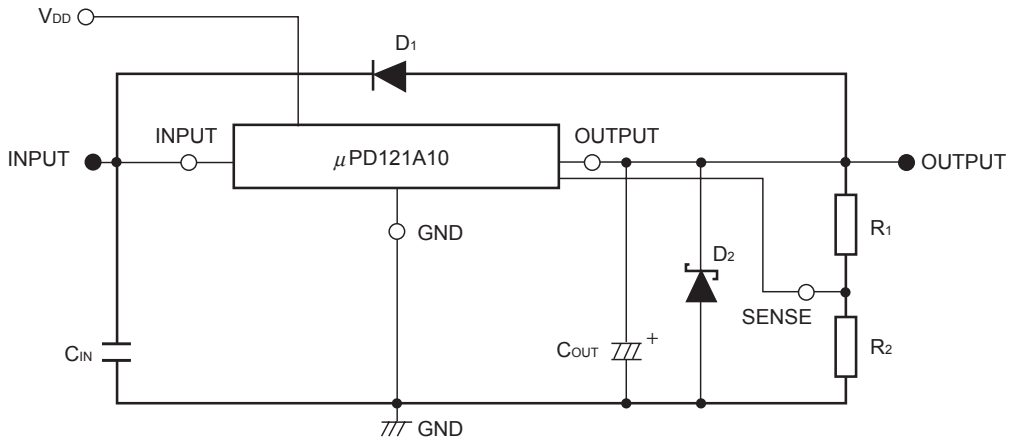
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Rating	Unit
Input Voltage	V_{IN}	−0.3 to +6.0	V
Bias Voltage	V_{DD}	−0.3 to +6.0	V
Internal Power Dissipation (T_C = 25°C) [Note]	P_T	10	W
Operating Ambient Temperature	T_A	−20 to +85	°C
Operating Junction Temperature	T_J	−20 to +150	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Thermal Resistance (junction to ambient)	$R_{th(J-A)}$	125	°C/W
Thermal Resistance (junction to case)	$R_{th(J-C)}$	12.5	°C/W

Note Internally limited. When the operating junction temperature rises above 150°C, the internal circuit shuts down the output voltage.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

TYPICAL CONNECTION



C_{IN} : 0.1 μF or higher. Be sure to connect C_{IN} to prevent parasitic oscillation. Set this value according to the length of the line between the regulator and the INPUT pin. Use of a film capacitor or other capacitor with first-rate voltage and temperature characteristics is recommended. If using a laminated ceramic capacitor, it is necessary to ensure that C_{IN} is 0.1 μF or higher for the voltage and temperature range to be used.

C_{OUT} : 10 μF or higher. Be sure to connect C_{OUT} to prevent oscillation and improve excessive load regulation. Place C_{IN} and C_{OUT} as close as possible to the IC pins (within 1 to 2 cm). Use the capacitor whose capacitance value is 10 μF or more under use conditions.

D_1 : If the OUTPUT pin has a higher voltage than the INPUT pin, connect a diode.

D_2 : If the OUTPUT pin has a lower voltage than the GND pin, connect a Schottky barrier diode.

R_1, R_2: The total amount of R_1 and R_2 is sure to below 200 kΩ (100 kΩ TYP.).

$V_{OUT} = (1 + R_1/R_2) V_{REF}$ **Note**

Note When V_{OUT} = 1 V: R_1 = 40 kΩ, R_2 = 60 kΩ

Caution1. Make sure that no external voltage is applied to the OUTPUT pin.

2. V_{DD} pins (Bias voltage) must be supplied in a separate power supply from that of INPUT pins (Input voltage).

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Input Voltage (V_O = 1.0 V)	V_{IN}	1.62 **Note**	2.0	2.65	V
Output Voltage	V_O	0.95	1.0	1.15	V
Bias Voltage	V_{DD}	4.0	5.0	5.5	V
Output Current	I_O	0		2.0	A
Operating Ambient Temperature	T_A	−20		+85	°C
Operating Junction Temperature	T_J	−20		+125	°C

Note It needs 1.7 V ≤ V_{IN} ≤ 2.65 V to output I_O = 2.0 A.

Caution1. Power on V_{IN} first, and then V_{DD} on start-up. When the power is turned off, turn off V_{DD} first. Note that the voltage of V_{DD} must not be kept 3.0 V or less.

2. If absolute maximum rating is not exceeded, you can used this product above the recommended operating range. However, since a margin with absolute maximum rating decreases, please use this product after sufficient evaluation.

ELECTRICAL CHARACTERISTICS

(T_J = 25°C, V_{IN} = 2.0 V, V_{DD} = 5.0 V, I_O = 1.0 A, V_O = 1.0 V, C_{IN} = 0.1 μF, C_{OUT} = 10 μF, unless otherwise specified)

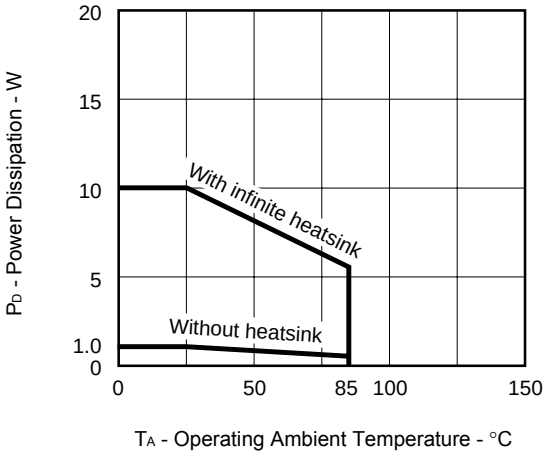
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Reference Voltage (SENSE pin)	V_{REF1}	–	0.59	0.6	0.61	V
	V_{REF2}	−20°C ≤ T_J ≤ +125°C	(0.58)	–	(0.62)	V
Line Regulation	REG_{IN}	1.7 V ≤ V_{IN} ≤ 2.65 V	–	1	15	mV
Load Regulation	REG_L	0 A ≤ I_O ≤ 2.0 A	–	1	15	mV
Quiescent Current	I_{BIAS1}	I_O = 0 A	–	125	500	μA
	I_{BIAS2}	I_O = 2.0 A	–	300	1000	μA
Quiescent Current Change	ΔI_{BIAS1}	4.0 V ≤ V_{DD} ≤ 5.5 V, I_O = 0 A	–	12	300	μA
	ΔI_{BIAS2}	0 A ≤ I_O ≤ 2.0 A	–	100	500	μA
Output Noise Voltage	V_n	10 Hz ≤ f ≤ 100 kHz	–	230	–	$\mu V_{r.m.s.}$
Ripple Rejection	R • R	f = 1 kHz, 1.8 V ≤ V_{IN} ≤ 2.2 V	–	56	–	dB
Dropout Voltage	V_{DIF}	I_O = 1.0 A	–	0.17	0.7	V
Short Circuit Current	I_{Oshort}	V_O = 0 V	–	3.0	–	A
Peak Output Current	I_{Opeak}	4.0 V ≤ V_{DD} ≤ 5.5 V	2.0	–	–	A
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	I_O = 0 A, 0°C ≤ T_J ≤ 125°C	–	0.14	–	mV/°C
ON-state Voltage (V_{DD})	$V_{DD(ON)}$	–	4.0	–	–	V
OFF-state Voltage (V_{DD})	$V_{DD(OFF)}$	–	–	–	0.5	V
ON-state Bias Pin (V_{DD} Pin) Current	$I_{BIAS(ON1)}$	I_O = 0 A	–	I_{BIAS1}	–	μA
	$I_{BIAS(ON2)}$	I_O = 2.0 A	–	I_{BIAS2}	–	μA
OFF-state Bias Pin (V_{DD} Pin) Current **Note**	$I_{BIAS(OFF)}$	I_O = 0 A, V_{DD} = 0 V	–	–	1	μA

Note Standby Current

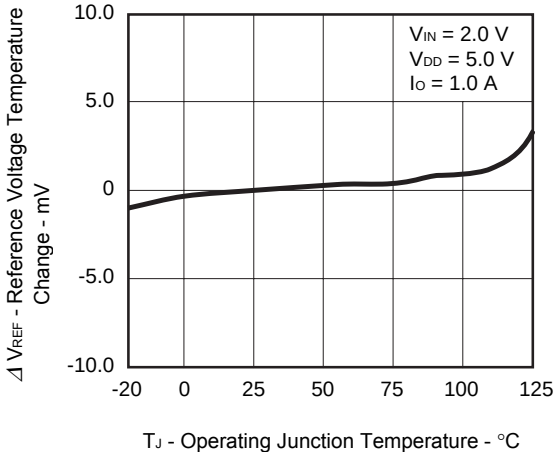
Remark Values in parentheses are product design values, and are thus provided as reference values.

TYPICAL CHARACTERISTICS

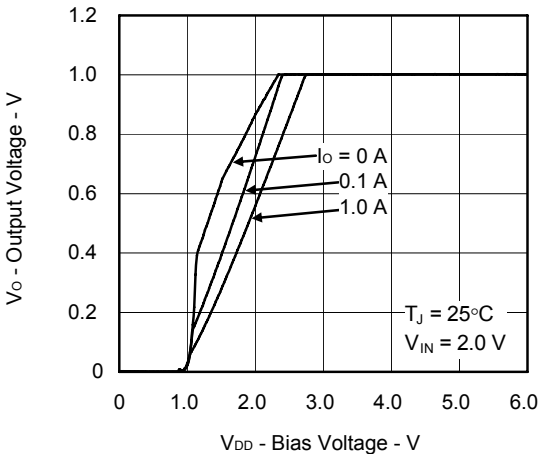
P_D vs. T_A



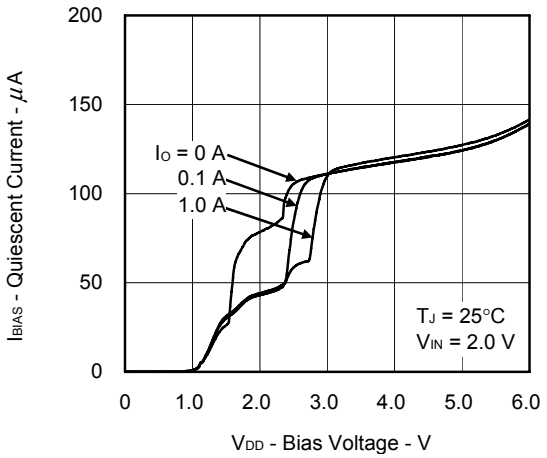
ΔV_{REF} vs.T_J



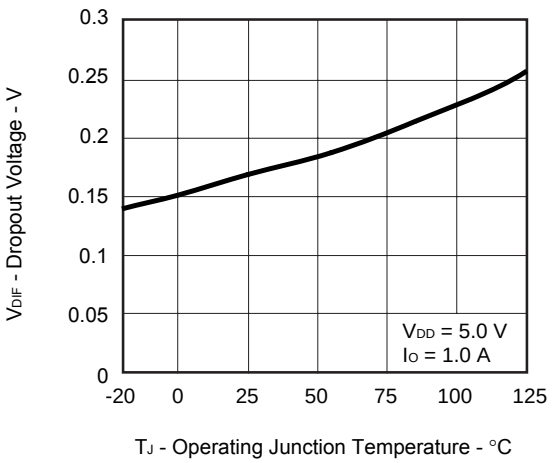
V_O vs. V_{DD}



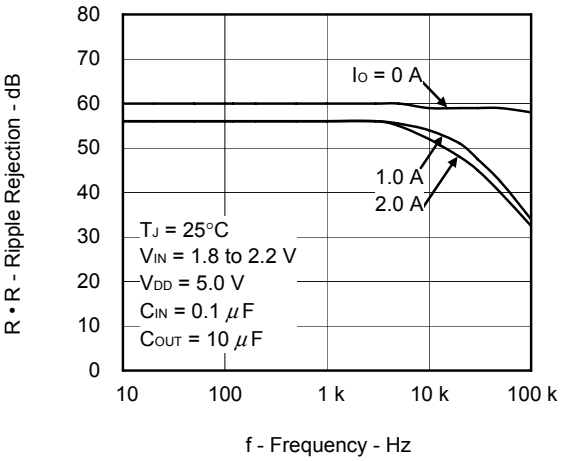
I_{BIAS} vs. V_{DD}



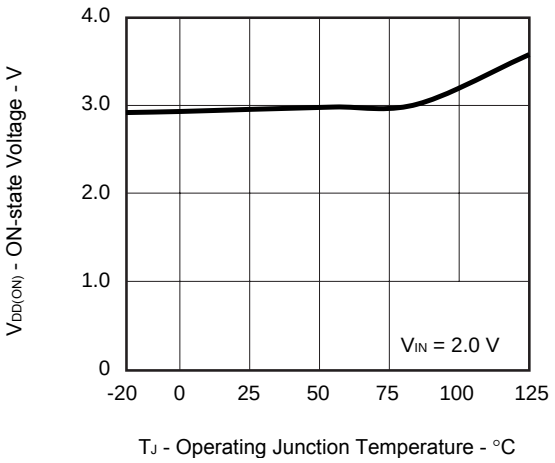
V_{DIF} vs. T_J



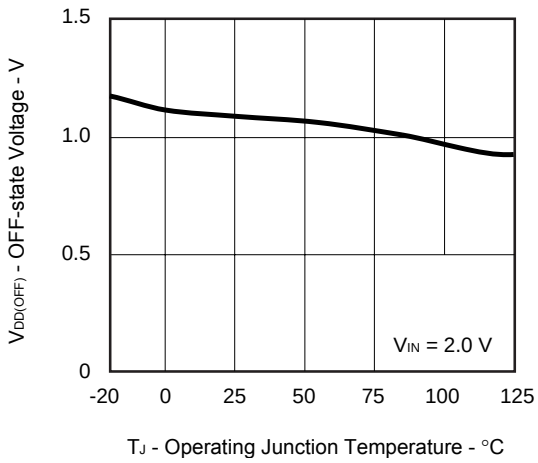
R • R vs. f



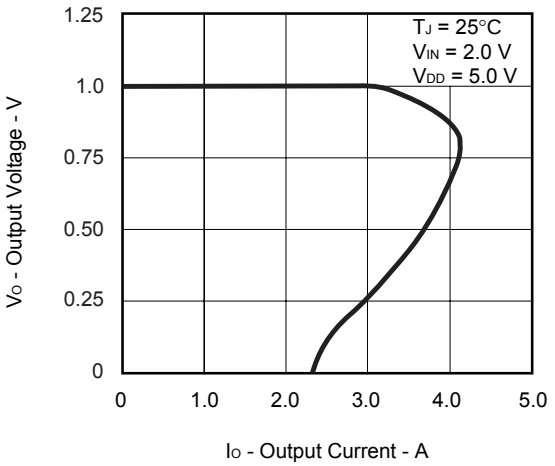
$V_{DD(ON)}$ vs. T_J



$V_{DD(OFF)}$ vs. T_J

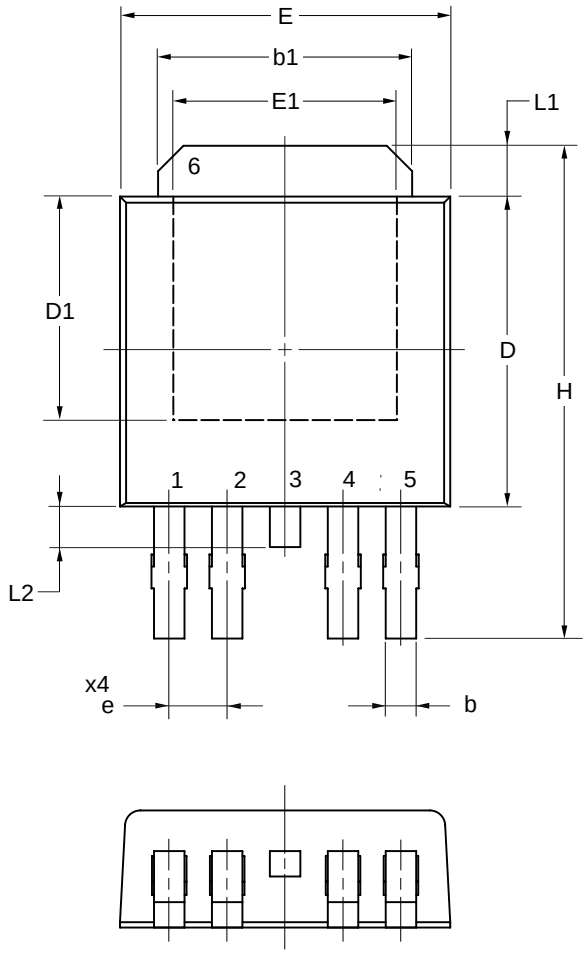


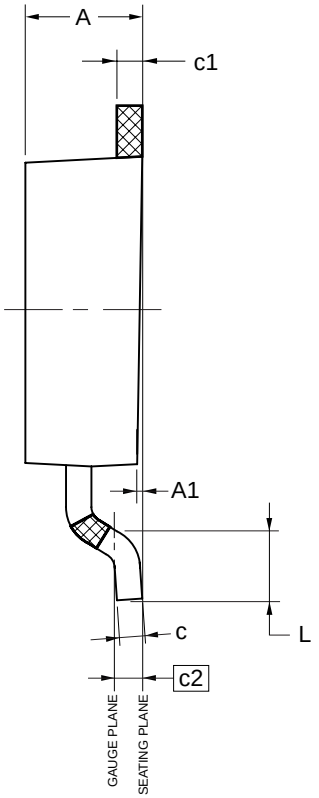
V_O vs. I_O



PACKAGE DRAWING (Unit: mm)

5-PIN TO-252 (MP-3ZK)





NOTE
1. ⊠ No Plating area

(UNIT:mm)

ITEM	DIMENSIONS
D	6.10±0.20
D1	4.4TYP(4.0MIN)
E	6.50±0.20
E1	4.4TYP(4.3MIN)
H	9.8TYP(10.3MAX)
A	2.30±0.10
A1	0 to 0.25
b	0.60±0.10
b1	5.0
c	0.50±0.10
c1	0.50±0.10
c2	0.508
e	1.14
L	1.52±0.12
L1	1.0
L2	0.80

P5T1F-114-1

RECOMMENDED MOUNTING CONDITIONS

The μPD121A10 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

μPD121A10T1F-AT [Note]: 5-PIN TO-252 (5-PIN MP-3ZK)

Process	Conditions	Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds MAX. (at 220°C or higher), Count: Three times, Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended.	IR60-00-3
Partial Heating Method	Pin temperature: 350°C or below, Heat time: 3 seconds or less (per each side of the device).	P350

Note Pb-free (This product does not contain Pb in the external electrode and other parts.)

Caution Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

REFERENCE DOCUMENTS

USER'S MANUAL USAGE OF THREE TERMINAL REGULATORS	Document No.G12702E
INFORMATION VOLTAGE REGULATOR OF SMD	Document No.G11872E
SEMICONDUCTOR DEVICE MOUNT MANUAL	http://www.necel.com/pkg/en/mount/index.html

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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