

**NEC****MOS INTEGRATED CIRCUIT**  
 **$\mu$ PD160040B****384-OUTPUT TFT-LCD SOURCE DRIVER**  
**(COMPATIBLE WITH 256-GRAY SCALE)****DESCRIPTION**

The  $\mu$ PD160040B is a source driver for TFT-LCDs capable of dealing with displays with 256-gray scale. Data input is based on digital input configured as 8 bits by 6 dots (2 pixels), which can realize a full-color display of 16,777,216 colors by output of 256 values  $\gamma$ -corrected by an internal D/A converter and 8-by-2 external power modules.

Because the output dynamic range is as large as  $V_{SS2} + 0.2$  V to  $V_{DD2} - 0.2$  V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 8-bit D/A converter circuit whose odd output pins and even output pins respectively output gray-scale voltage of differing polarity.

**FEATURES**

- CMOS level input
- 384 outputs
- Input of 8 bits (gray scale data) by 6 dots
- Capable of outputting 256 values by means of 8-by-2 external power modules (16 units) and a D/A converter
- Logic power supply voltage ( $V_{DD1}$ ): 2.5 to 3.6 V
- Driver power supply voltage ( $V_{DD2}$ ): 12.5 to 15.5 V (switchable,  $V_{SEL}$ )
- Output dynamic range:  $V_{SS2} + 0.2$  V to  $V_{DD2} - 0.2$  V
- High-speed data transfer:  $f_{CLK} = 55$  MHz MAX. (internal data transfer speed when operating at  $3.0$  V  $\leq V_{DD1} \leq 3.6$  V)  
 $f_{CLK} = 40$  MHz MAX. (internal data transfer speed when operating at  $2.5$  V  $\leq V_{DD1} < 3.0$  V)
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output voltage polarity inversion function (POL)
- Output inversion function (POL21, POL 22)
- Output reset control is possible (MODE)
- Trough-rate control is possible (SRC)
- Output resistance control is possible (ORC)
- Single bank arrangement is possible (Loaded with slim TCP)

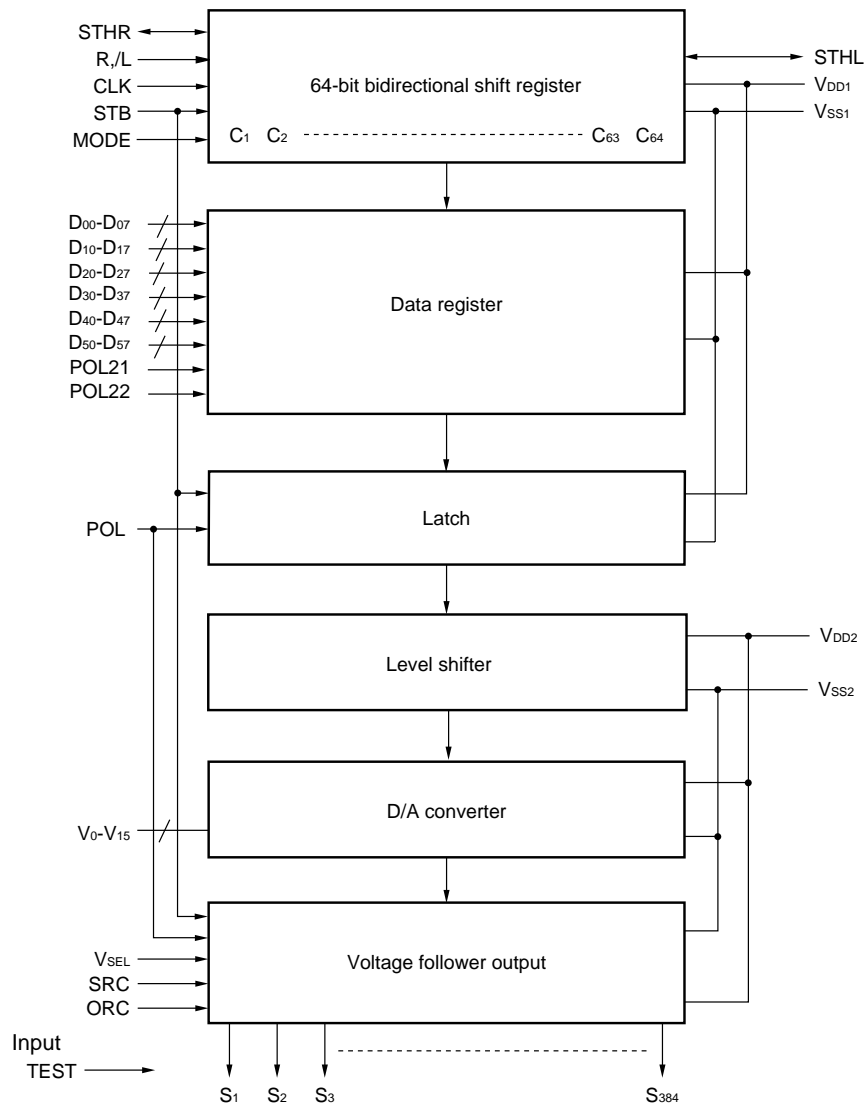
**ORDERING INFORMATION**

Part Number	Package
$\mu$ PD160040BN-xxx	TCP (TAB package)

**Remark** The TCP's external shape is customized. To order the required shape, so please contact one of our sales representatives.

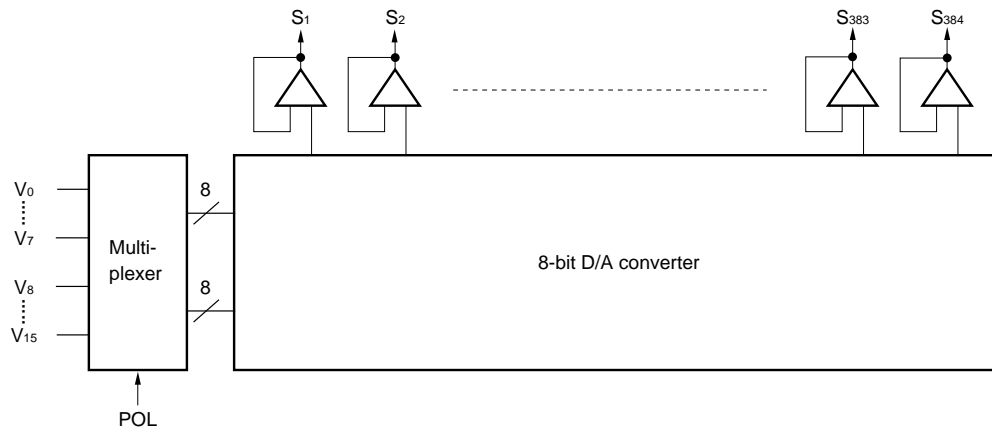
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1. BLOCK DIAGRAM

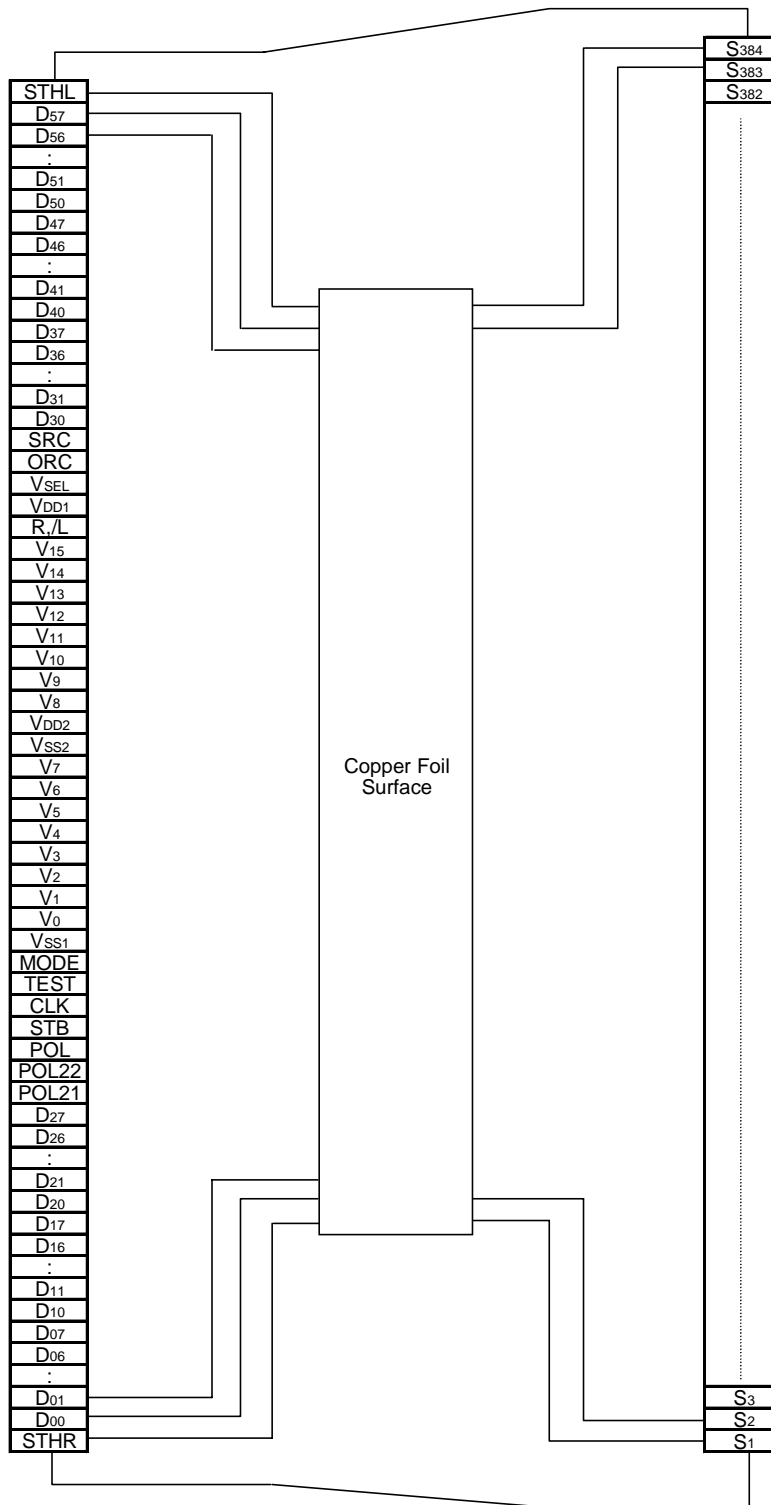


Remark /xxx indicates active low signal.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD160040BN-xxx) (Copper Foil Surface, Face-up)



**Remark** This figure does not specify the TCP package.

4. PIN FUNCTIONS

Pin Symbol	Pin Name	I/O	Description
S <sub>1</sub> to S <sub>384</sub>	Driver	Output	The D/A converted 256-gray-scale analog voltage is output.
D <sub>00</sub> to D <sub>07</sub>	Port 1 display data	Input	The display data is input with a width of 48 bits, viz., the gray scale data (8 bits) by 6 dots (2 pixels). D <sub>x0</sub> : LSB, D <sub>x7</sub> : MSB
D <sub>10</sub> to D <sub>17</sub>			
D <sub>20</sub> to D <sub>27</sub>			
D <sub>30</sub> to D <sub>37</sub>	Port 2 display data	Input	
D <sub>40</sub> to D <sub>47</sub>			
D <sub>50</sub> to D <sub>57</sub>			
R,/L	Shift direction control	Input	The shift direction control pin of shift register. The shift directions of the shift registers are as follows. R,/L = H (right shift): STHR (input) → S <sub>1</sub> → S <sub>384</sub> → STHL (output) R,/L = L (left shift) : STHL (input) → S <sub>384</sub> → S <sub>1</sub> → STHR (output)
★ STHR	Right shift start pulse	I/O	These are the start pulse input/output pins when connected in cascade. Loading of display data starts when a H level is read at the rising edge of CLK. A H level should be input at the pulse of one cycle of the clock signal.
★ STHL	Left shift start pulse	I/O	If the start pulse input is more than 2 CLK, the first 1 CLK of the H-level input is valid. For right shift, STHR is input and STHL is output. For left shift, STHL is input and STHR is output.
CLK	Shift clock	Input	The shift clock input pin of shift register. The display data is loaded into the data register at the rising edge. When 66 clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch	Input	The contents of the data register are transferred to the latch circuit at the rising edge. In addition, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
SRC	Through rate control	Input	SRC = H: High through rate mode (large current consumption) SRC = L: Low through rate mode (small current consumption) SRC is pulled up to the V <sub>DD1</sub> in the IC.
ORC	Output resistance control	Input	ORC = H: Low output resistance mode ORC = L: High output resistance mode ORC is pulled up to the V <sub>DD1</sub> in the IC.
POL	Polarity input	Input	POL = L: The S <sub>2n-1</sub> output uses V <sub>0</sub> -V <sub>7</sub> as the reference supply. The S <sub>2n</sub> output uses V <sub>8</sub> -V <sub>15</sub> as the reference supply. POL = H: The S <sub>2n-1</sub> output uses V <sub>8</sub> -V <sub>15</sub> as the reference supply. The S <sub>2n</sub> output uses V <sub>0</sub> -V <sub>7</sub> as the reference supply. S <sub>2n-1</sub> indicates the odd output and S <sub>2n</sub> indicates the even output. Input of the POL signal is allowed the setup time (t <sub>POL-STB</sub> ) with respect to STB's rising edge. When it switches such as POL = H → L or L → H, all output pins are output reset during STB = H. When it does not switch, all output pins become Hi-Z (high impedance) during STB = H. Refer to 7. <b>RELATIONSHIP BETWEEN MODE, STB, SRC, ORC, POL, AND OUTPUT WAVEFORM</b> for details.

Pin Symbol	Pin Name	I/O	Description
MODE	Output reset control	Input	MODE = H or open: Output reset MODE = L: No output reset MODE is pulled up to the V <sub>DD1</sub> in the IC.
POL21, POL22	Data inversion	Input	Select of inversion or no inversion for input data. POL21: Data inversion or no inversion of Port1. POL22: Data inversion or no inversion of Port2 POL21, POL22 = H: Data are inverted in the IC. POL21, POL22 = L: Data are not inverted in the IC.
V <sub>SEL</sub>	Driver voltage select	Input	The driver voltage can be switched by controlling the stationary bias current of the output amplifier via V <sub>SEL</sub> . V <sub>SEL</sub> = H: V <sub>DD2</sub> = 12.5 to (14.0 V) (large bias current) V <sub>SEL</sub> = L or open: V <sub>DD2</sub> = (14.0 V) to 15.5 V (small bias current) LPC is pulled down to the V <sub>SS1</sub> in the IC.
V <sub>0</sub> -V <sub>15</sub>	γ-corrected power supplies	–	Input the γ-corrected power supplies from outside by using operational amplifier. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. Make sure to maintain the following relationships. $V_{DD2} - 0.2\text{ V} \geq V_0 > V_1 > V_2 > \dots \dots, > V_6 > V_7 \geq 0.5 V_{DD2} + 0.5\text{ V}$ $0.5 V_{DD2} - 0.5\text{ V} \geq V_8 > V_9 > V_{10} > \dots \dots, > V_{14} > V_{15} \geq 0.5 V_{SS2} + 0.2\text{ V}$
TEST	Test	Input	Normally, set the TEST pin to H level or leave open. This pin is pulled up to V <sub>DD1</sub> in the IC.
V <sub>DD1</sub>	Logic power supply	–	2.5 to 3.6 V
V <sub>DD2</sub>	Driver power supply	–	12.5 to 15.5 V
V <sub>SS1</sub>	Logic ground	–	Grounding
V <sub>SS2</sub>	Driver ground	–	Grounding

- Cautions 1. The power start sequence must be V<sub>DD1</sub>, logic input, and V<sub>DD2</sub> & V<sub>0</sub>-V<sub>15</sub> in that order. Reverse this sequence to shut down.**
- 2. To stabilize the supply voltage, please be sure to insert a 0.47 μF bypass capacitor between V<sub>DD1</sub>-V<sub>SS1</sub> and V<sub>DD2</sub>-V<sub>SS2</sub>. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.1 μF is also advised between the γ-corrected power supply terminals (V<sub>0</sub>, V<sub>1</sub>, V<sub>2</sub>,....., V<sub>15</sub>) and V<sub>SS2</sub>.**

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The μPD160040B incorporates a 8-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode voltage. The D/A converter consists of ladder resistors and switches.

The ladder resistors ( $r_0$  to  $r_{254}$ ) are designed so that the ratio of LCD panel ( $\gamma$ -compensated voltages to  $V_0'-V_{255}'$  and  $V_0''-V_{255}''$ ) is almost equivalent as shown in Figure 5-2. For the 2 sets of eight  $\gamma$ -compensated power supplies,  $V_0-V_7$  and  $V_8-V_{15}$ , respectively, input gray scale voltages of the same polarity with respect to the  $0.5 V_{DD2}$ .

Figure 5-1 shows the relationship between the driving voltages such as liquid-crystal driving voltages  $V_{DD2}$ ,  $V_{SS2}$  and  $0.5 V_{DD2}$ , and  $\gamma$ -corrected voltages  $V_0-V_{15}$  and the input data. Be sure to maintain the voltage relationships below.

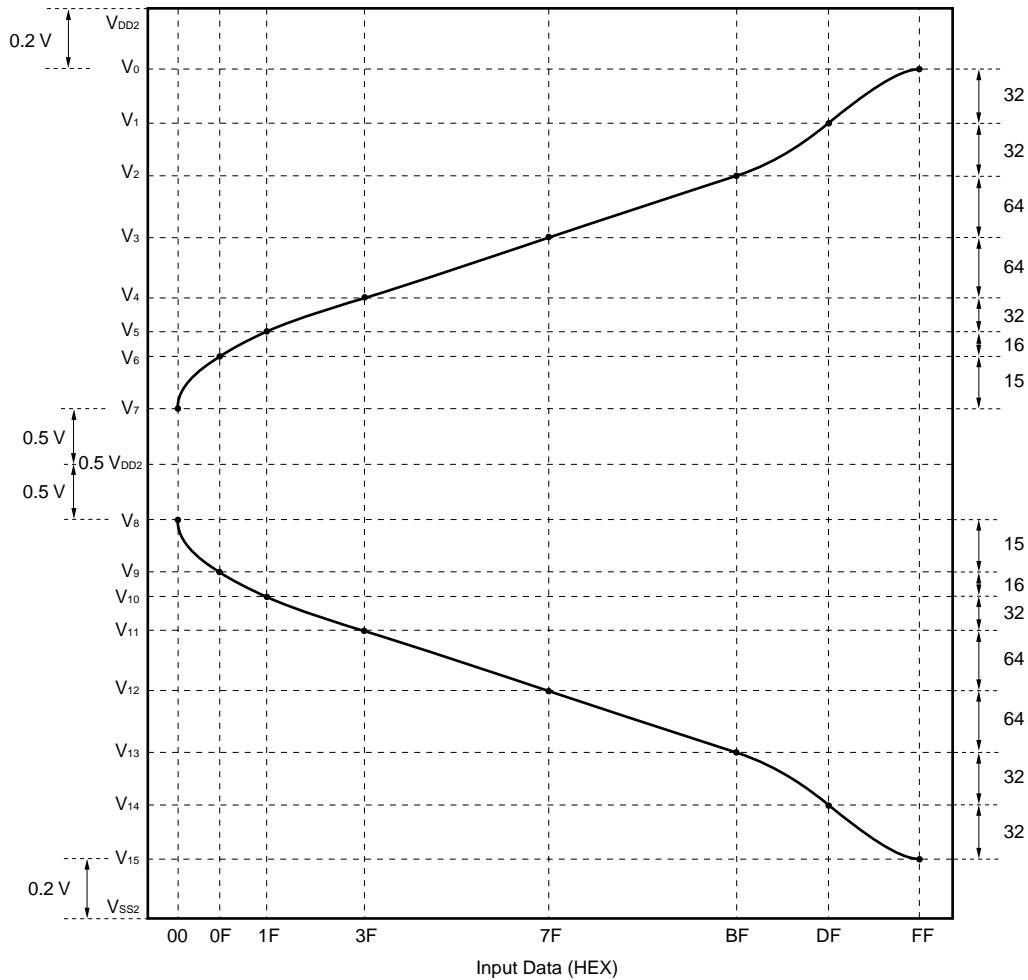
$$V_{DD2} - 0.2 V \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 \geq 0.5 V_{DD2} + 0.5 V$$

$$0.5 V_{DD2} - 0.5 V \geq V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} \geq 0.5 V_{SS2} + 0.2 V$$

Figures 5-2 and 5-3 show the relation ship between the input data and the output voltage and the resistance values of the resistor strings.

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Figure 5-1. Relationship between Input Data and  $\gamma$ -corrected Power Supplies











6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 8 bits x 2 RGBs (6 dots)

Input width: 48 bits (2-pixel data)

(1) R,/L = H (right shift)

Output	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	...	S <sub>383</sub>	S <sub>384</sub>
Data	D <sub>00</sub> to D <sub>07</sub>	D <sub>10</sub> to D <sub>17</sub>	D <sub>20</sub> to D <sub>27</sub>	D <sub>30</sub> to D <sub>37</sub>	...	D <sub>40</sub> to D <sub>47</sub>	D <sub>50</sub> to D <sub>57</sub>

(2) R,/L = L (left shift)

Output	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	...	S <sub>383</sub>	S <sub>384</sub>
Data	D <sub>00</sub> to D <sub>07</sub>	D <sub>10</sub> to D <sub>17</sub>	D <sub>20</sub> to D <sub>27</sub>	D <sub>30</sub> to D <sub>37</sub>	...	D <sub>40</sub> to D <sub>47</sub>	D <sub>50</sub> to D <sub>57</sub>

POL	S <sub>2n-1</sub> <sup>Note</sup>	S <sub>2n</sub> <sup>Note</sup>
L	V <sub>0</sub> -V <sub>7</sub>	V <sub>8</sub> -V <sub>15</sub>
H	V <sub>8</sub> -V <sub>15</sub>	V <sub>0</sub> -V <sub>7</sub>

**Note** S<sub>2n-1</sub> (odd output), S<sub>2n</sub> (even output), n = 1, 2, ..., 192.

7. RELATIONSHIP BETWEEN MODE, STB, SRC, ORC, POL, AND OUTPUT WAVEFORM

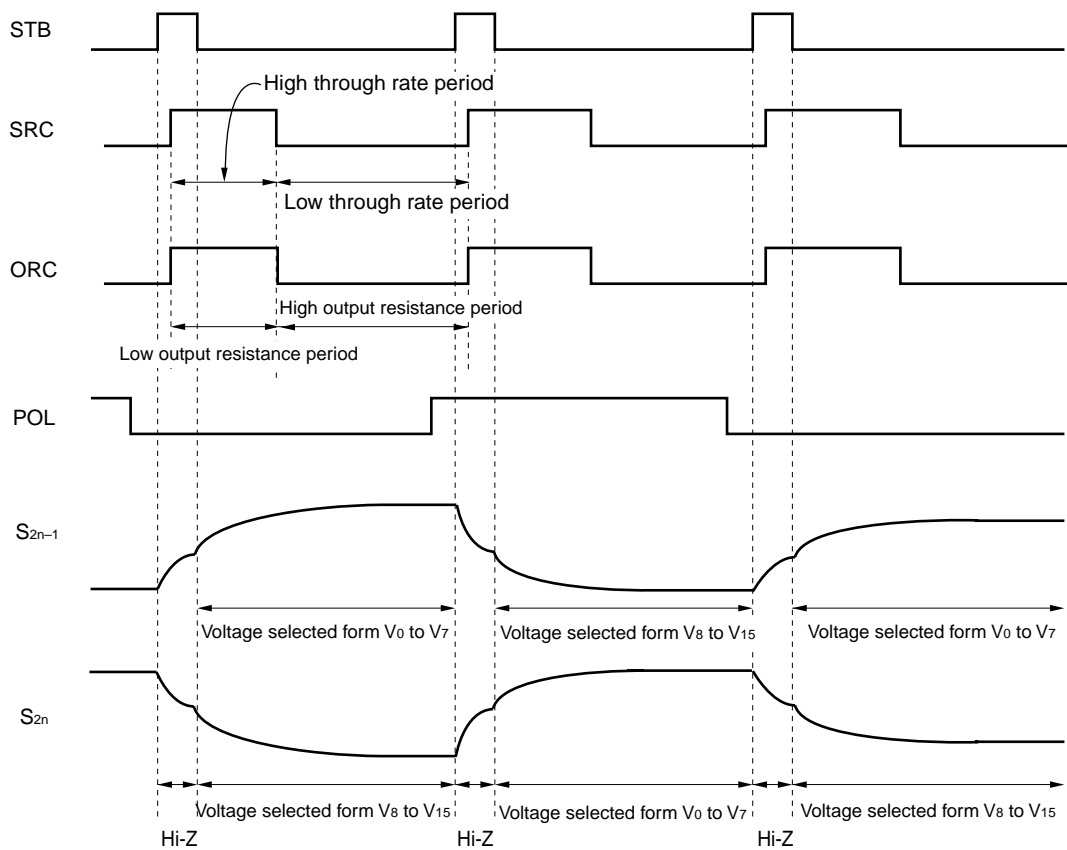
When MODE = H or open and STB = H, all outputs are reset (short) and the gray-scale voltage is output to LCD in synchronization with the falling edge of STB.

When MODE = L and STB = H, all outputs became Hi-Z and the gray-scale voltage is output to the LCD in synchronization with the falling edge of STB.

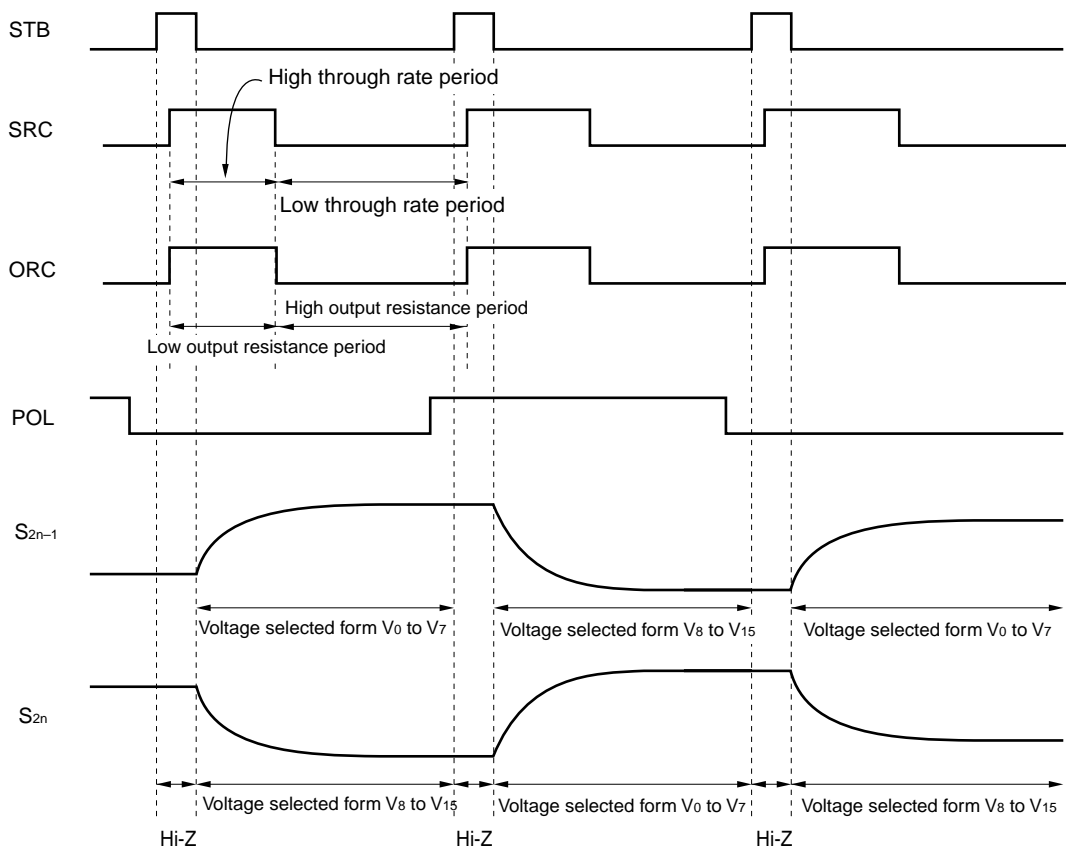
Also, setting the SRC pin to H level allows the bias current value of the output amplifier to rise temporarily, and setting the ORC pin to H level allows the output resistance value of the amplifier to lower temporarily.

For the timing and the processing of STB, SRC, or ORC during a high-level period, We recommend a thorough evaluation of the LCD panel specifications in advance.

(1) MODE = H or open



(2) MODE = L



8. ELECTRICAL SPECIFICATIONS

**Absolute Maximum Ratings (T<sub>A</sub> = 25°C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	Ratings	Unit
Logic part supply voltage	V <sub>DD1</sub>	-0.5 to + 4.0	V
Driver part supply voltage	V <sub>DD2</sub>	-0.5 to + 17.0	V
Logic part input voltage	V <sub>I1</sub>	-0.5 to V <sub>DD1</sub> + 0.5	V
Driver part input voltage	V <sub>I2</sub>	-0.5 to V <sub>DD2</sub> + 0.5	V
Logic part output voltage	V <sub>O1</sub>	-0.5 to V <sub>DD1</sub> + 0.5	V
Driver part output voltage	V <sub>O2</sub>	-0.5 to V <sub>DD2</sub> + 0.5	V
Operating ambient temperature	T <sub>A</sub>	-10 to + 75	°C
Storage temperature	T <sub>stg</sub>	-55 to + 125	°C

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Recommended Operating Range (T<sub>A</sub> = -10 to +75°C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic part supply voltage	V <sub>DD1</sub>		2.5		3.6	V
Driver part supply voltage	V <sub>DD2</sub>	V <sub>SEL</sub> = H	12.5	13.0	(14.0)	V
		V <sub>SEL</sub> = L or open	(14.0)	15.0	15.5	V
High-level input voltage	V <sub>IH</sub>		0.7 V <sub>DD1</sub>		V <sub>DD1</sub>	V
Low-level input voltage	V <sub>IL</sub>		0		0.3 V <sub>DD1</sub>	V
γ-corrected voltage	V <sub>0</sub> -V <sub>7</sub>		0.5 V <sub>DD2</sub> + 0.5		V <sub>DD2</sub> - 0.2	V
	V <sub>8</sub> -V <sub>15</sub>		0.2		0.5 V <sub>DD2</sub> - 0.5	V
Driver part output voltage	V <sub>O</sub>		0.2		V <sub>DD2</sub> - 0.2	V
Clock frequency	f <sub>CLK</sub>	3.0 V ≤ V <sub>DD1</sub> ≤ 3.6 V			55	MHz
		2.5 V ≤ V <sub>DD1</sub> < 3.0 V			40	MHz

**Remark** The value enclosed in parentheses is a reference value.

**Electrical Characteristics (TA = -10 to +75°C, VDD1 = 2.5 to 3.6 V, VDD2 = 12.5 to 15.5 V, VSS1 = VSS2 = 0 V)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input leakage current	IIL				±1.0	μA
High-level output voltage	VOH	STHR (STHL), IOH = 0 mA	VDD1 - 0.1			V
Low-level output voltage	VOL	STHR (STHL), IOL = 0 mA			0.1	V
γ-corrected resistance	Rγ	VDD2 = 15.0 V, V0-V7 = V8-V15 = 7.0 V	6.5	13.0	19.5	kΩ
Driver output current	I <sub>VOH</sub>	V <sub>X</sub> = 12.0 V, V <sub>OUT</sub> = 11.0 V <sup>Note1</sup>			-0.40	mA
	I <sub>VOL</sub>	V <sub>X</sub> = 1.0 V, V <sub>OUT</sub> = 2.0 V <sup>Note1</sup>	0.65			mA
Output voltage deviation	ΔV <sub>O</sub>	T <sub>A</sub> = 25°C, V <sub>SS2</sub> + 1.0 V to V <sub>DD2</sub> - 1.0 V		±10	±20	mV
Output swing voltage difference deviation	ΔV <sub>P-P1</sub>	V <sub>DD1</sub> = 3.3 V, V <sub>OUT</sub> = 7.0 to 8.0 V <sup>Note1</sup>		±5	±10	mV
	ΔV <sub>P-P2</sub>	V <sub>DD2</sub> = 15.0 V, V <sub>OUT</sub> = 4.0 to 11.0 V <sup>Note1</sup>		±7	±15	mV
	ΔV <sub>P-P3</sub>	T <sub>A</sub> = 25°C, V <sub>OUT</sub> = 1.0 to 14.0 V <sup>Note1</sup>		±10	±20	mV
Logic part dynamic current consumption	I <sub>DD1</sub>	V <sub>DD1</sub> <sup>Notes 2, 3</sup>		1.3	12	mA
Driver part dynamic current consumption	I <sub>DD2</sub>	V <sub>DD2</sub> , with no load <sup>Notes 3, 4</sup>		12	30	mA

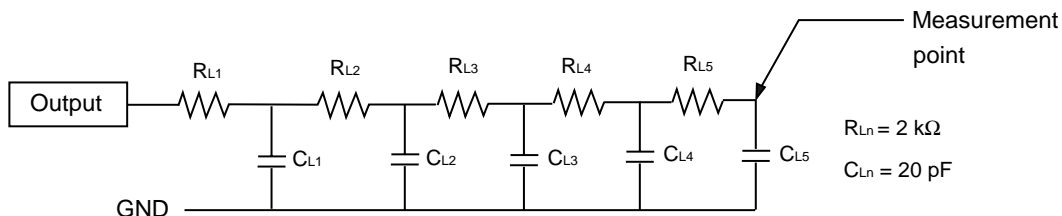
- Notes 1.** V<sub>X</sub> refers to the output voltage of analog output pins S<sub>1</sub> to S<sub>384</sub>.  
V<sub>OUT</sub> refers to the voltage applied to analog output pins S<sub>1</sub> to S<sub>384</sub>
- f<sub>STB</sub> = 64 kHz, f<sub>CLK</sub> = 54 MHz
  - The TYP. values refer to an all black or all white input pattern. The MAX. Value refers to the measured values in the dot checkerboard input pattern.
  - Refers to the current consumption per driver when cascades are connected under the assumption of SXGA single-sided mounting (10 units).

**Switching Characteristics (TA = -10 to +75°C, VDD1 = 2.5 to 3.6 V, VDD2 = 12.5 to 15.5 V, VSS1 = VSS2 = 0 V)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start pulse delay time	t <sub>PLH1</sub>	C <sub>L</sub> = 15 pF, 3.0 V ≤ V <sub>DD1</sub> ≤ 3.6 V			17	ns
		C <sub>L</sub> = 15 pF, 2.5 V ≤ V <sub>DD1</sub> < 3.0 V			24	ns
Driver output delay time	t <sub>PLH2</sub> <sup>Note</sup>	C <sub>L</sub> = 100 pF, R <sub>L</sub> = 10 kΩ			5	μs
	t <sub>PLH3</sub> <sup>Note</sup>				10	μs
	t <sub>PHL2</sub> <sup>Note</sup>				5	μs
	t <sub>PHL3</sub> <sup>Note</sup>				10	μs
Input capacitance	C <sub>I1</sub>	logic input, except STHR (STHL), T <sub>A</sub> = 25°C		5	10	pF
	C <sub>I2</sub>	STHR (STHL), T <sub>A</sub> = 25°C		10	15	pF

**Note** t<sub>PLH2</sub>, t<sub>PHL2</sub> refer to the arrival time from falling edge of STB to target voltage ±10%  
t<sub>PLH3</sub>, t<sub>PHL3</sub> refer to the arrival time from falling edge of STB to target voltage ±0.02 V (condition: V<sub>O</sub> = 3.0 V ↔ 12.0 V)

★ <Test Condition>



Timing Requirements (T<sub>A</sub> = -10 to +75°C, V<sub>DD1</sub> = 2.5 to 3.6 V, V<sub>SS1</sub> = 0 V, t<sub>r</sub> = t<sub>f</sub> = 5.0 ns)

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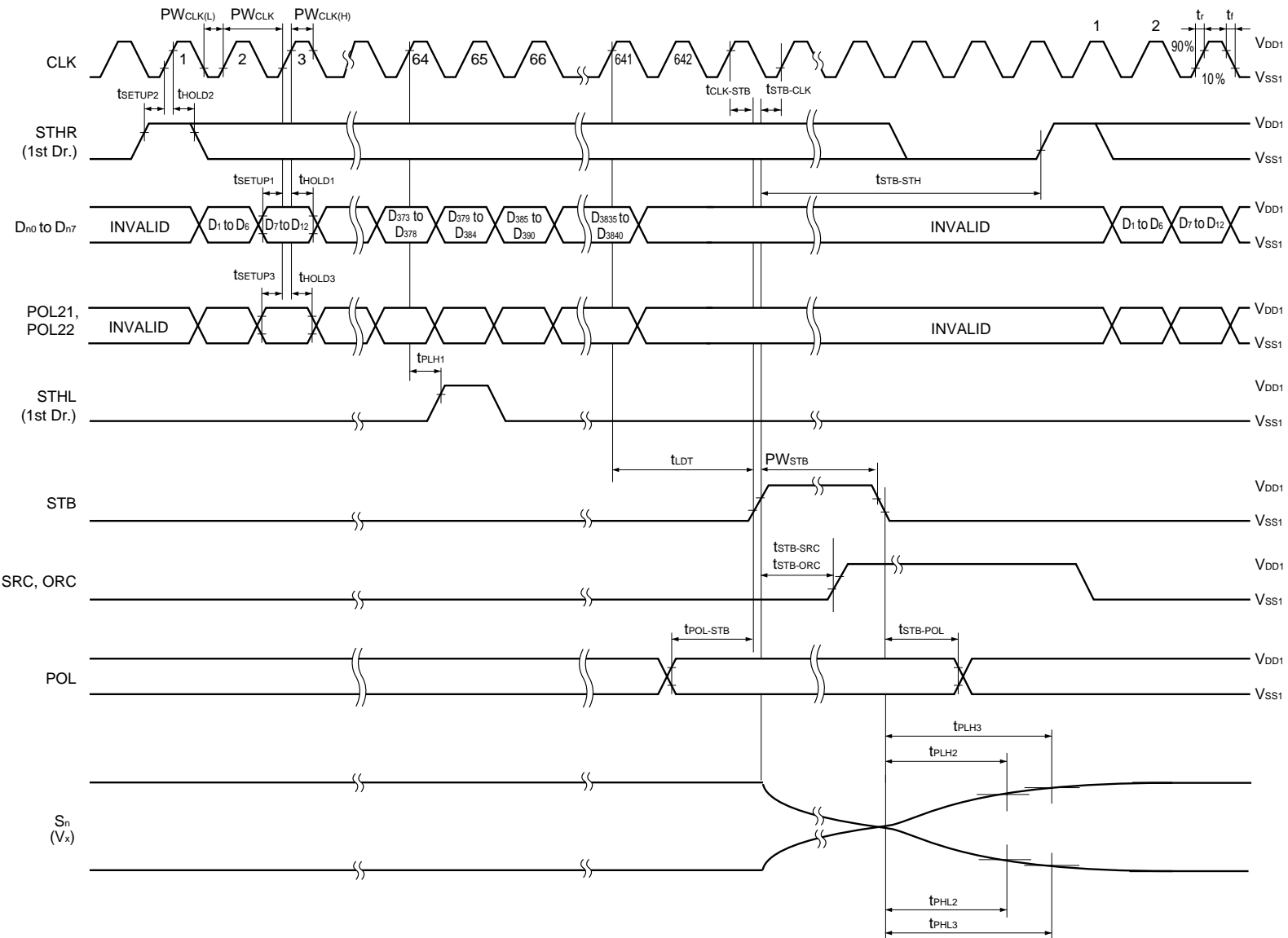
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	PW <sub>CLK</sub>	3.0 V ≤ V <sub>DD1</sub> ≤ 3.6 V	18			ns
		2.5 V ≤ V <sub>DD1</sub> < 3.0 V	25			ns
Clock pulse high period	PW <sub>CLK (H)</sub>	3.0 V ≤ V <sub>DD1</sub> ≤ 3.6 V	4			ns
		2.5 V ≤ V <sub>DD1</sub> < 3.0 V	6			ns
Clock pulse low period	PW <sub>CLK (L)</sub>		4			ns
Data setup time	t <sub>SETUP1</sub>		0			ns
Data hold time	t <sub>HOLD1</sub>		4			ns
Start pulse setup time	t <sub>SETUP2</sub>		0			ns
Start pulse hold time	t <sub>HOLD2</sub>		4			ns
POL21, POL22 setup time	t <sub>SETUP3</sub>		0			ns
POL21, POL22 hold time	t <sub>HOLD3</sub>		4			ns
STB pulse width	PW <sub>STB</sub>		1.0			μs
Last data timing	t <sub>LDT</sub>		2			CLK
CLK-STB time	t <sub>CLK-STB</sub>	CLK ↑ → STB ↑	4			ns
STB-CLK time	t <sub>STB-CLK</sub>	STB ↑ → CLK ↑	4			ns
Time between STB and start pulse	t <sub>STB-STH</sub>	STB ↑ → STHR (STHL) ↑	2			CLK
POL-STB time	t <sub>POL-STB</sub>	POL ↑ or ↓ → STB ↑	4			ns
STB-POL time	t <sub>STB-POL</sub>	STB ↓ → POL ↓ or ↑	4			ns
STB-SRC time	t <sub>STB-SRC</sub>	STB ↑ → SRC ↑	0			ns
★ STB-ORC time	t <sub>STB-ORC</sub>	STB ↑ → ORC ↑	0			ns

**Remark** Unless otherwise specified, the input level is defined to be V<sub>IH</sub> = 0.7 V<sub>DD1</sub>, V<sub>IL</sub> = 0.3 V<sub>DD1</sub>.

Switching Characteristic Waveform

(1) R/L=H, MODE = H or open

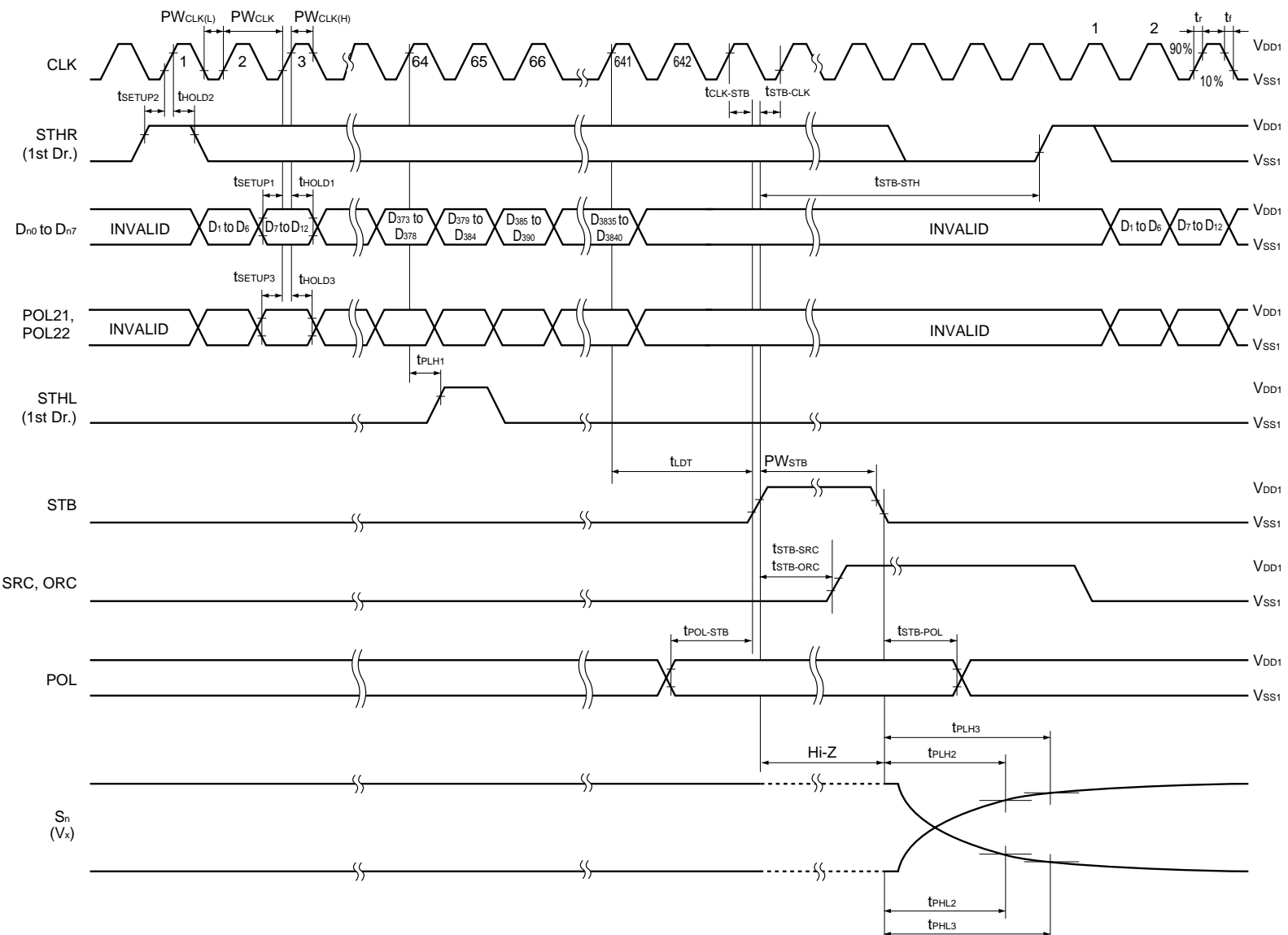
Unless otherwise specified,  $V_{IH}$ ,  $V_{IL}$  are defined to be  $V_{IH} = 0.7 V_{DD1}$ ,  $V_{IL} = 0.3 V_{DD1}$  (numbers clock and display data are example when in SXGA).





(2) R/L= H, MODE = L

Unless otherwise specified,  $V_{IH}$ ,  $V_{IL}$  are defined to be  $V_{IH} = 0.7 V_{DD1}$ ,  $V_{IL} = 0.3 V_{DD1}$  (Numbers clock and display data are example when in SXGA).



**9. RECOMMENDED MOUNTING CONDITIONS**

The following conditions must be met for mounting conditions of the μPD160040B.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD160040BN-xxx: TCP (TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 sec, pressure 100g (per solder).
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C, pressure 3 to 8 kg/cm <sup>2</sup> , time 3 to 5 sec. Real bonding 165 to 180°C pressure 25 to 45 kg/cm <sup>2</sup> , time 30 to 40 sec. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

**Caution** To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.