RENESAS

MOS INTEGRATED CIRCUIT

μPD161602A/B

360/396-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

DESCRIPTION

The μPD161602A/B is a source driver for TFT-LCDs supporting 64 gray-scale display and can operate with a supply voltage of 2.5 V for the logic block and 5.0 V for the driver block. Data input as 6-bit x 3-dot digital data is output as 64 γ-corrected values using an internal D/A converter and 5 external power modules, thus achieving a 260,000-color (full-color) display. In addition, the difference with A articles and B articles is only a difference in γ compensation resistance.

FEATURES

- CMOS level input
- 360/396 outputs
- Input of 6 bits (gray-scale data) by 3 dots
- Capable of outputting 64 values by means of 5 external power modules and a D/A converter
- Output dynamic range: V_{SS2} to V_{DD2}
- High-speed data transfer: f_{CLK} = 15 MHz MAX. (internal data transfer speed when operating at V_{DD1} = 2.5 V)
- Level inversion γ-correction power supply is possible
- Logic power supply voltage (V_{DD1}): 2.2 to 3.6 V
- Driver power supply voltage (V_{DD2}): 4.5 to 5.5 V

★ ORDERING INFORMATION

Part Number	Package
μPD161602AP	Chip
μPD161602BP	Chip

Remark Purchasing the above chip entail the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representatives.

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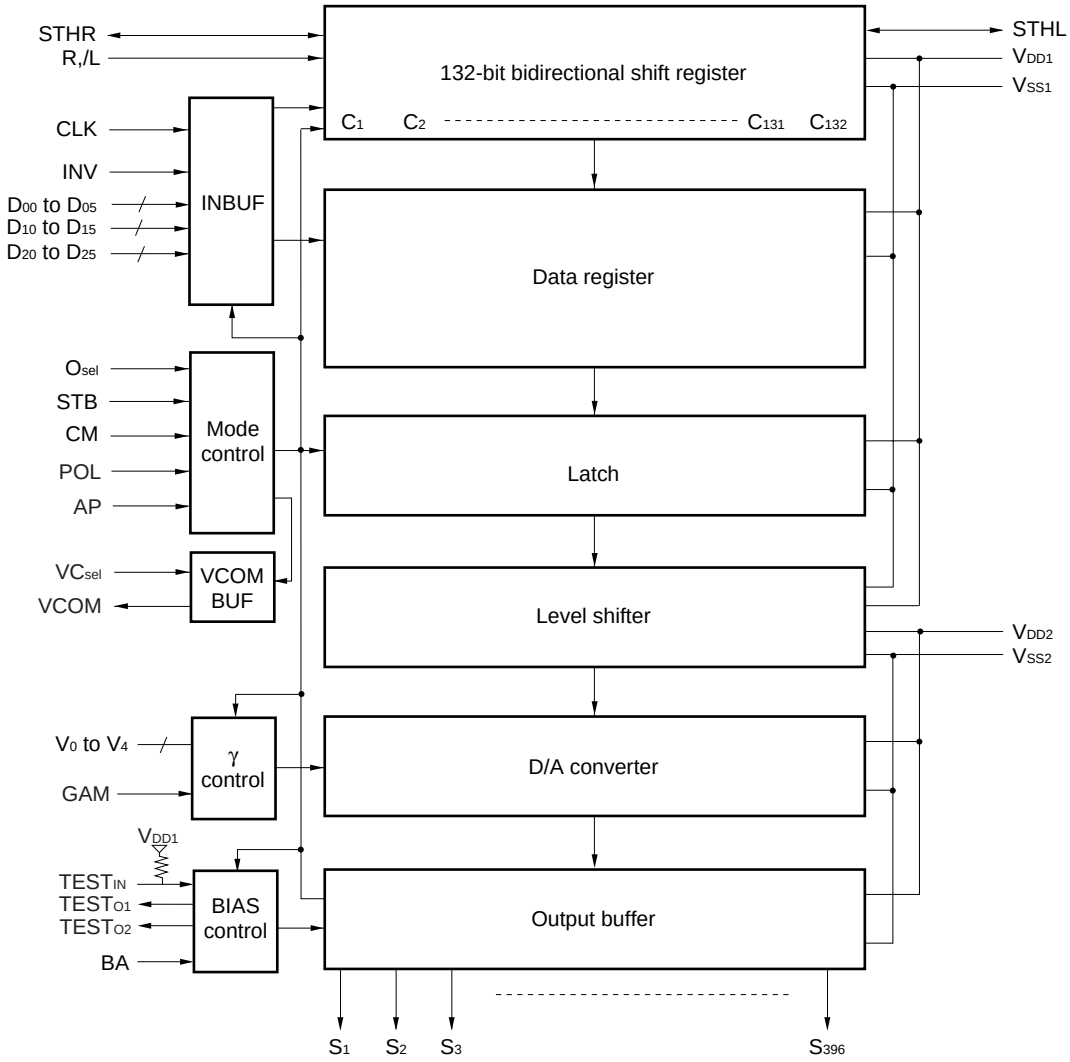
The mark ★ shows major revised points.

★ 1. BLOCK DIAGRAM



★ **Remark** /xxx indicates active low signal.

2. PIN CONFIGURATION (Pad Layout)

Chip size: 16980 x 1620 μm^2

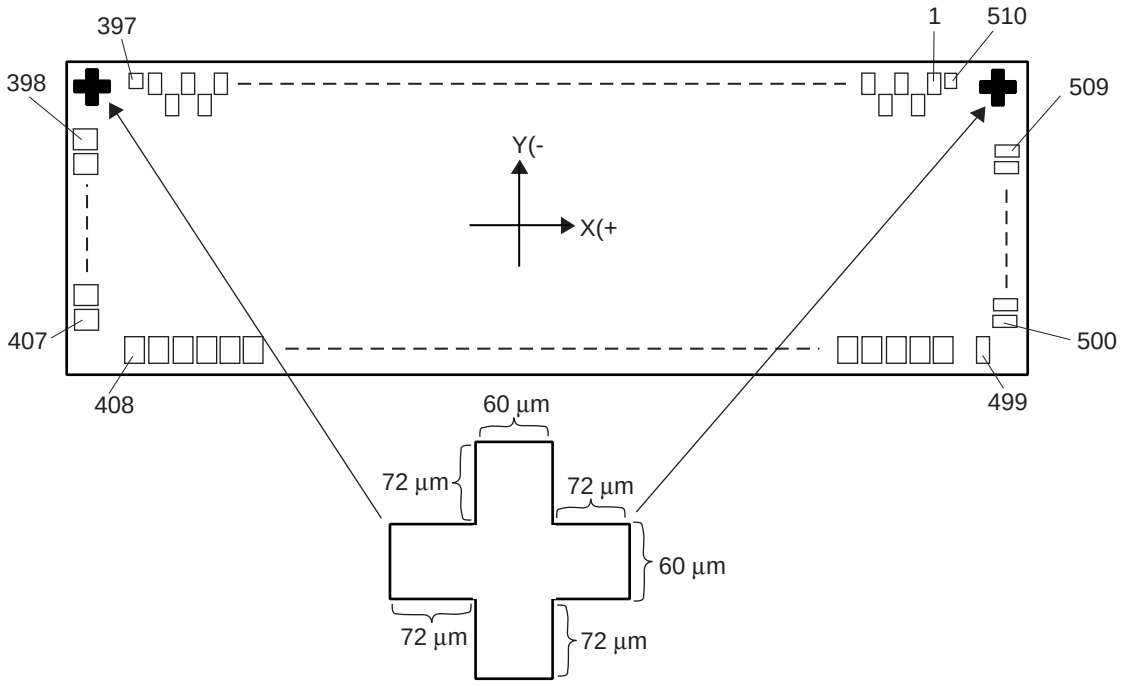
Bump size (Input/VCOM/test/dummy): 86 x 80 μm^2

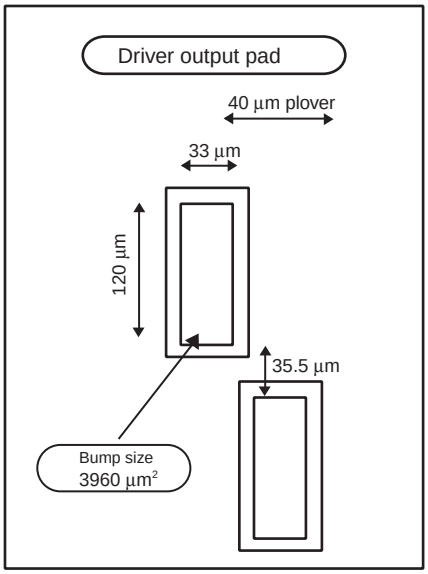
Bump size (Output): 33 x 120 μm^2

Alignment Mark (μm)

X: –8284.4 Y: 600

X: 8284.4 Y: 600





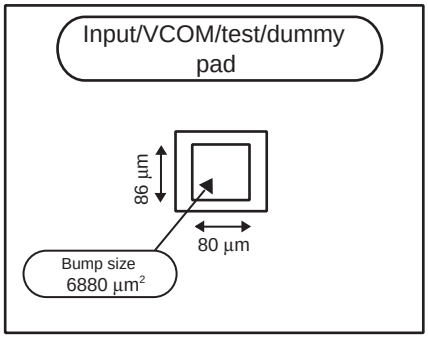


Table 2–1. Pad Layout (1/3)

No.	Pad Name	X [μm]	Y [μm]
1	S1	7900.0	667.7
2	S2	7860.0	512.2
3	S3	7820.0	667.7
4	S4	7780.0	512.2
5	S5	7740.0	667.7
6	S6	7700.0	512.2
7	S7	7660.0	667.7
8	S8	7620.0	512.2
9	S9	7580.0	667.7
10	S10	7540.0	512.2
11	S11	7500.0	667.7
12	S12	7460.0	512.2
13	S13	7420.0	667.7
14	S14	7380.0	512.2
15	S15	7340.0	667.7
16	S16	7300.0	512.2
17	S17	7260.0	667.7
18	S18	7220.0	512.2
19	S19	7180.0	667.7
20	S20	7140.0	512.2
21	S21	7100.0	667.7
22	S22	7060.0	512.2
23	S23	7020.0	667.7
24	S24	6980.0	512.2
25	S25	6940.0	667.7
26	S26	6900.0	512.2
27	S27	6860.0	667.7
28	S28	6820.0	512.2
29	S29	6780.0	667.7
30	S30	6740.0	512.2
31	S31	6700.0	667.7
32	S32	6660.0	512.2
33	S33	6620.0	667.7
34	S34	6580.0	512.2
35	S35	6540.0	667.7
36	S36	6500.0	512.2
37	S37	6460.0	667.7
38	S38	6420.0	512.2
39	S39	6380.0	667.7
40	S40	6340.0	512.2
41	S41	6300.0	667.7
42	S42	6260.0	512.2
43	S43	6220.0	667.7
44	S44	6180.0	512.2
45	S45	6140.0	667.7
46	S46	6100.0	512.2
47	S47	6060.0	667.7
48	S48	6020.0	512.2
49	S49	5980.0	667.7
50	S50	5940.0	512.2
51	S51	5900.0	667.7
52	S52	5860.0	512.2
53	S53	5820.0	667.7
54	S54	5780.0	512.2
55	S55	5740.0	667.7
56	S56	5700.0	512.2
57	S57	5660.0	667.7
58	S58	5620.0	512.2
59	S59	5580.0	667.7
60	S60	5540.0	512.2
61	S61	5500.0	667.7
62	S62	5460.0	512.2
63	S63	5420.0	667.7
64	S64	5380.0	512.2
65	S65	5340.0	667.7
66	S66	5300.0	512.2
67	S67	5260.0	667.7
68	S68	5220.0	512.2
69	S69	5180.0	667.7
70	S70	5140.0	512.2
71	S71	5100.0	667.7
72	S72	5060.0	512.2
73	S73	5020.0	667.7
74	S74	4980.0	512.2
75	S75	4940.0	667.7
76	S76	4900.0	512.2
77	S77	4860.0	667.7
78	S78	4820.0	512.2
79	S79	4780.0	667.7
80	S80	4740.0	512.2
81	S81	4700.0	667.7
82	S82	4660.0	512.2
83	S83	4620.0	667.7
84	S84	4580.0	512.2
85	S85	4540.0	667.7
86	S86	4500.0	512.2
87	S87	4460.0	667.7
88	S88	4420.0	512.2
89	S89	4380.0	667.7
90	S90	4340.0	512.2
91	S91	4300.0	667.7
92	S92	4260.0	512.2
93	S93	4220.0	667.7
94	S94	4180.0	512.2
95	S95	4140.0	667.7
96	S96	4100.0	512.2
97	S97	4060.0	667.7
98	S98	4020.0	512.2
99	S99	3980.0	667.7
100	S100	3940.0	512.2
101	S101	3900.0	667.7
102	S102	3860.0	512.2
103	S103	3820.0	667.7
104	S104	3780.0	512.2
105	S105	3740.0	667.7
106	S106	3700.0	512.2
107	S107	3660.0	667.7
108	S108	3620.0	512.2
109	S109	3580.0	667.7
110	S110	3540.0	512.2
111	S111	3500.0	667.7
112	S112	3460.0	512.2
113	S113	3420.0	667.7
114	S114	3380.0	512.2
115	S115	3340.0	667.7
116	S116	3300.0	512.2
117	S117	3260.0	667.7
118	S118	3220.0	512.2
119	S119	3180.0	667.7
120	S120	3140.0	512.2
121	S121	3100.0	667.7
122	S122	3060.0	512.2
123	S123	3020.0	667.7
124	S124	2980.0	512.2
125	S125	2940.0	667.7
126	S126	2900.0	512.2
127	S127	2860.0	667.7
128	S128	2820.0	512.2
129	S129	2780.0	667.7
130	S130	2740.0	512.2
131	S131	2700.0	667.7
132	S132	2660.0	512.2
133	S133	2620.0	667.7
134	S134	2580.0	512.2
135	S135	2540.0	667.7
136	S136	2500.0	512.2
137	S137	2460.0	667.7
138	S138	2420.0	512.2
139	S139	2380.0	667.7
140	S140	2340.0	512.2
141	S141	2300.0	667.7
142	S142	2260.0	512.2
143	S143	2220.0	667.7
144	S144	2180.0	512.2
145	S145	2140.0	667.7
146	S146	2100.0	512.2
147	S147	2060.0	667.7
148	S148	2020.0	512.2
149	S149	1980.0	667.7
150	S150	1940.0	512.2
151	S151	1900.0	667.7
152	S152	1860.0	512.2
153	S153	1820.0	667.7
154	S154	1780.0	512.2
155	S155	1740.0	667.7
156	S156	1700.0	512.2
157	S157	1660.0	667.7
158	S158	1620.0	512.2
159	S159	1580.0	667.7
160	S160	1540.0	512.2
161	S161	1500.0	667.7
162	S162	1460.0	512.2
163	S163	1420.0	667.7
164	S164	1380.0	512.2
165	S165	1340.0	667.7
166	S166	1300.0	512.2
167	S167	1260.0	667.7
168	S168	1220.0	512.2
169	S169	1180.0	667.7
170	S170	1140.0	512.2
171	S171	1100.0	667.7
172	S172	1060.0	512.2
173	S173	1020.0	667.7
174	S174	980.0	512.2

Table 2–1. Pad Layout (2/3)

No.	Pad Name	X [μm]	Y [μm]
175	S175	940.0	667.7
176	S176	900.0	512.2
177	S177	860.0	667.7
178	S178	820.0	512.2
179	S179	780.0	667.7
180	S180	740.0	512.2
181	S181	700.0	667.7
182	S182	660.0	512.2
183	S183	620.0	667.7
184	S184	580.0	512.2
185	S185	540.0	667.7
186	S186	500.0	512.2
187	S187	460.0	667.7
188	S188	420.0	512.2
189	S189	380.0	667.7
190	S190	340.0	512.2
191	S191	300.0	667.7
192	S192	260.0	512.2
193	S193	220.0	667.7
194	S194	180.0	512.2
195	S195	140.0	667.7
196	S196	100.0	512.2
197	S197	60.0	667.7
198	S198	20.0	512.2
199	S199	-20.0	667.7
200	S200	-60.0	512.2
201	S201	-100.0	667.7
202	S202	-140.0	512.2
203	S203	-180.0	667.7
204	S204	-220.0	512.2
205	S205	-260.0	667.7
206	S206	-300.0	512.2
207	S207	-340.0	667.7
208	S208	-380.0	512.2
209	S209	-420.0	667.7
210	S210	-460.0	512.2
211	S211	-500.0	667.7
212	S212	-540.0	512.2
213	S213	-580.0	667.7
214	S214	-620.0	512.2
215	S215	-660.0	667.7
216	S216	-700.0	512.2
217	S217	-740.0	667.7
218	S218	-780.0	512.2
219	S219	-820.0	667.7
220	S220	-860.0	512.2
221	S221	-900.0	667.7
222	S222	-940.0	512.2
223	S223	-980.0	667.7
224	S224	-1020.0	512.2
225	S225	-1060.0	667.7
226	S226	-1100.0	512.2
227	S227	-1140.0	667.7
228	S228	-1180.0	512.2
229	S229	-1220.0	667.7
230	S230	-1260.0	512.2
231	S231	-1300.0	667.7
232	S232	-1340.0	512.2
233	S233	-1380.0	667.7
234	S234	-1420.0	512.2
235	S235	-1460.0	667.7
236	S236	-1500.0	512.2
237	S237	-1540.0	667.7
238	S238	-1580.0	512.2
239	S239	-1620.0	667.7
240	S240	-1660.0	512.2
241	S241	-1700.0	667.7
242	S242	-1740.0	512.2
243	S243	-1780.0	667.7
244	S244	-1820.0	512.2
245	S245	-1860.0	667.7
246	S246	-1900.0	512.2
247	S247	-1940.0	667.7
248	S248	-1980.0	512.2
249	S249	-2020.0	667.7
250	S250	-2060.0	512.2
251	S251	-2100.0	667.7
252	S252	-2140.0	512.2
253	S253	-2180.0	667.7
254	S254	-2220.0	512.2
255	S255	-2260.0	667.7
256	S256	-2300.0	512.2
257	S257	-2340.0	667.7
258	S258	-2380.0	512.2
259	S259	-2420.0	667.7
260	S260	-2460.0	512.2
261	S261	-2500.0	667.7
262	S262	-2540.0	512.2
263	S263	-2580.0	667.7
264	S264	-2620.0	512.2
265	S265	-2660.0	667.7
266	S266	-2700.0	512.2
267	S267	-2740.0	667.7
268	S268	-2780.0	512.2
269	S269	-2820.0	667.7
270	S270	-2860.0	512.2
271	S271	-2900.0	667.7
272	S272	-2940.0	512.2
273	S273	-2980.0	667.7
274	S274	-3020.0	512.2
275	S275	-3060.0	667.7
276	S276	-3100.0	512.2
277	S277	-3140.0	667.7
278	S278	-3180.0	512.2
279	S279	-3220.0	667.7
280	S280	-3260.0	512.2
281	S281	-3300.0	667.7
282	S282	-3340.0	512.2
283	S283	-3380.0	667.7
284	S284	-3420.0	512.2
285	S285	-3460.0	667.7
286	S286	-3500.0	512.2
287	S287	-3540.0	667.7
288	S288	-3580.0	512.2
289	S289	-3620.0	667.7
290	S290	-3660.0	512.2
291	S291	-3700.0	667.7
292	S292	-3740.0	512.2
293	S293	-3780.0	667.7
294	S294	-3820.0	512.2
295	S295	-3860.0	667.7
296	S296	-3900.0	512.2
297	S297	-3940.0	667.7
298	S298	-3980.0	512.2
299	S299	-4020.0	667.7
300	S300	-4060.0	512.2
301	S301	-4100.0	667.7
302	S302	-4140.0	512.2
303	S303	-4180.0	667.7
304	S304	-4220.0	512.2
305	S305	-4260.0	667.7
306	S306	-4300.0	512.2
307	S307	-4340.0	667.7
308	S308	-4380.0	512.2
309	S309	-4420.0	667.7
310	S310	-4460.0	512.2
311	S311	-4500.0	667.7
312	S312	-4540.0	512.2
313	S313	-4580.0	667.7
314	S314	-4620.0	512.2
315	S315	-4660.0	667.7
316	S316	-4700.0	512.2
317	S317	-4740.0	667.7
318	S318	-4780.0	512.2
319	S319	-4820.0	667.7
320	S320	-4860.0	512.2
321	S321	-4900.0	667.7
322	S322	-4940.0	512.2
323	S323	-4980.0	667.7
324	S324	-5020.0	512.2
325	S325	-5060.0	667.7
326	S326	-5100.0	512.2
327	S327	-5140.0	667.7
328	S328	-5180.0	512.2
329	S329	-5220.0	667.7
330	S330	-5260.0	512.2
331	S331	-5300.0	667.7
332	S332	-5340.0	512.2
333	S333	-5380.0	667.7
334	S334	-5420.0	512.2
335	S335	-5460.0	667.7
336	S336	-5500.0	512.2
337	S337	-5540.0	667.7
338	S338	-5580.0	512.2
339	S339	-5620.0	667.7
340	S340	-5660.0	512.2
341	S341	-5700.0	667.7
342	S342	-5740.0	512.2
343	S343	-5780.0	667.7
344	S344	-5820.0	512.2
345	S345	-5860.0	667.7
346	S346	-5900.0	512.2
347	S347	-5940.0	667.7
348	S348	-5980.0	512.2

Table 2–1. Pad Layout (3/3)

No.	Pad Name	X [μm]	Y [μm]
349	S349	-6020.0	667.7
350	S350	-6060.0	512.2
351	S351	-6100.0	667.7
352	S352	-6140.0	512.2
353	S353	-6180.0	667.7
354	S354	-6220.0	512.2
355	S355	-6260.0	667.7
356	S356	-6300.0	512.2
357	S357	-6340.0	667.7
358	S358	-6380.0	512.2
359	S359	-6420.0	667.7
360	S360	-6460.0	512.2
361	S361	-6500.0	667.7
362	S362	-6540.0	512.2
363	S363	-6580.0	667.7
364	S364	-6620.0	512.2
365	S365	-6660.0	667.7
366	S366	-6700.0	512.2
367	S367	-6740.0	667.7
368	S368	-6780.0	512.2
369	S369	-6820.0	667.7
370	S370	-6860.0	512.2
371	S371	-6900.0	667.7
372	S372	-6940.0	512.2
373	S373	-6980.0	667.7
374	S374	-7020.0	512.2
375	S375	-7060.0	667.7
376	S376	-7100.0	512.2
377	S377	-7140.0	667.7
378	S378	-7180.0	512.2
379	S379	-7220.0	667.7
380	S380	-7260.0	512.2
381	S381	-7300.0	667.7
382	S382	-7340.0	512.2
383	S383	-7380.0	667.7
384	S384	-7420.0	512.2
385	S385	-7460.0	667.7
386	S386	-7500.0	512.2
387	S387	-7540.0	667.7
388	S388	-7580.0	512.2
389	S389	-7620.0	667.7
390	S390	-7660.0	512.2
391	S391	-7700.0	667.7
392	S392	-7740.0	512.2
393	S393	-7780.0	667.7
394	S394	-7820.0	512.2
395	S395	-7860.0	667.7
396	S396	-7900.0	512.2
397	Dummy1	-8031.4	687.0
398	Dummy2	-8367.0	347.0
399	Dummy3	-8367.0	247.0
400	Dummy4	-8367.0	147.0
401	Dummy5	-8367.0	47.0
402	Dummy6	-8367.0	-53.1
403	Dummy7	-8367.0	-153.1
404	Dummy8	-8367.0	-253.1
405	Dummy9	-8367.0	-353.1
406	Dummy10	-8367.0	-453.2
407	Dummy11	-8367.0	-553.2
408	Dummy12	-8254.8	-687.0
409	VCOM	-8079.8	-687.0
410	STHL	-7829.8	-687.0
411	Dummy13	-7654.8	-687.0
412	VDD2	-7393.4	-687.0
413	VDD2	-7293.4	-687.0
414	VDD2	-7193.4	-687.0
415	Dummy14	-6932.0	-687.0
416	VDD1	-6831.9	-687.0
417	VDD1	-6732.0	-687.0
418	VDD1	-6632.0	-687.0
419	Dummy15	-6456.9	-687.0
420	VSS1	-6278.6	-687.0
421	VSS1	-6178.7	-687.0
422	VSS1	-6078.7	-687.0
423	Dummy16	-5903.7	-686.9
424	VSS2	-5728.7	-687.0
425	VSS2	-5628.7	-687.0
426	VSS2	-5528.7	-687.0
427	Dummy17	-5350.4	-687.0
428	VCSEL	-5175.4	-687.0
429	R,/L	-4925.3	-687.0
430	OSEL	-4675.3	-687.0
431	BA	-4425.3	-687.0
432	GAM	-4175.3	-687.0
433	CM	-3925.3	-687.0
434	POL	-3675.2	-687.0
435	AP	-3425.2	-687.0
436	STB	-3175.2	-687.0
437	D25	-2925.2	-687.0
438	D24	-2675.2	-687.0
439	D23	-2425.1	-687.0
440	D22	-2175.1	-687.0
441	D21	-1925.1	-687.0
442	D20	-1675.1	-687.0
443	CLK	-1425.1	-687.0
444	Dummy18	-1250.0	-687.0
445	V4	-1075.0	-687.0
446	V4	-975.0	-687.0
447	V4	-875.1	-687.0
448	Dummy19	-700.0	-687.0
449	V3	-525.0	-687.0
450	V3	-425.0	-687.0
451	V3	-325.1	-687.0
452	Dummy20	-150.0	-687.0
453	V2	25.1	-687.0
454	V2	125.0	-687.0
455	V2	225.0	-687.0
456	Dummy21	400.0	-687.0
457	V1	575.1	-687.0
458	V1	675.0	-687.0
459	V1	775.0	-687.0
460	Dummy22	950.0	-687.0
461	V0	1125.1	-687.0
462	V0	1225.1	-687.0
463	V0	1325.0	-687.0
464	Dummy23	1500.1	-687.0
465	INV	1675.1	-687.0
466	D15	1925.1	-687.0
467	D14	2175.1	-687.0
468	D13	2425.1	-687.0
469	D12	2675.2	-687.0
470	D11	2925.2	-687.0
471	D10	3175.2	-687.0
472	D05	3425.2	-687.0
473	D04	3675.2	-687.0
474	D03	3925.3	-687.0
475	D02	4175.3	-687.0
476	D01	4425.3	-687.0
477	D00	4675.3	-687.0
478	TESTO1	4925.3	-687.0
479	TESTO2	5175.4	-687.0
480	TESTIN	5425.4	-687.0
481	Dummy24	5600.4	-687.0
482	VDD1	5775.5	-687.0
483	VDD1	5875.5	-687.0
484	VDD1	5975.4	-687.0
485	Dummy25	6075.5	-687.0
486	VSS1	6253.8	-687.0
487	VSS1	6353.8	-687.0
488	VSS1	6453.8	-687.0
489	Dummy26	6628.8	-687.0
490	VSS2	6803.8	-687.0
491	VSS2	6903.8	-687.0
492	VSS2	7003.7	-687.0
493	Dummy27	7182.0	-687.0
494	VDD2	7443.5	-687.0
495	VDD2	7543.4	-687.0
496	VDD2	7643.4	-687.0
497	Dummy28	7904.8	-687.0
498	STHR	8079.8	-687.0
499	Dummy29	8254.8	-687.0
500	Dummy30	8367.0	-553.2
501	Dummy31	8367.0	-453.2
502	Dummy32	8367.0	-353.1
503	Dummy33	8367.0	-253.1
504	Dummy34	8367.0	-153.1
505	Dummy35	8367.0	-53.1
506	Dummy36	8367.0	47.0
507	Dummy37	8367.0	147.0
508	Dummy38	8367.0	247.0
509	Dummy39	8367.0	347.0
510	Dummy40	8031.4	687.0

★ 3. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	Pad No.	I/O	Description
S_1 to S_{396}	Driver output	1 to 396	Output	The D/A converted 64-gray-scale analog voltage is output. O_{sel} = L: S_1 to S_{396} O_{sel} = H: S_{19} to S_{378}
D_{00} to D_{05}	Display data input	477 to 472	Input	The display data is input with a width of 18 bits, viz., the gray scale data (6 bits) by 3 dots (1 pixels). D_{X0}: LSB, D_{X5}: MSB
D_{10} to D_{15}		471 to 466		
D_{20} to D_{25}		442 to 437		
R,/L	Shift direction control input	429	Input	These refer to the shift direction control input. The shift directions of the shift registers are as follows. <When in O_{sel} = L> R,/L = L (left shift): STHL (input), $S_{396} \rightarrow S_1 \rightarrow$ STHR (output) R,/L = H (right shift) : STHR (input), $S_1 \rightarrow S_{396} \rightarrow$ STHL (output) <When in O_{sel} = H> R,/L = L (left shift): STHL (input), $S_{378} \rightarrow S_{19} \rightarrow$ STHR (output) R,/L = H (right shift) : STHR (input), $S_{19} \rightarrow S_{378} \rightarrow$ STHL (output)
STHR	Right shift start pulse input/output	498	I/O	These refer to the start pulse I/O pins when driver ICs are connected in cascade. Fetching of display data starts when H is read at the rising edge of CLK. R,/L = H (right shift): STHR input, STHL output R,/L = L (left shift): STHL input, STHR output
STHL	Left shift start pulse input/output	410	I/O	
CLK	Shift clock input	443	Input	This pin is the shift clock input of the shift register. Display data is captured into the data register at the rising edge. O_{sel} = L: The start pulse output enters high level at the rising edge of the 132 th clock following the start pulse input, and becomes the start pulse of the next level driver. The 133th clock of the first driver becomes the start pulse input of the next driver O_{sel} = H: The start pulse output enters high level at the rising edge of the 120th clock following the start pulse input, and becomes the start pulse of the next driver. The 121th clock of the first driver becomes the start pulse input of the next driver.
STB	Latch input	436	Input	A timing signal that latches the contents of the data register. When an H level is read at the rising edge of CLK, the contents of the data register are latched and transferred to the D/A converter, and analog voltage corresponding to the display data is output. Also, because the internal operation via CLK continues even after the STB latch, do not stop CLK. The contents of the shift register are cleared at the rising edge of STB. Following a 1-pulse input at startup, this IC will operate normally. Note that the output switch is turned off at the rising edge of STB. For the STB input timing, refer to **Switching Characteristics Waveform.**
POL	Polarity inversion signal	434	Input	This pin inverts the output polarity. The polarity inversion signal data is captured at the rising edge of STB. The γ-resistor is switched in accordance with the positive/negative polarity. POL = L: Negative polarity POL = H: Positive polarity
INV	Data inversion	465	Input	This pin inverts the input data. Input data in synchronization with the shift clock. INV = L: Normal input INV = H: Data inversion input
VCOM	COM amplitude output	409	Output	This pin inverts the signal input from the POL pin and outputs it following conversion to the V_{DD2} potential at the rising edge of STB. When the VCOM output is not used, VC_{sel} must be fixed to L.

(2/2)

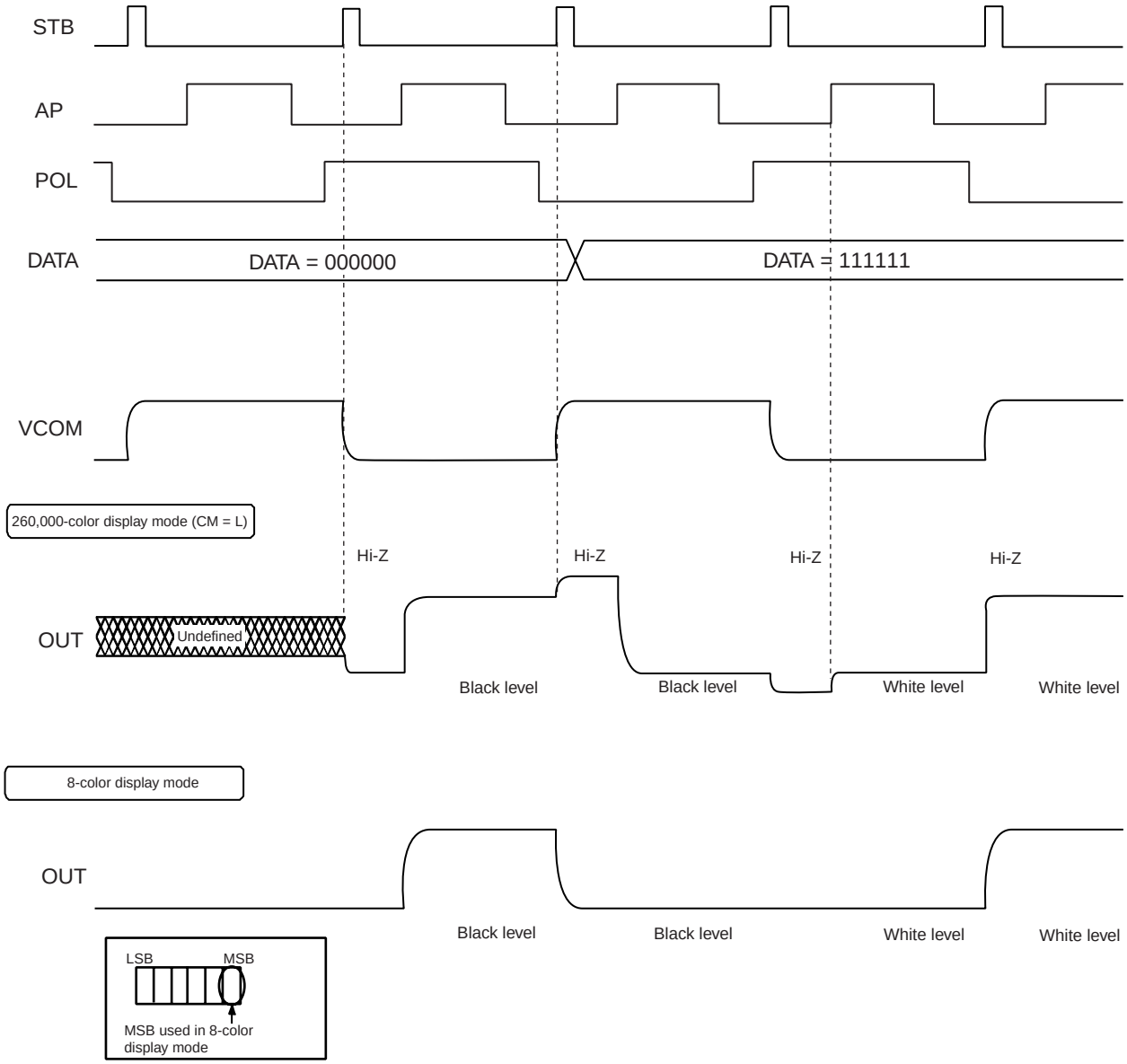
Pin Symbol	Pin Name	Pad No.	I/O	Description
VC_{sel}	COM amplitude output fixing signal	428	Input	The VCOM output is fixed to L. When the VCOM output is not used, VC_{sel} needs to be fixed to L. VC_{sel} = L: VCOM output fixed to L VC_{sel} = H: VCOM signal output in correspondence with POL signal
CM	8-color display mode switching	433	Input	The operating mode is switched to 8-color mode. In this mode, turn off the γ-resistor, amplifier, and BIAS circuit. However, when the γ-correction power supply is input externally, the γ-circuit current will flow continuously. CM = L: Normal display mode CM = H: 8-color display mode
AP	Output SW ON/OFF	435	Input	This pin turns ON/OFF the BIAS circuit and turns on the output SW and amplifier. When AP is H, the amplifier is set and the LCD is driving. The amplifier output and output SW are turned on at the rising edge of AP, starting the LCD drive. Note that the output SW is turned off at the rising edge of STB and the output becomes Hi-Z. For the AP input timing, refer to **Switching Characteristics Waveform.**
GAM	External γ usage selection	432	Input	When the γ-correction power supply is input externally, switch GAM to H. If two or more chips are used, be sure to input the γ-correction power supply externally. Figure 4–1 shows an input example of the γ-correction power supply. GAM = L: External γ-correction power supply not input (open) GAM = H: External γ-correction power supply input
O_{sel}	Driver output count switching	430	Input	The output count can be selected. When O_{sel} = H, the unused pins S_1 to S_{18} and S_{379} to S_{396} always become Hi-Z. O_{sel} = L: 396 outputs O_{sel} = H: 360 outputs
V_0 to V_4	γ-corrected power supplies	461 to 463, 457 to 459, 453 to 455, 449 to 451, 445 to 447	–	These pins input the γ-corrected power supplies from outside, the relationship below must be observed. Also, be sure to stabilize the gray-scale-level power supply during gray-scale voltage output. $V_{SS2} \leq V_4 \leq V_3 \leq V_2 \leq V_1 \leq V_0 \leq V_{DD2}$
BA	BIAS current adjustment function	431	Input	This pin adjusts the BIAS current. Select either the high power mode or low power mode. BA = L: Low power mode BA = H: high power mode
$TEST_{IN}$	TEST input pin	480	Input	Set to H or leave open
$TEST_{O1}$, $TEST_{O2}$	TEST output pin	478, 479	Output	Leave open.
V_{DD1}	Logic power supply	416 to 418, 482 to 484	–	2.2 to 3.6 V
V_{DD2}	Driver power supply	412 to 414, 494 to 496	–	4.5 to 5.5 V
V_{SS1}	Logic ground	420 to 422, 486 to 488	–	Ground
V_{SS2}	Driver ground	424 to 426, 490 to 492	–	Ground
Dummy1 to dummy40	Dummy	397 to 408, 411, 415, 419, 423, 427, 444, 448, 452, 456, 460, 464, 481, 485, 489, 493, 487, 499 to 510	–	This pin is dummy.

Caution To avoid latchup failure, the sequence when turning on the power must be V_{DD1} → logic input → V_{DD2} →gray-scale power supply (V_0 to V_4), and the reverse sequence when turning off the power. Follow this sequence during shift periods as well.

4. EXAMPLES OF EACH SINGAL INPUT OR OUTPUT

Examples of the input/output timing of each signal during white and black display are shown below.

Figure 4–1. Timing Chart

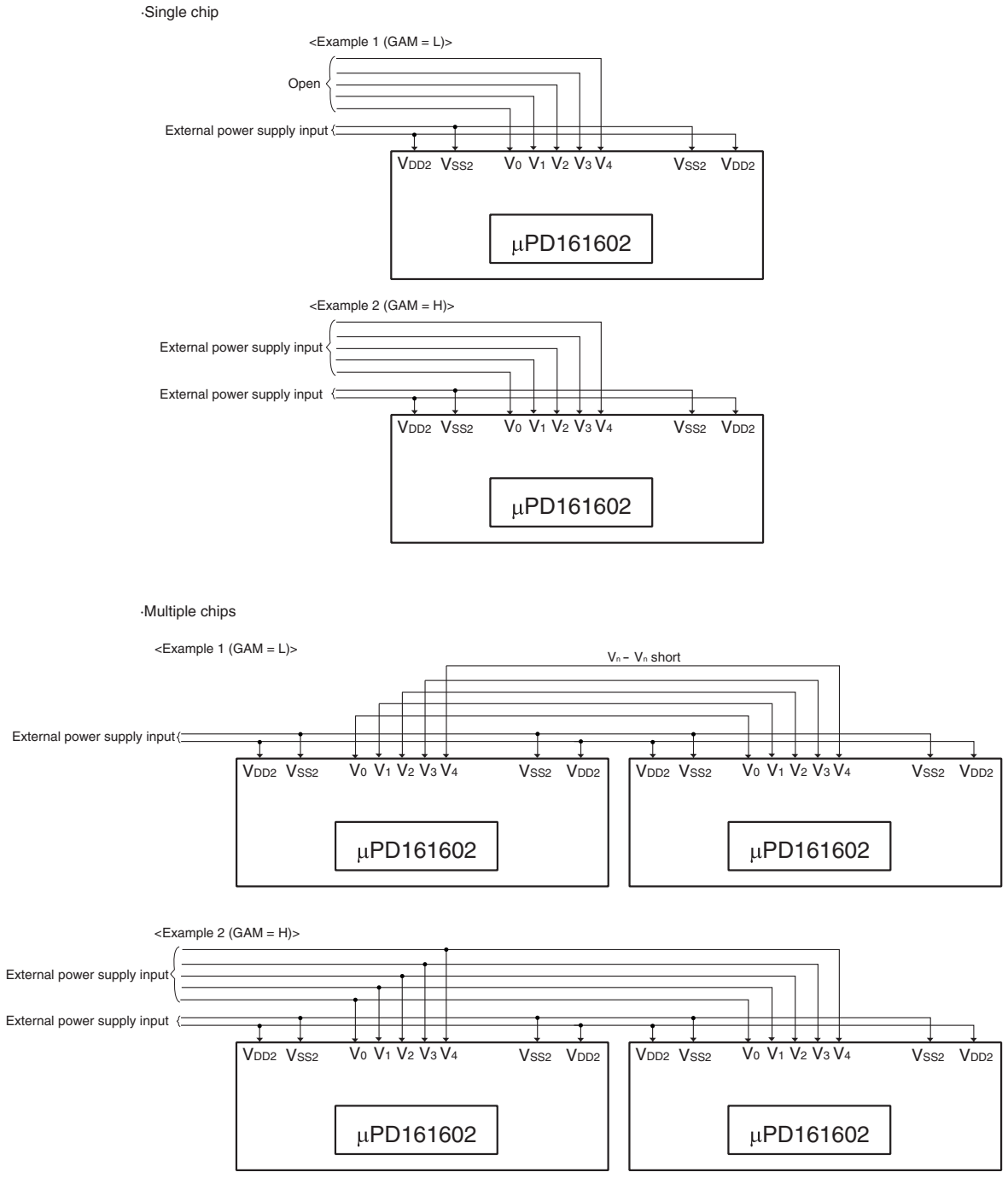


4.1 γ-Correction Power Supply Connection Example

The μ PD161602A/B enables customization of the γ-correction power supply on both the positive and negative polarity sides (refer to **6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE**). Consequently, a γ-correction power supply does not have to be input externally when a single source-driver chip is being used in the panel.

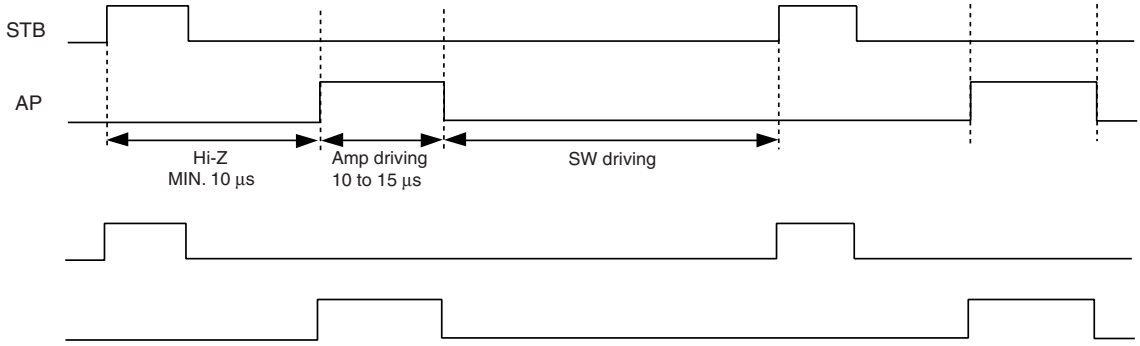
Multiple chips can also be used without having to input a γ-correction power supply externally because the error between the chips can be absorbed by shorting the γ-correction power supply pins, as shown in Figure 4–2.

Figure 4–2. γ-Correction Power-Supply Connection Example



4.2 AP Signal Timing

The driver power consumption is dependent on the high period of the AP signal because the operational amplifier in the IC is operation and current is constantly flowing in this period. A chart indication the recommended timing of inputting the AP signal vis-a-vis the STB signal is shown below.

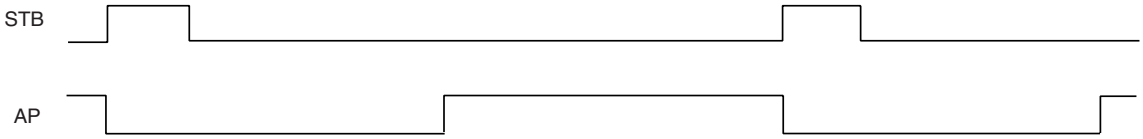


Note that the ideal AP signal high period differs depending on the load of the liquid crystal. The AP period must therefore be able to be adjusted using a controller.

The AP signal can also be used as shown below. However, in these cases, be sure to perform sufficient evaluation before use.

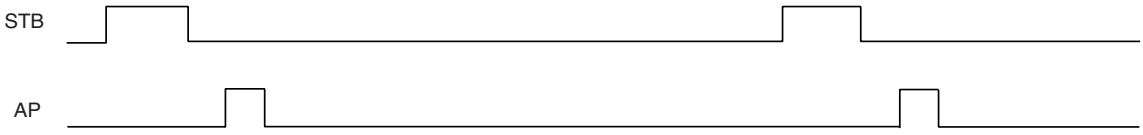
<When SW drive in not used>

Only the amp is driven (SW drive is not used) if one horizontal period is short (40 μs or less) or the liquid crystal load is large (50 pF or more).



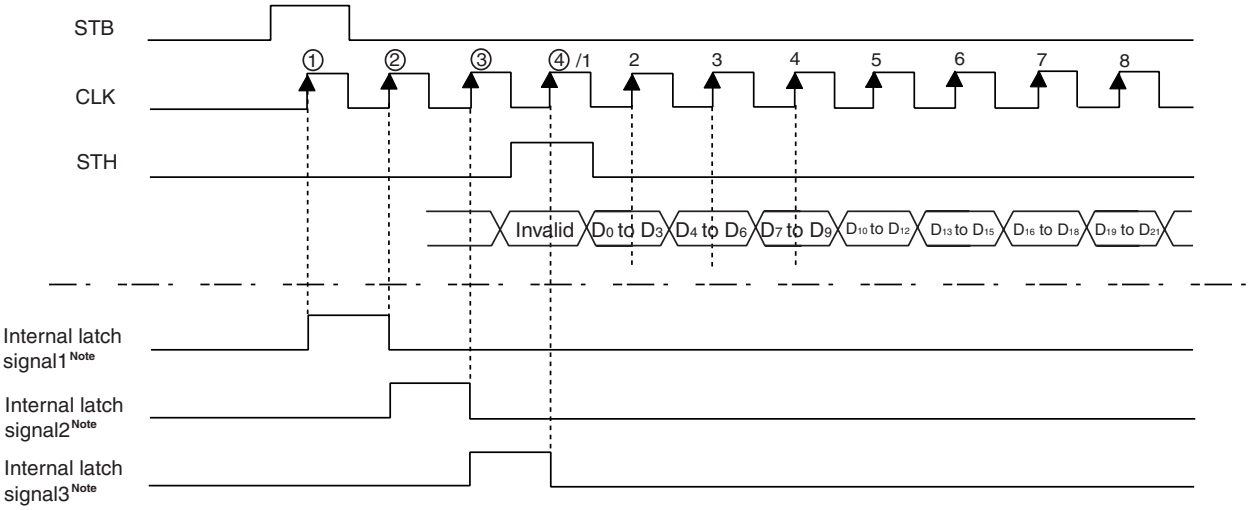
<When the AP signal high period is 10 μs or less>

The amp drive period is shortened and the SW drive period lengthened when one horizontal period is long (100 μs or more) and the liquid crystal load is small (20 pF).



4.3 CLK Signal Input

Input at least 4 clocks of the CLK signal after the rising of the STB signal.



Note Internal latch signal : It is the signal that do latch the display data put in data register in output latch circuit.

5. MODE EXPLANATION

Normal Mode/ 8-clor Display Mode

CM	POL	Data	Driver Output Status	Driver Output (in normally white)
H	H	MSB = H	8-color mode	White level display
		MSB = L		Black level display
	L	MSB = H		White level display
		MSB = L		Black level display
L	H	All bit = H	260,000-color mode	White level display
		All bit = L		Black level display
	L	All bit = H		White level display
		All bit = L		Black level display

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The relation between input data and output voltage are shown in Table 6–2, 6–3.

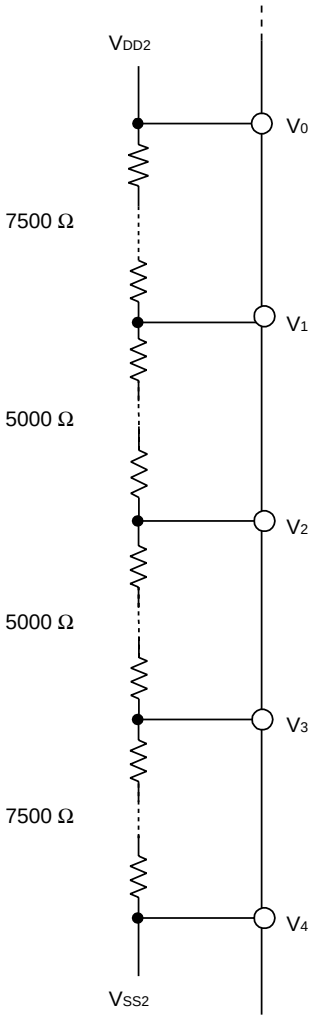
Any 3 major points V_1 to V_3 from the LCD panel γ-characteristics curve can be used as the external power supplies.

The relationship V_0 to V_4 external power supplies and γ-correction resistance is shown in Table 6–1, Figure 6–1.

Table 6–1. Relationship between External Power Supply Pins and γ-correction Resistance

Pin Name	Voltage (V)	Resistance (Ω)
V_0	5.0	0
V_1	3.5	7,500
V_2	2.5	12,500
V_3	1.5	17,500
V_4	0	25,000

Figure 6–1. Relationship between External Power Supply Pins and γ-correction Resistance



This external power supply pins (V_0 to V_4) can customize the γ-correction voltage by selecting the desired voltage from one of 250 divisions of the string resistor between V_{SS2} and V_{DD2}, which generated γ-correction voltage. Note that the voltage can be selected individually for both positive and negative polarity.

Table 6–2. Relation of Input Data and Output Voltage in μPD161602A

Input Data	Gray Scale	Positive Polarity Side (V)	Negative Polarity Side (V)	Positive Polarity Side (Ω)	Negative Polarity Side (Ω)
00H	0	5.000	0.000	0	25000
01H	1	4.920	0.080	400	24600
02H	2	4.760	0.260	1200	23700
03H	3	4.540	0.480	2300	22600
04H	4	4.280	0.760	3600	21200
05H	5	3.960	1.080	5200	19600
06H	6	3.840	1.200	5800	19000
07H	7	3.740	1.300	6300	18500
08H	8	3.640	1.400	6800	18000
09H	9	3.540	1.520	7300	17400
0AH	10	3.480	1.580	7600	17100
0BH	11	3.400	1.660	8000	16700
0CH	12	3.320	1.740	8400	16300
0DH	13	3.240	1.840	8800	15800
0EH	14	3.160	1.920	9200	15400
0FH	15	3.100	2.000	9500	15000
10H	16	3.060	2.060	9700	14700
11H	17	3.000	2.100	10000	14500
12H	18	2.960	2.160	10200	14200
13H	19	2.900	2.220	10500	13900
14H	20	2.860	2.280	10700	13600
15H	21	2.820	2.320	10900	13400
16H	22	2.780	2.360	11100	13200
17H	23	2.740	2.400	11300	13000
18H	24	2.700	2.440	11500	12800
19H	25	2.680	2.480	11600	12600
1AH	26	2.640	2.520	11800	12400
1BH	27	2.620	2.560	11900	12200
1CH	28	2.600	2.580	12000	12100
1DH	29	2.560	2.620	12200	11900
1EH	30	2.540	2.660	12300	11700
1FH	31	2.500	2.700	12500	11500

Input Data	Gray Scale	Positive Polarity Side (V)	Negative Polarity Side (V)	Positive Polarity Side (Ω)	Negative Polarity Side (Ω)
20H	32	2.480	2.720	12600	11400
21H	33	2.460	2.760	12700	11200
22H	34	2.420	2.800	12900	11000
23H	35	2.400	2.820	13000	10900
24H	36	2.360	2.860	13200	10700
25H	37	2.340	2.900	13300	10500
26H	38	2.300	2.940	13500	10300
27H	39	2.280	2.960	13600	10200
28H	40	2.240	3.000	13800	10000
29H	41	2.220	3.040	13900	9800
2AH	42	2.180	3.080	14100	9600
2BH	43	2.160	3.100	14200	9500
2CH	44	2.140	3.140	14300	9300
2DH	45	2.120	3.180	14400	9100
2EH	46	2.080	3.200	14600	9000
2FH	47	2.060	3.240	14700	8800
30H	48	2.040	3.260	14800	8700
31H	49	2.020	3.300	14900	8500
32H	50	1.980	3.340	15100	8300
33H	51	1.960	3.360	15200	8200
34H	52	1.920	3.400	15400	8000
35H	53	1.900	3.440	15500	7800
36H	54	1.860	3.480	15700	7600
37H	55	1.840	3.520	15800	7400
38H	56	1.780	3.580	16100	7100
39H	57	1.740	3.620	16300	6900
3AH	58	1.680	3.680	16600	6600
3BH	59	1.620	3.760	16900	6200
3CH	60	1.520	3.860	17400	5700
3DH	61	1.360	4.040	18200	4800
3EH	62	1.180	4.220	19100	3900
3FH	63	0.400	5.000	23000	0

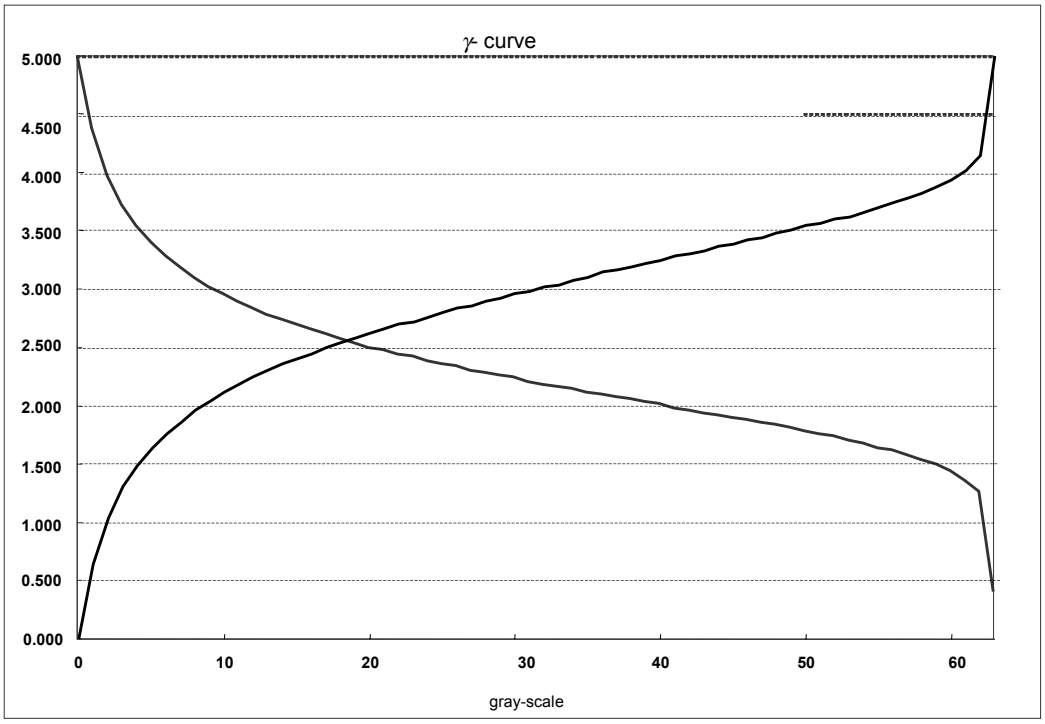
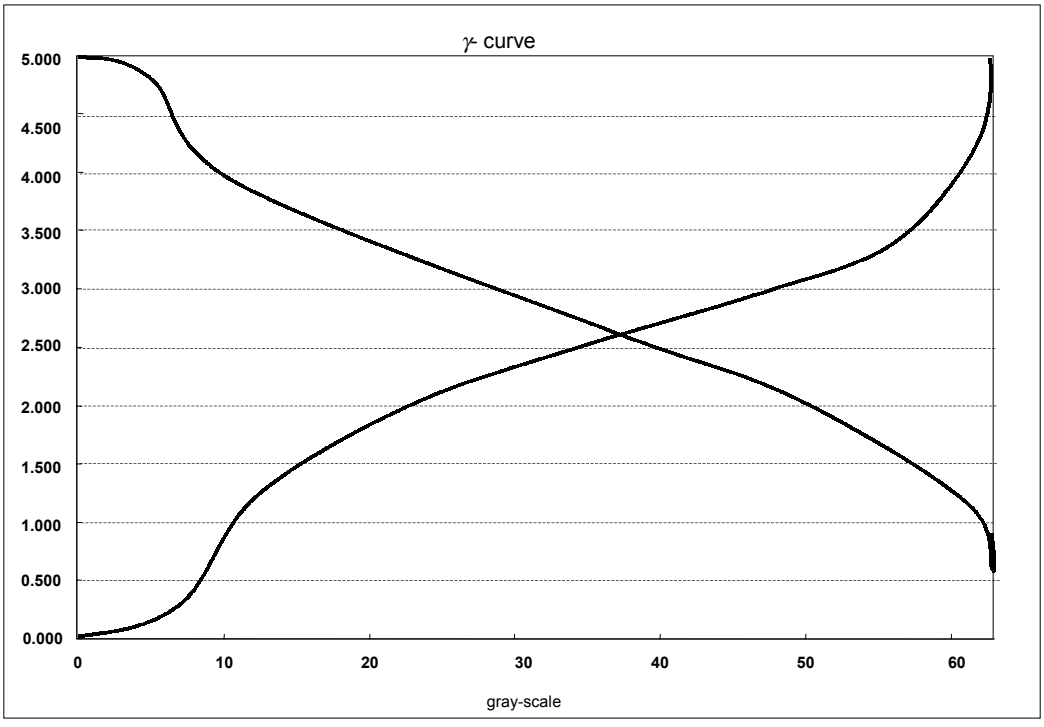


Table 6–3. Relation of Input Data and Output Voltage in μPD161602B

Input Data	Gray Scale	Positive Polarity Side (V)	Negative Polarity Side (V)	Positive Polarity Side (Ω)	Negative Polarity Side (Ω)
00H	0	5.000	0.000	0	25000
01H	1	4.980	0.020	100	24900
02H	2	4.960	0.060	200	24700
03H	3	4.920	0.100	400	24500
04H	4	4.880	0.140	600	24300
05H	5	4.800	0.220	1000	23900
06H	6	4.720	0.300	1400	23500
07H	7	4.600	0.440	2000	22800
08H	8	4.460	0.580	2700	22100
09H	9	4.320	0.740	3400	21300
0AH	10	4.160	0.920	4200	20400
0BH	11	4.000	1.080	5000	19600
0CH	12	3.860	1.240	5700	18800
0DH	13	3.780	1.320	6100	18400
0EH	14	3.700	1.420	6500	17900
0FH	15	3.620	1.500	6900	17500
10H	16	3.540	1.600	7300	17000
11H	17	3.460	1.680	7700	16600
12H	18	3.380	1.760	8100	16200
13H	19	3.320	1.820	8400	15900
14H	20	3.280	1.880	8600	15600
15H	21	3.220	1.940	8900	15300
16H	22	3.160	2.000	9200	15000
17H	23	3.120	2.040	9400	14800
18H	24	3.060	2.100	9700	14500
19H	25	3.040	2.140	9800	14300
1AH	26	3.000	2.180	10000	14100
1BH	27	2.960	2.220	10200	13900
1CH	28	2.940	2.240	10300	13800
1DH	29	2.900	2.280	10500	13600
1EH	30	2.860	2.320	10700	13400
1FH	31	2.820	2.360	10900	13200

Input Data	Gray Scale	Positive Polarity Side (V)	Negative Polarity Side (V)	Positive Polarity Side (Ω)	Negative Polarity Side (Ω)
20H	32	2.780	2.400	11100	13000
21H	33	2.760	2.440	11200	12800
22H	34	2.720	2.480	11400	12600
23H	35	2.680	2.520	11600	12400
24H	36	2.660	2.540	11700	12300
25H	37	2.620	2.580	11900	12100
26H	38	2.600	2.620	12000	11900
27H	39	2.560	2.660	12200	11700
28H	40	2.520	2.700	12400	11500
29H	41	2.480	2.740	12600	11300
2AH	42	2.460	2.780	12700	11100
2BH	43	2.400	2.820	13000	10900
2CH	44	2.360	2.860	13200	10700
2DH	45	2.340	2.900	13300	10500
2EH	46	2.300	2.940	13500	10300
2FH	47	2.260	2.980	13700	10100
30H	48	2.220	3.020	13900	9900
31H	49	2.180	3.060	14100	9700
32H	50	2.140	3.100	14300	9500
33H	51	2.100	3.160	14500	9200
34H	52	2.040	3.220	14800	8900
35H	53	2.000	3.260	15000	8700
36H	54	1.960	3.320	15200	8400
37H	55	1.900	3.380	15500	8100
38H	56	1.840	3.420	15800	7900
39H	57	1.780	3.520	16100	7400
3AH	58	1.700	3.600	16500	7000
3BH	59	1.580	3.720	17100	6400
3CH	60	1.460	3.840	17700	5800
3DH	61	1.260	4.060	18700	4700
3EH	62	1.080	4.280	19600	3600
3FH	63	0.400	5.000	23000	0

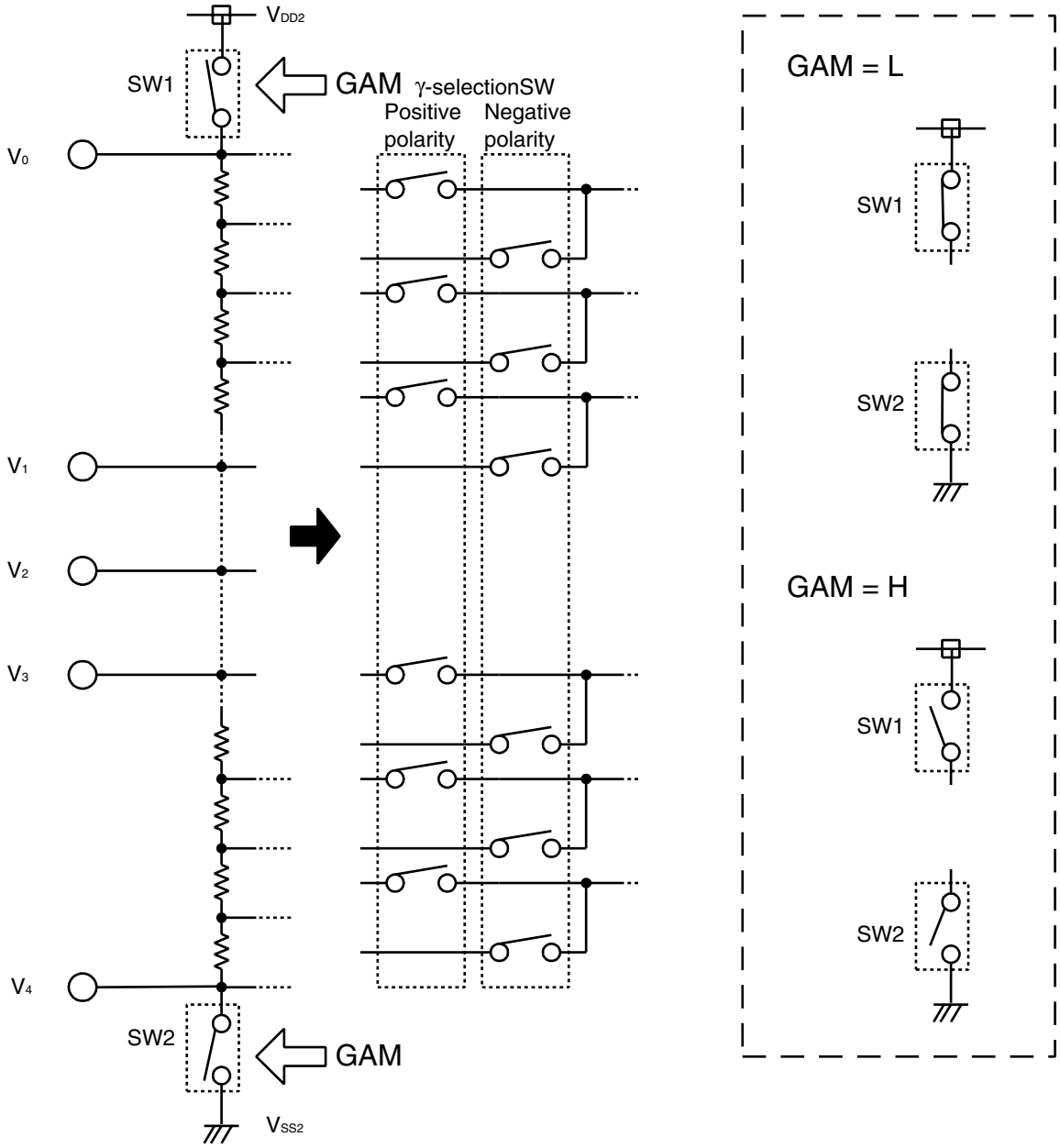


6.1 Connection between γ-correction Resistance, Power Supply, and GND Pin

Connection of γ- compensation resistance power supply (V_0-V_4) and a power supply pin (V_{DD2} and V_{SS2}) is indicated below to be γ- compensation resistance of μPD161602 A/B.

By setup of a GAM pin, as for γ-compensation resistance, connection changes the highest minimum potential between V_{DD2}-V_{SS2} or among V_0-V_4.

Figure 6–2. GAM Pin Function



7. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 6 bits x RGBs (3 dots)

Input width: 18 bits (1-pixel data)

R,/L = H (Right shift), O_{sel} = L (396 outputs)

Output	S_1	S_2	S_3	S_4	...	S_{395}	S_{396}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{00} to D_{05}	...	D_{10} to D_{15}	D_{20} to D_{25}

R,/L = L (Left shift), O_{sel} = L (396 outputs)

Output	S_1	S_2	S_3	S_4	...	S_{395}	S_{396}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{00} to D_{05}	...	D_{10} to D_{15}	D_{20} to D_{25}

8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	–0.3 to +4.5	V
Driver Part Supply Voltage	V_{DD2}	–0.3 to +6.0	V
Input Voltage	V_I	–0.3 to $V_{DD1,2}$ + 0.3	V
Output Voltage	V_O	–0.3 to $V_{DD1,2}$ + 0.3	V
Operating Ambient Temperature	T_A	–20 to +75	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –20 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}		2.2		3.6	V
Driver Part Supply Voltage	V_{DD2}		4.5	5.0	5.5	V
High-Level Input Voltage	V_{IH}		0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}		0		0.3 V_{DD1}	V
γ-Corrected Voltage	V_0 to V_4		V_{SS2}		V_{DD2}	V
Clock Frequency	f_{CLK}				15	MHz

Electrical Characteristics (T_A = –20 to +75°C, V_{DD1} = 2.2 to 3.6 V, V_{DD2} = 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Leak Current	I_{IL}	D_{00}-D_{05}, D_{10}-D_{15}, D_{20}-D_{25}, R,/L, STB, CLK, STHR(L), INV, CM, AP, O_{sel}, BA, POL, GAM, VC_{sel}			±1.0	μA
Input Current	I_{IL2}	$TEST_{IN}$	10	40	200	μA
High-Level Output Voltage	V_{OH}	STHR (STHL), I_{OH} = –1.0 mA	V_{DD1} – 0.5			V
Low-Level Output Voltage	V_{OL}	STHR (STHL), I_{OL} = +1.0 mA			0.5	V
VCOM Output Voltage	V_{OH2}	V_{DD2} = 5.0 V, I_O = –1.0 mA	V_{DD2} – 0.5			V
	V_{OL2}	V_{DD2} = 5.0 V, I_O = +1.0 mA			0.5	V
γ-Correction Power-supply Static Current Consumption	I_γ	V_0 = 5.0 V, V_4 = 0 V (when in γ-correction power mode)	100	200	400	μA
Driver Output Current (AMP drive)	I_{VOH1}	V_{DD2} = 5.0 V, V_{OUT} = V_X – 1.0 V **Note1** Input data: 1FH		–0.5	–0.15	mA
	I_{VOL1}	V_{DD2} = 5.0 V, V_{OUT} = V_X + 1.0 V **Note1** Input data: 20H	0.15	0.50		mA
Driver Output Current (Switch drive)	I_{VOH2}	V_{DD2} = 5.0 V, V_{OUT} = V_X – 1.0 V **Note1** Input data: 1FH		–50	–15	μA
	I_{VOL2}	V_{DD2} = 5.0 V, V_{OUT} = V_X + 1.0 V **Note1** Input data: 20H	15	40		μA
Driver Output Current (8-color display mode)	V_{OH3}	V_{DD2} = 5.0 V, I_O = –50 uA	V_{DD2} – 0.5			V
	V_{OL3}	V_{DD2} = 5.0 V, I_O = +50 uA			0.5	V
Output Voltage Deviation	ΔV_O	V_{DD1} = 2.5 V, V_{DD2} = 5.0 V, V_{OUT} = 2.5 V **Note1**		±10	±20	mV
Output Voltage Range	V_O	Input data: 00H to 3FH	V_{SS2} + 0.05		V_{DD2} – 0.05	V
Logic Part Dynamic Current Consumption	I_{DD1}	With no load **Note2**		0.4	0.8	mA
Driver Part Dynamic Current Consumption	I_{DD2}	V_{DD} = 5.0 V, with no load **Note2**		0.9	1.5	mA

Notes 1. V_X refers to the output voltage of analog output pins S_1 to S_{396}.

V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{396}.

2. f_{CLK} = 15 MHz, STB cycle = 60 μs, AP pulse width = 15 μs, BA = L (low power mode)

Switching Characteristics (T_A = –20 to +75°C, V_{DD1} = 2.2 to 3.6 V, V_{DD2} = 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

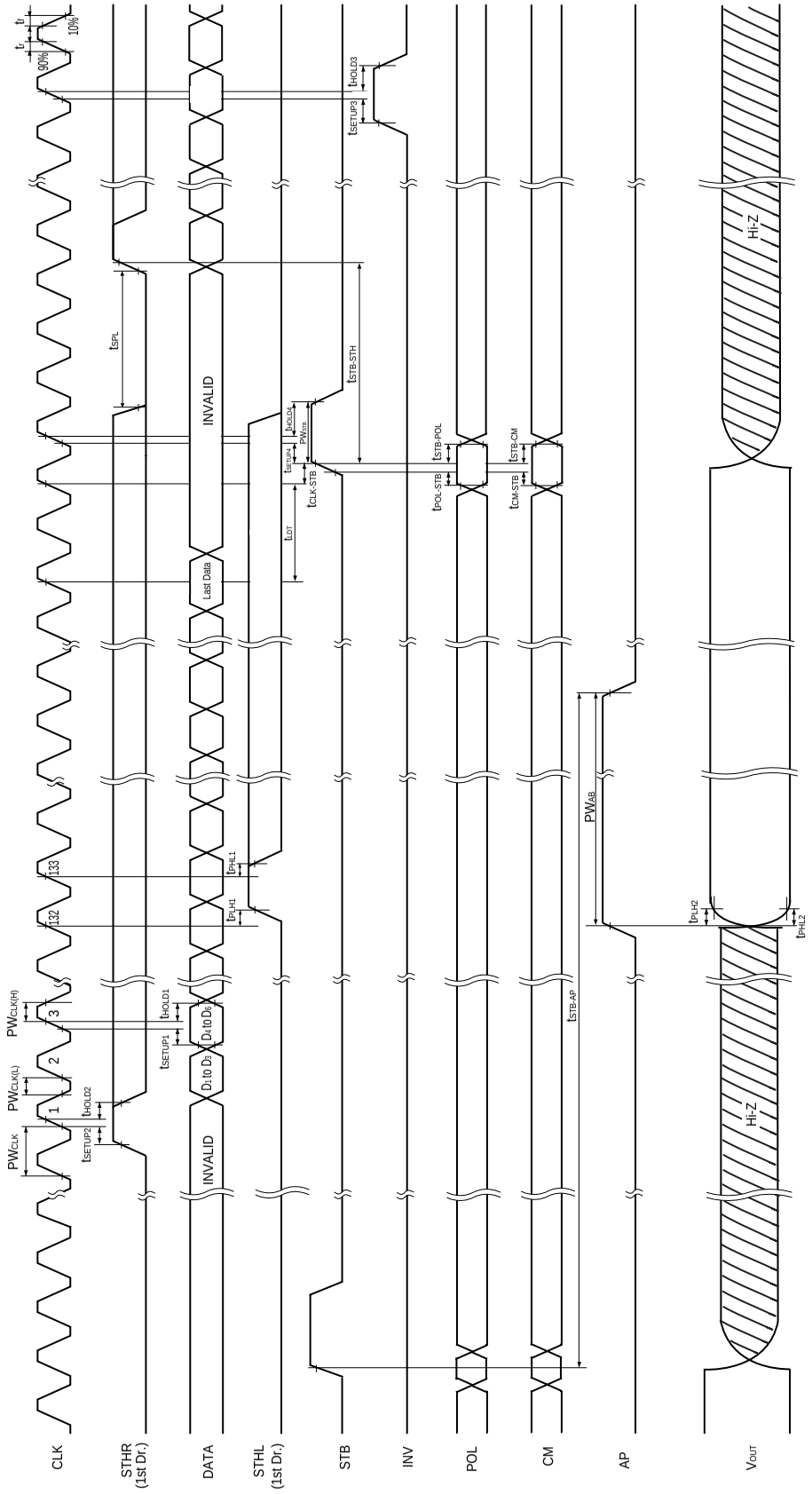
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	C_L = 15 pF			25	ns
	t_{PHL1}				25	ns
Driver Output Delay Time	t_{PLH2H}	C_L = 30 pF			12	μs
(High power mode)	t_{PHL2H}	AP↓ →V_{OUT} – 100 mV or V_{OUT} + 100 mV			12	μs
Driver Output Delay Time	t_{PLH2L}	C_L = 30 pF			15	μs
(Low power mode)	t_{PHL2L}	AP↓ →V_{OUT} – 100 mV or V_{OUT} + 100 mV			15	μs
Input Capacitance	C_{I1}	V_0 to V_4, T_A = 25°C		5	15	pF
	C_{I2}	Excluded V_0 to V_4, T_A = 25°C		10	15	pF

★ **Timing Requirements (T_A = –20 to +75°C, V_{DD1} = 2.2 to 3.6 V, V_{SS1} = 0 V, t_r = t_f = 10 ns)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		65			ns
Clock Pulse High Period	$PW_{CLK(H)}$		20			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		20			ns
Data Setup Time	t_{SETUP1}		20			ns
Data Hold Time	t_{HOLD1}		20			ns
Start Pulse Setup Time	t_{SETUP2}		20			ns
Start Pulse Hold Time	t_{HOLD2}		20			ns
Start Pulse Low Period	t_{SPL}		3			CLK
Last Data Timing	t_{LDT}		2			CLK
CLK-STB Time	$t_{CLK-STB}$	CLK↑ →STB↑	20			ns
STB Pulse Width	PW_{STB}		40			ns
Start Pulse Rising Time	$t_{STB-STH}$	STB↑ →STH↑	3			CLK
INV Set-up Time	t_{SETUP3}		20			ns
INV Hold Time	t_{HOLD3}		20			ns
STB Set-up Time	t_{SETUP4}		20			ns
STB Hold Time	t_{HOLD4}		20			ns
POL-STB Time	$t_{POL-STB}$		0			ns
STB-POL Time	$t_{STB-POL}$		40			ns
CM-STB Time	t_{CM-STB}		0			ns
STB-CM Time	t_{STB-CM}		40			ns
STB-AP Time	t_{STB-AP}	STB↑ →AP↓	20			μs
AP Pulse Width (High power mode)	PW_{APH}		12			μs
AP Pulse Width (Low power mode)	PW_{APL}	STB cycle 40μs, C_L = 30 pF	15			μs

Switching Characteristic Waveform (R,/L= H, OSEL=L)

Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.



[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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