

MOS INTEGRATED CIRCUIT

μ PD161623

528 OUTPUT TFT-LCD SOURCE DRIVER WITH RAM

DESCRIPTION

The μ PD161623 is a TFT-LCD source driver that includes display RAM.

This driver has 528 outputs, a display RAM capacity of 760,320 bits (176 pixels x 18 bits x 240 lines) and, can provide a 262,144-color display.

FEATURES

- TFT-LCD driver with on-chip display RAM
- I/O circuit power supply voltage: 1.7 to 3.6 V
- Logic power supply voltage: 2.5 to 3.6 V
- Driver power supply voltage: 4.3 to 5.5 V
- Display RAM: 176 x 18 x 240 bits
- Driver outputs: 528 output
- CPU interface: Serial, 18-bit/16-bit parallel interface selectable
- Colors: 262,144 colors/pixel
- On-chip VCOM generator
- On-chip timing generator
- On-chip oscillator

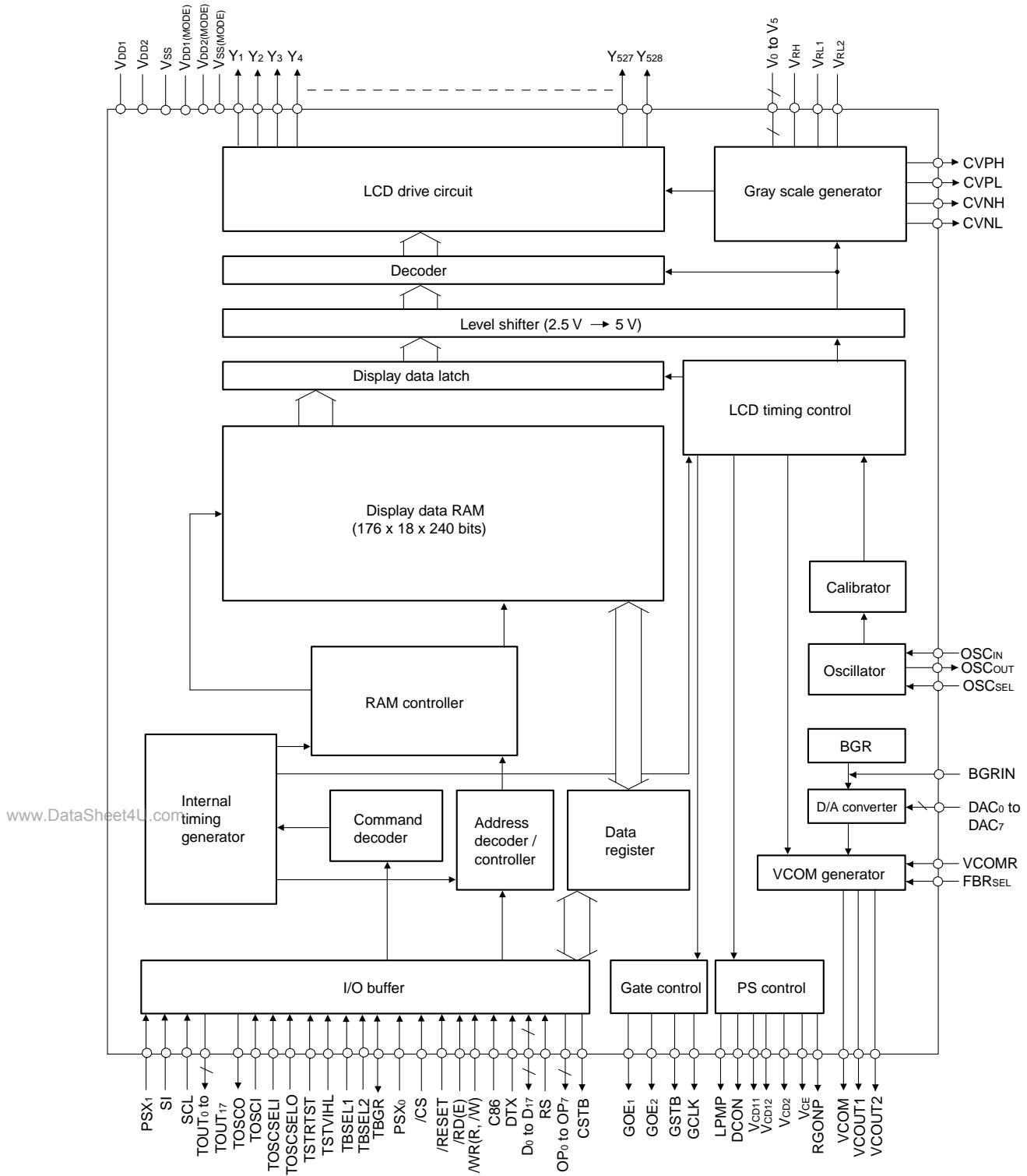
ORDERING INFORMATION

| Part Number | Package |
|-----------------|---------|
| μ PD161623P | Chip |

Remark Purchasing the above chip entails the exchange of documents such as a separate memorandum on product quality, so please contact one of our sales representatives.

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

1. BLOCK DIAGRAM



Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (PAD LAYOUT)

Chip size: 3.75 x 23.00 mm² TYP.

Bump size (output): 35 x 94 μ m² TYP.

Bump size (input & dummy): 80 x 86 μ m² TYP.

Alignment mark (Mark center, unit: μ m)

| | X | Y |
|----|-------|--------|
| M1 | -1690 | 11315 |
| M2 | -1690 | -11315 |

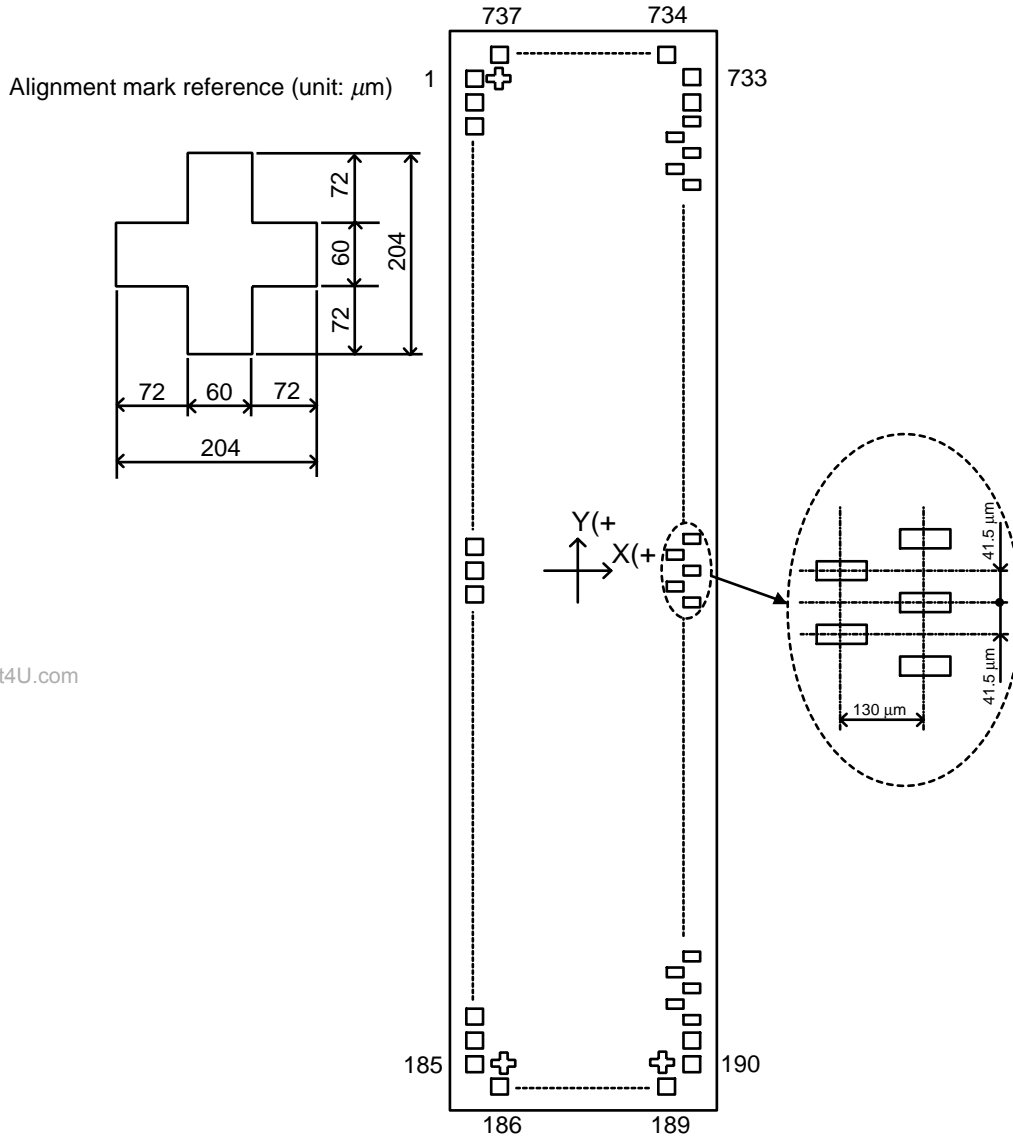


Table 2-1. Pad Layout (4/4)

| Pad No. | Pad Name | Pad Type | Pad Layout [μm] | | Pad No. | Pad Name | Pad Type | Pad Layout [μm] | |
|---------|----------|----------|-----------------|---------|---------|----------|----------|-----------------|----------|
| | | | X | Y | | | | X | Y |
| 631 | Y100 | A | 1745.00 | 7036.50 | 701 | Y30 | A | 1745.00 | 9941.50 |
| 632 | Y99 | A | 1615.00 | 7078.00 | 702 | Y29 | A | 1615.00 | 9983.00 |
| 633 | Y98 | A | 1745.00 | 7119.50 | 703 | Y28 | A | 1745.00 | 10024.50 |
| 634 | Y97 | A | 1615.00 | 7161.00 | 704 | Y27 | A | 1615.00 | 10066.00 |
| 635 | Y96 | A | 1745.00 | 7202.50 | 705 | Y26 | A | 1745.00 | 10107.50 |
| 636 | Y95 | A | 1615.00 | 7244.00 | 706 | Y25 | A | 1615.00 | 10149.00 |
| 637 | Y94 | A | 1745.00 | 7285.50 | 707 | Y24 | A | 1745.00 | 10190.50 |
| 638 | Y93 | A | 1615.00 | 7327.00 | 708 | Y23 | A | 1615.00 | 10232.00 |
| 639 | Y92 | A | 1745.00 | 7368.50 | 709 | Y22 | A | 1745.00 | 10273.50 |
| 640 | Y91 | A | 1615.00 | 7410.00 | 710 | Y21 | A | 1615.00 | 10315.00 |
| 641 | Y90 | A | 1745.00 | 7451.50 | 711 | Y20 | A | 1745.00 | 10356.50 |
| 642 | Y89 | A | 1615.00 | 7493.00 | 712 | Y19 | A | 1615.00 | 10398.00 |
| 643 | Y88 | A | 1745.00 | 7534.50 | 713 | Y18 | A | 1745.00 | 10439.50 |
| 644 | Y87 | A | 1615.00 | 7576.00 | 714 | Y17 | A | 1615.00 | 10481.00 |
| 645 | Y86 | A | 1745.00 | 7617.50 | 715 | Y16 | A | 1745.00 | 10522.50 |
| 646 | Y85 | A | 1615.00 | 7659.00 | 716 | Y15 | A | 1615.00 | 10564.00 |
| 647 | Y84 | A | 1745.00 | 7700.50 | 717 | Y14 | A | 1745.00 | 10605.50 |
| 648 | Y83 | A | 1615.00 | 7742.00 | 718 | Y13 | A | 1615.00 | 10647.00 |
| 649 | Y82 | A | 1745.00 | 7783.50 | 719 | Y12 | A | 1745.00 | 10688.50 |
| 650 | Y81 | A | 1615.00 | 7825.00 | 720 | Y11 | A | 1615.00 | 10730.00 |
| 651 | Y80 | A | 1745.00 | 7866.50 | 721 | Y10 | A | 1745.00 | 10771.50 |
| 652 | Y79 | A | 1615.00 | 7908.00 | 722 | Y9 | A | 1615.00 | 10813.00 |
| 653 | Y78 | A | 1745.00 | 7949.50 | 723 | Y8 | A | 1745.00 | 10854.50 |
| 654 | Y77 | A | 1615.00 | 7991.00 | 724 | Y7 | A | 1615.00 | 10896.00 |
| 655 | Y76 | A | 1745.00 | 8032.50 | 725 | Y6 | A | 1745.00 | 10937.50 |
| 656 | Y75 | A | 1615.00 | 8074.00 | 726 | Y5 | A | 1615.00 | 10979.00 |
| 657 | Y74 | A | 1745.00 | 8115.50 | 727 | Y4 | A | 1745.00 | 11020.50 |
| 658 | Y73 | A | 1615.00 | 8157.00 | 728 | Y3 | A | 1615.00 | 11062.00 |
| 659 | Y72 | A | 1745.00 | 8198.50 | 729 | Y2 | A | 1745.00 | 11103.50 |
| 660 | Y71 | A | 1615.00 | 8240.00 | 730 | Y1 | A | 1615.00 | 11145.00 |
| 661 | Y70 | A | 1745.00 | 8281.50 | 731 | DUMMY | A | 1745.00 | 11206.50 |
| 662 | Y69 | A | 1615.00 | 8323.00 | 732 | DUMMY | A | 1745.00 | 11257.50 |
| 663 | Y68 | A | 1745.00 | 8364.50 | 733 | DUMMY | A | 1745.00 | 11307.50 |
| 664 | Y67 | A | 1615.00 | 8406.00 | 734 | DUMMY | B | 1340.00 | 11374.00 |
| 665 | Y66 | A | 1745.00 | 8447.50 | 735 | DUMMY | B | 440.00 | 11374.00 |
| 666 | Y65 | A | 1615.00 | 8489.00 | 736 | DUMMY | B | -460.00 | 11374.00 |
| 667 | Y64 | A | 1745.00 | 8530.50 | 737 | DUMMY | B | -1360.00 | 11374.00 |
| 668 | Y63 | A | 1615.00 | 8572.00 | | | | | |
| 669 | Y62 | A | 1745.00 | 8613.50 | | | | | |
| 670 | Y61 | A | 1615.00 | 8655.00 | | | | | |
| 671 | Y60 | A | 1745.00 | 8696.50 | | | | | |
| 672 | Y59 | A | 1615.00 | 8738.00 | | | | | |
| 673 | Y58 | A | 1745.00 | 8779.50 | | | | | |
| 674 | Y57 | A | 1615.00 | 8821.00 | | | | | |
| 675 | Y56 | A | 1745.00 | 8862.50 | | | | | |
| 676 | Y55 | A | 1615.00 | 8904.00 | | | | | |
| 677 | Y54 | A | 1745.00 | 8945.50 | | | | | |
| 678 | Y53 | A | 1615.00 | 8987.00 | | | | | |
| 679 | Y52 | A | 1745.00 | 9028.50 | | | | | |
| 680 | Y51 | A | 1615.00 | 9070.00 | | | | | |
| 681 | Y50 | A | 1745.00 | 9111.50 | | | | | |
| 682 | Y49 | A | 1615.00 | 9153.00 | | | | | |
| 683 | Y48 | A | 1745.00 | 9194.50 | | | | | |
| 684 | Y47 | A | 1615.00 | 9236.00 | | | | | |
| 685 | Y46 | A | 1745.00 | 9277.50 | | | | | |
| 686 | Y45 | A | 1615.00 | 9319.00 | | | | | |
| 687 | Y44 | A | 1745.00 | 9360.50 | | | | | |
| 688 | Y43 | A | 1615.00 | 9402.00 | | | | | |
| 689 | Y42 | A | 1745.00 | 9443.50 | | | | | |
| 690 | Y41 | A | 1615.00 | 9485.00 | | | | | |
| 691 | Y40 | A | 1745.00 | 9526.50 | | | | | |
| 692 | Y39 | A | 1615.00 | 9568.00 | | | | | |
| 693 | Y38 | A | 1745.00 | 9609.50 | | | | | |
| 694 | Y37 | A | 1615.00 | 9651.00 | | | | | |
| 695 | Y36 | A | 1745.00 | 9692.50 | | | | | |
| 696 | Y35 | A | 1615.00 | 9734.00 | | | | | |
| 697 | Y34 | A | 1745.00 | 9775.50 | | | | | |
| 698 | Y33 | A | 1615.00 | 9817.00 | | | | | |
| 699 | Y32 | A | 1745.00 | 9858.50 | | | | | |
| 700 | Y31 | A | 1615.00 | 9900.00 | | | | | |

3. PIN FUNCTIONS

3.1 Power Supply System Pins

| Symbol | Pin Name | Pad No. | I/O | Function |
|--|---|--|-----|---|
| V _{DD1} | Logic power supply | 77, 95 | – | Power supply pin for logic circuit |
| V _{DD2} | I/O power supply | 96, 108, 109 | – | Power supply pin for I/O buffer |
| V _S | Driver power supply | 103, 104 | – | Power supply pin for driver circuit |
| V _{SS} | Ground | 94, 97, 98, 105 | – | Ground pin for logic and driver circuits |
| V ₀ to V ₅ V _{RH} V _{RL1} , V _{RL2} | Power supply for γ -curve correction | 120 to 125, 119, 126, 127 | – | The μ PD161623 includes power supplies and registers for the γ -curve, so if the characteristics of the γ -curve and LCD panel in the μ PD161623 match, leave V ₀ to V ₅ , V _{RH} , V _{RL1} , V _{RL2} open. If some kind of correction is required, adjust the γ -curve by connecting registers between the V ₀ to V ₅ , V _{RH} , V _{RL1} , V _{RL2} pins (see 5.9 γ-Curve Correction Power Supply Circuit). |
| V _{DD1 (MODE)} | Mode setting pull-up power supply | 81, 85 | – | Pull-up power supply pin for mode setting |
| V _{DD2 (MODE)} | Mode setting pull-down power supply | 42, 116 | – | Pull-down power supply pin for mode setting |
| V _{SS (MODE)} | Mode setting ground | 35, 44, 46, 48, 68, 74, 79, 83, 113, 118, 128, 140 | – | Ground pin for mode setting |

3.2 Logic System Pins

(1/2)

| Symbol | Pin Name | Pad No. | I/O | Function | | | | | | |
|------------------|---------------------------|---------|-------|---|------------------|--------------------|---|---------------------------|---|---------------------------|
| PSX ₀ | CPU interface selection | 80 | Input | This pin is used to select the CPU interface mode. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>PSX₀</th> <th>CPU Interface Mode</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>18-bit parallel interface</td> </tr> <tr> <td>L</td> <td>16-bit parallel interface</td> </tr> </tbody> </table> | PSX ₀ | CPU Interface Mode | H | 18-bit parallel interface | L | 16-bit parallel interface |
| PSX ₀ | CPU Interface Mode | | | | | | | | | |
| H | 18-bit parallel interface | | | | | | | | | |
| L | 16-bit parallel interface | | | | | | | | | |
| /CS | Chip select | 69 | Input | This pin is used for chip select signals. When /CS = L, the chip is active and can perform data input/output operations including command and data I/O. | | | | | | |
| /RESET | Reset | 70 | Input | When /RESET is L, an internal reset is performed. The reset operation is executed at the /RESET signal level. Be sure to perform reset via this pin at power application. | | | | | | |
| /RD (E) | Read (Enable) | 73 | Input | When i80 series parallel data transfer (/RD) has been selected, the signal at this pin is used to enable read operations. Data is output to the data bus only when this pin is low. When M68 series parallel data transfer (E) has been selected, the signal at this pin is used to enable read/write operations. | | | | | | |
| /WR (R, /W) | Write (Read/write) | 72 | Input | When i80 series parallel data transfer (/WR) has been selected, the signal at this pin is used to enable write operations. Data is written at the rising edge of this signal. When M68 series parallel data transfer (R, /W) and serial data has been selected, this pin is used to determine the direction of data transfer. L: Write H: Read | | | | | | |
| C86 | Select interface | 82 | Input | This pin is used to switch between interface modes (i80 series CPU or M68 series CPU). L: Selects i80 series CPU mode H: Selects M68 series CPU mode | | | | | | |

(2/2)

| Symbol | Pin Name | Pad No. | I/O | Function |
|------------------------------------|------------------------------|------------|--------|---|
| D ₀ to D ₁₇ | Data bus | 67 to 50 | I/O | These pins comprise 18-bit bi-directional data. When the chip is not selected, D ₀ to D ₁₇ are in high impedance mode. |
| RS | Data/command selection | 71 | Input | When parallel data transfer has been selected, this pin is usually connected to the least significant bit of the standard CPU address bus and is used to distinguish between data from display data and commands. RS = H: Indicates that data from D ₀ to D ₁₇ is display data. RS = L: Indicates that data from D ₀ to D ₁₇ is commands. |
| DTX | Data major select | 84 | Input | When parallel data transfer has been selected, this pin is selected data major selection that inputs display data through serial interface. DTX = H: 1-pixel/18-bit mode DTX = L: 1-pixel/16-bit mode |
| OSC _{SEL} | Oscillation signal selection | 43 | Input | This pin is for oscillation signal selection. When is used external resistance connected oscillation circuit, this pin sets H. When in used CR internal oscillation circuit, this pin sets L. OSC _{SEL} = H: External resistance connected oscillation circuit select OSC _{SEL} = L: CR internal oscillation circuit select |
| OSC _{IN} | Oscillation signal | 47 | Input | This pin is for oscillation signal input. OSC _{SEL} = H: Connect 42 kΩ resistance between OSC _{IN} and OSC _{OUT} . (240 line, in case of NGO = 0) OSC _{SEL} = L: Leave it open. |
| OSC _{OUT} | Oscillation signal | 45 | Output | This pin is for oscillation signal input. OSC _{SEL} = H: Connect 42 kΩ resistance between OSC _{IN} and OSC _{OUT} . (240 line, in case of NGO = 0) OSC _{SEL} = L: Leave it open. |
| CSTB | GSTB logic signal | 49 | Output | This pin outputs STB signal for gate driver leveled by interface power supply voltage (V _{DD1}). This output signal is reverse signal of GSTB. |
| OP ₀ to OP ₇ | Output port | 141 to 148 | Output | This is a general-purpose output port. The status of these pins (H or L) can be write via a command. Leave open when in unused. |

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3.3 Gate Driver IC Control Pins

| Symbol | Pin Name | Pad No. | I/O | Function |
|------------------|--|---------|--------|--|
| GOE ₁ | OE ₁ output for gate driver | 151 | Output | This pin is an output pin for the low power mode (for the OE ₁). Connect to the OE ₁ pin of the gate driver. Timing signal for output, refer to 5.4 Display Timing Generator . |
| GOE ₂ | OE ₂ output for gate driver | 152 | Output | This pin is the OE ₂ output for the gate driver. Connect to the OE ₂ pin of the gate driver. Timing signal for output, refer to 5.4 Display Timing Generator . |
| GSTB | STB output for gate driver | 149 | Output | This pin is the STB output for the gate driver. Connect to the STVR or STVL pin of the gate driver. Timing signal for output, refer to 5.4 Display Timing Generator . |
| GCLK | CLK output for gate driver | 150 | Output | This pin is the CLK output for the gate driver. Connect to the CLK pin of the gate driver. |

3.4 Power Supply Control Pins

| Symbol | Pin Name | Pad No. | I/O | Function |
|---------------------------------------|------------------------------------|---------|--------|---|
| LPMP | Low power mode signal | 90 | Output | Low power mode control signal output pin (for power supply IC). This pin connects to LPM pin of power supply IC. |
| DCON | DC/DC converter control | 92 | Output | DC/DC converter ON/OFF signal pin for power supply IC. This pin connects DCON pin of power supply IC. |
| RGONP | Regulator control | 91 | Output | Regulator ON/OFF control signal pin for power supply IC. This pin connects to RGONP pin of power supply IC. |
| V _{CD11} , V _{CD12} | V _{DD1} booster selection | 89, 88 | Output | Control signal to select x4/x5/x6/x7 booster of power supply IC for V _{DD1} . Connect to the V _{CD11} and V _{CD12} pins of the power supply IC. |
| V _{CD2} | V _{DD2} booster selection | 87 | Output | Control signal to select x2/x3 booster of power supply IC for V _{DD2} . Connect to the V _{CD2} pin of the power supply IC. |
| V _{CE} | V _O level selection | 86 | Output | Signal for selecting the level of the power supply IC booster voltage, to be used for the maximum voltage of V _O . Selects that the booster voltage level is either the same level as V _{DD1} or a multiple of minus 1. Connect to the V _{CE} pin of the power supply IC. |

3.5 Driver-Related Pins

(1/2)

| Symbol | Pin Name | Pad No. | I/O | Function |
|------------------------------------|----------------------------------|---------------------------|--------|---|
| Y ₁ to Y ₅₂₈ | Source output | 730 to 468, 457 to 193 | Output | These pins are source output pins. |
| VCOM | COM adjustment | 110 | Output | This pin is the common adjustment output pin. |
| V _{COU1} | Center rectangle signal output | 106, 107 | Output | This pin is the center rectangle signal output (V _{P-P}) for common modulation between 0 V and V _s . |
| V _{COU2} | Center rectangle signal output | 93 | Output | This pin is the center rectangle signal output (V _{P-P}) for common modulation between 0 V and V _{DD2} . |
| BGRIN | External-power supply connect | 115 | Input | This is an external-power supply input pin for VCOM. This pin is valid when BGRS (power supply control register 1: R25) = 1. In this case, the reference voltage of the amplifier for setting the common waveform center value is input from outside the μ PD161623. When BGRS = 0, the μ PD161623 internal voltage is set as the reference voltage of the amplifier for setting the common waveform center value. In this case, leave it open. |
| V _{COMR} | VCOM setting register connection | 114 | Input | This pin connects an external feedback resistor for setting VCOM. This pin is valid when FBR _{SEL} = L. In this case, connect a feedback resistor between the VCOM pin and GND. When FBR _{SEL} = H, the amplifier for setting the common waveform center value operates as a voltage follower. In this case, leave it open. |

(2/2)

| Symbol | Pin Name | Pad No. | I/O | Function |
|--------------------------------------|---|-------------------|--------|--|
| FBR _{SEL} | VCOM setting external circuit select | 117 | Input | This pin is used to select the method of adjusting the amplifier for setting the common waveform center value used to set the COMMON drive waveform center level. FBR _{SEL} = H: Voltage follower circuit used (VCOMR connected to VCOM internally) FBR _{SEL} = L: External feedback resistor used |
| ★ CVPH, CVPL, CVNH, CVNL | Basis power supply pin for γ -corrected power supplies | 102, 101, 100, 99 | Output | This is operational amplifier output pin for the g-corrected power supplies. Normally, this pin connects capacitor of 1.0 μ F. |
| DAC ₀ to DAC ₇ | D/A converter value setting | 139 to 132 | Input | These pins set the reference voltage of the amplifier for setting the VCOM value used to set the COMMON drive waveform center level. These pins are valid when the VCOM output center value setting register (R29) = 00H and BGRS (R25: D ₆) = 0. For more details, refer to 5.5 Common Adjustment Circuit . |

Remark T.B.D. (To be determined.)

3.6 Test or Other Pins

| Symbol | Pin Name | Pad No. | I/O | Function |
|---|-------------------|---|--------|---|
| TOUT ₀ to TOUT ₁₇ , TOSCO | Source output | 34 to 17, 41 | Output | This is output pin when μ PD161623 is in test mode. Normally, leave it open. |
| TSTRTST, TSTVIHL, TOSCI, TOSCSELI, TOSCSELO, TBSEL1, TBSEL2, PSX ₁ | COM adjustment | 37, 36, 40, 39, 38, 129, 130, 78 | Output | These pins are to set up test mode of μ PD161623. Normally, fixed it to V _{SS} . |
| SI, SCL | Test input | 75, 76 | Input | These pins are to set up test mode of μ PD161623. Normally, fixed it to either V _{DD1} or V _{SS} . |
| TBGR | Test input/output | 131 | I/O | This is output pin when μ PD161623 is in test mode. Normally, leave it open. |
| DUMMY | Dummy | 1 to 16, 111, 112, 153 to 192, 458 to 467, 731 to 737 | – | Dummy pin |

4. PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The I/O circuit types of each pin and recommended connection of unused pins are described below.

| Pin Name | Input Type | I/O | Power Supply | Recommended Connection of Unused Pins | Note |
|---|-----------------|--------|------------------|---|------|
| PSX ₀ | Schmitt trigger | Input | V _{DD1} | Mode setting pin | 1 |
| /RESET | Schmitt trigger | Input | V _{DD1} | Always reset on power application | – |
| /RD(E) | Schmitt trigger | Input | V _{DD1} | Connect to V _{DD1} (when i80 series interface) | – |
| C86 | Schmitt trigger | Input | V _{DD1} | Mode setting pin | 1 |
| D ₀ to D ₁₇ | Schmitt trigger | I/O | V _{DD1} | – | – |
| RS | Schmitt trigger | Input | V _{DD1} | Register setting pin | 2 |
| OP ₀ to OP ₇ | – | Output | V _{DD2} | Leave open | – |
| OSC _{IN} | CMOS | Input | V _{DD2} | Input external clock (in OSC _{SEL} = H mode) | – |
| OSC _{OUT} | CMOS | Input | V _{DD2} | Leave open (in OSC _{SEL} = H mode) | – |
| CSTB | – | Output | V _{DD1} | Leave open | – |
| OSC _{SEL} | Schmitt trigger | Input | V _{DD2} | Mode setting pin | 3 |
| GOE ₁ | – | Output | V _{DD2} | Always connect to the gate driver | – |
| GOE ₂ | – | Output | V _{DD2} | Always connect to the gate driver | – |
| GSTB | – | Output | V _{DD2} | Always connect to the gate driver | – |
| GCLK | – | Output | V _{DD2} | Always connect to the gate driver | – |
| LPMP | – | Output | V _{DD2} | Leave open | – |
| DCON | – | Output | V _{DD2} | Always connect to the power IC | – |
| RGONP | – | Output | V _{DD2} | Always connect to the power IC | – |
| V _{CD11} , V _{CD12} | – | Output | V _{DD2} | Always connect to the power IC | – |
| V _{CD2} | – | Output | V _{DD2} | Always connect to the power IC | – |
| V _{CE} | – | Output | V _{DD2} | Always connect to the power IC | – |
| V _{COM} | – | Output | V _s | Leave open (FRB _{SEL} = H) | – |
| VCOUT1 | – | Output | V _s | Leave open | – |
| VCOUT2 | – | Output | V _{DD2} | Leave open | – |
| BGRIN | – | Input | V _s | Leave open (BGRS = 0 [R25]) | – |
| VCOMR | – | Input | V _s | Leave open (FRB _{SEL} = H) | – |
| TOUT ₀ to TOUT ₁₇ | – | Output | V _{DD2} | Leave open | – |
| TOSCO | – | Output | V _{DD2} | Leave open | – |
| TSTRST | – | Input | V _{DD2} | Connect to V _{SS} | – |
| TSTVIHL | – | Input | V _{DD2} | Connect to V _{SS} | – |
| TOSCI | – | Input | V _{DD2} | Connect to V _{SS} | – |
| TOSCSELI | – | Input | V _{DD2} | Connect to V _{SS} | – |
| TOSCSELO | – | Input | V _{DD2} | Connect to V _{SS} | – |
| TBSEL1 | – | Input | V _{DD2} | Connect to V _{SS} | – |
| TBSEL2 | – | Input | V _{DD2} | Connect to V _{SS} | – |
| TBGR | – | Input | V _{DD2} | Connect to V _{SS} | – |
| PSX ₁ | – | Input | V _{DD1} | Connect to V _{SS} | – |
| SCL | – | Input | V _{DD1} | Connect to V _{DD1} or V _{SS} | – |
| SI | – | Input | V _{DD1} | Connect to V _{DD1} or V _{SS} | – |
| DTX | Schmitt trigger | Input | V _{DD1} | Connect to V _{DD1} or V _{SS} | 1 |
| FBR _{SEL} | CMOS | Input | V _{DD2} | Connect to V _{DD2} or V _{SS} | 3 |

- Notes**
1. Connect to V_{DD1} or V_{SS}, depending on the mode selected.
 2. Input either H or L by CPU, depending on the register selected.
 3. Connect to V_{DD2} or V_{SS}, depending on the mode selected.

5. DESCRIPTION OF FUNCTIONS

5.1 CPU Interface

5.1.1 Selection of interface type

The μ PD161623 chip transfers data using a 18-bit bi-directional data bus (D₁₇ to D₀), 16-bit bi-directional data bus (D₁₅ to D₀). Setting the polarity of the PSX₀ pin as either H or L enables the selections shown in Table 5–1 below.

Table 5–1.

| PSX ₀ | Mode | /CS | RS | /RD (E) | /WR (R, /W) | C86 | D ₁₇ , D ₁₆ | D ₁₅ to D ₈ | D ₇ to D ₀ |
|------------------|-----------------|-----|----|---------|-------------|-----|-----------------------------------|-----------------------------------|----------------------------------|
| H | 18-bit parallel | /CS | RS | /RD (E) | /WR (R, /W) | C86 | D ₁₇ , D ₁₆ | D ₁₅ to D ₈ | D ₇ to D ₀ |
| L | 16-bit parallel | /CS | RS | /RD (E) | /WR (R, /W) | C86 | Hi-Z ^{Note} | D ₁₅ to D ₈ | D ₇ to D ₀ |

Note Hi-Z: High impedance

5.1.2 Selection of data transfer mode

In the μ PD161623, when the 16-bit parallel interface is selected, there are two types of modes to transfer data to display RAM. The mode can be selected as follows with the DTX command.

When using the 16-bit parallel interface and the 1-pixel/18-bit mode (DTX = H) is selected, one pixel of display data must be transferred every two words, as shown in Figure 5–4. At this time, the data of DB₁₅ to DB₉ is treated as invalid data.

When the 1-pixel/16-bit mode (DTX = L) is selected, one pixel of display data is transferred every word. However, because one pixel data is 16 bits long, the display color range is restricted to 65,536.

When the 18-bit parallel interface is used, the data transfer method is fixed to 1-pixel/18-bit mode, regardless of the setting of the DTX pin.

Because the display RAM in the μ PD161623 has a 1-pixel/18-bit configuration, when using the 1-pixel/16-bit mode (DTX = L), it will be necessary to add supplementary data for the two-bit data deficiency that occurs when (16-bit) data is transferred from the CPU.

For the relationship between the display data and the supplementary data set by the data supplement register, refer to Figure 5–3.

Table 5–2.

| PSX ₀ | Interface Mode | DTX | Mode |
|------------------|-----------------|-------------------|----------------|
| H | 18-bit parallel | X ^{Note} | 1-pixel/18-bit |
| L | 16-bit parallel | H | 1-pixel/18-bit |
| | | L | 1-pixel/16-bit |

Note X: Don't care (H or L)

Table 5-3. Data Supplement Register

| Supplemented Display Data | |
|---------------------------|--|
| CD12 | When 1-pixel/16-bit mode is used, the value set by this flag is stored in the display RAM as D ₁₂ data. |
| CD0 | When 1-pixel/16-bit mode is used, the value set by this flag is stored in the display RAM as D ₀ data. |

Figure 5-1. Relationship between Data Bus and Display RAM Data (18-bit parallel interface)

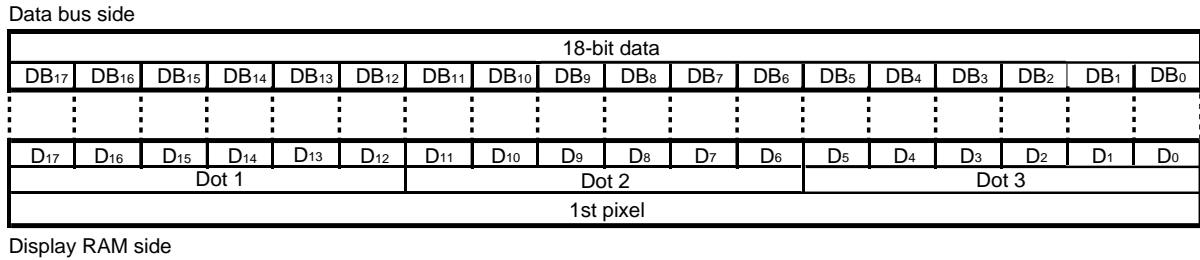
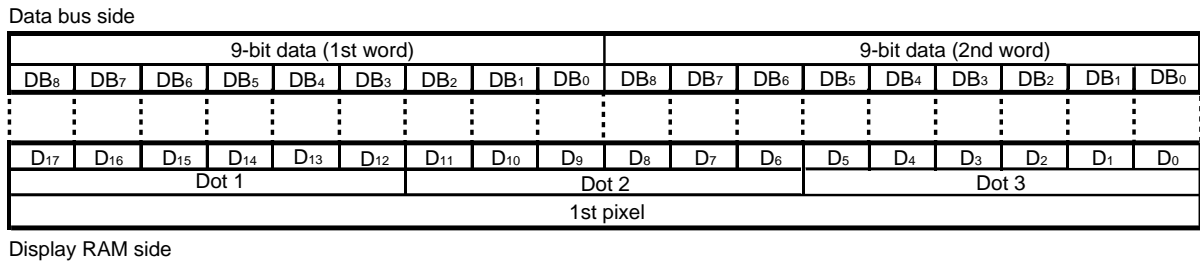


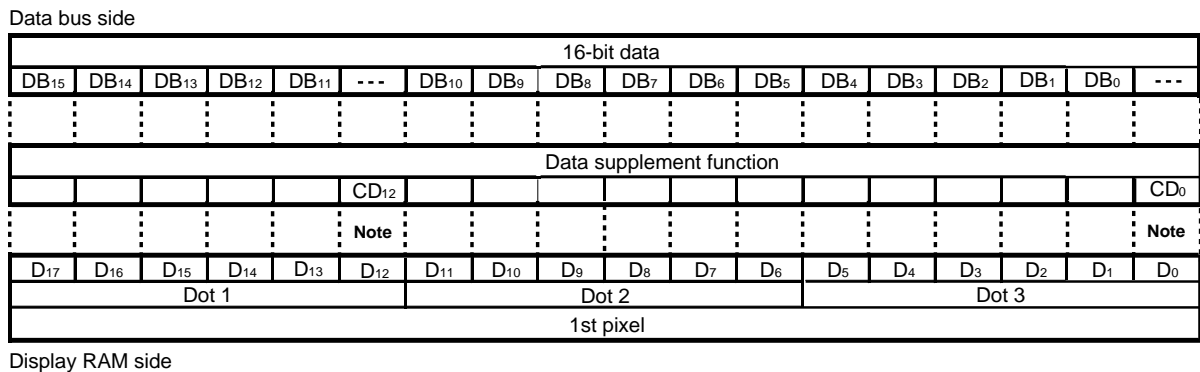
Figure 5-2. Relationship between Data Bus and Display RAM Data (1-pixel/18-bit mode [DTX = H], 16-bit parallel interface)



Note When in used 16-bit parallel interface, DB₁₅ to DB₉ is treated as invalid data.

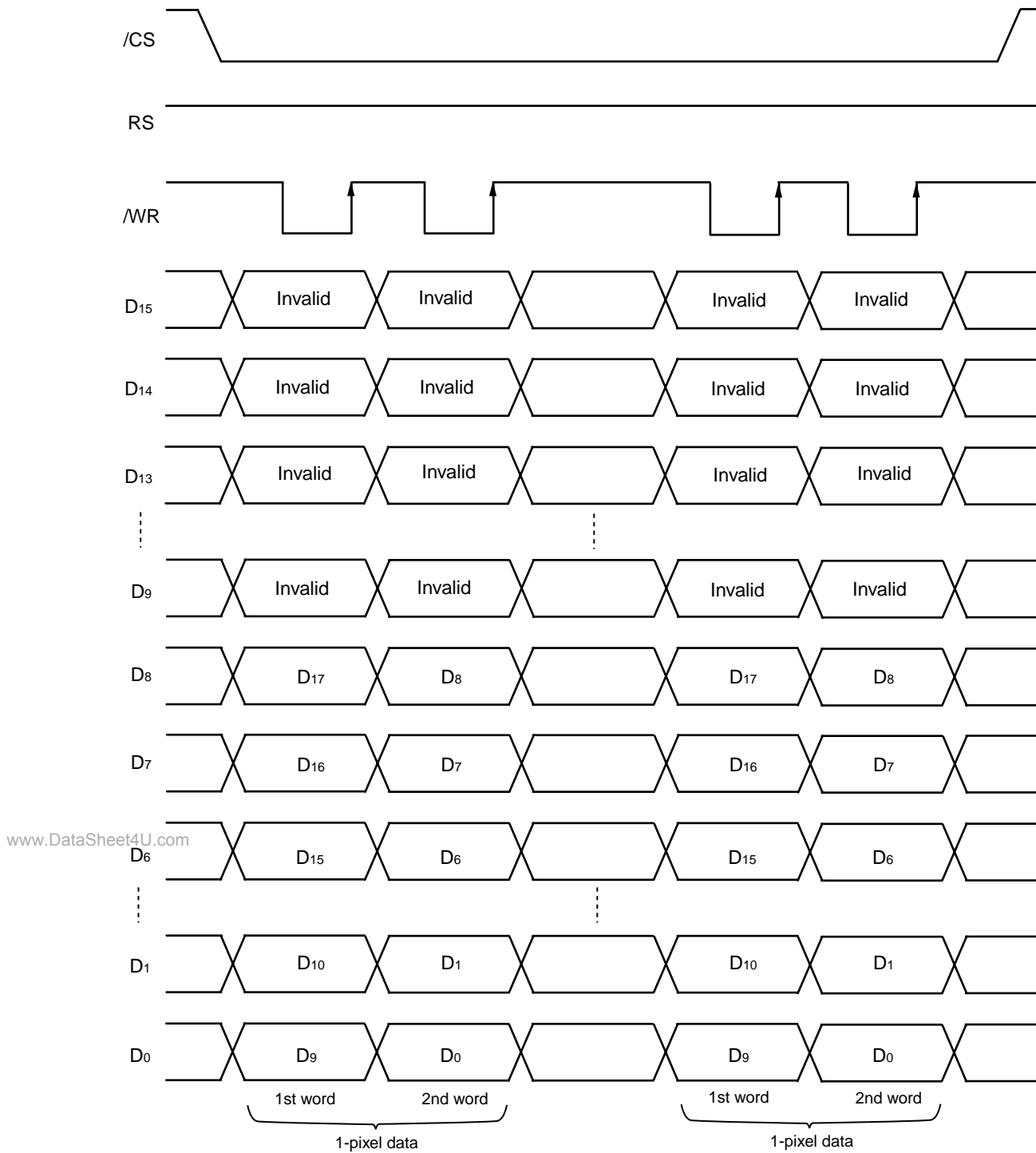
Figure 5-3. Relationship between Data Bus and Display RAM Data (1-pixel/16-bit mode [DTX = L], 16-bit parallel interface)

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Note When In used 16-bit parallel interface, display RAM data D₁₂ and D₀ are added to the 16-bit data by the data supplement register (R4), and written to the display RAM as 18-bit data.

Figure 5-4. 16-bit Parallel Interface Date Transfer (1-pixel/18-bit mode [DTX = H])



5.1.3 Parallel interface

When the parallel interface has been selected, setting the C86 pin as either H or L enables a direct connection to an i80 series or M68 series CPU (see Table 5–4 below).

Table 5–4.

| C86 | Mode | /RD (E) | /WR (R, /W) | PSX ₀ | D ₁₇ , D ₁₆ | D ₁₅ to D ₈ | D ₇ to D ₀ |
|-----|----------------|---------|-------------|------------------|-----------------------------------|-----------------------------------|----------------------------------|
| H | M68 series CPU | E | R, /W | H | D ₁₇ , D ₁₆ | D ₁₅ to D ₈ | D ₇ to D ₀ |
| | | | | L | Hi-Z ^{Note} | D ₁₅ to D ₈ | D ₇ to D ₀ |
| L | i80 series CPU | /RD | /WR | H | D ₁₇ , D ₁₆ | D ₁₅ to D ₈ | D ₇ to D ₀ |
| | | | | L | Hi-Z ^{Note} | D ₁₅ to D ₈ | D ₇ to D ₀ |

Note Hi-Z: High impedance. Leave it open.

The data bus signal is identified according to the combination of the RS, /RD (E), and /WR (R, /W) signals, as shown in the following Table 5–5.

★

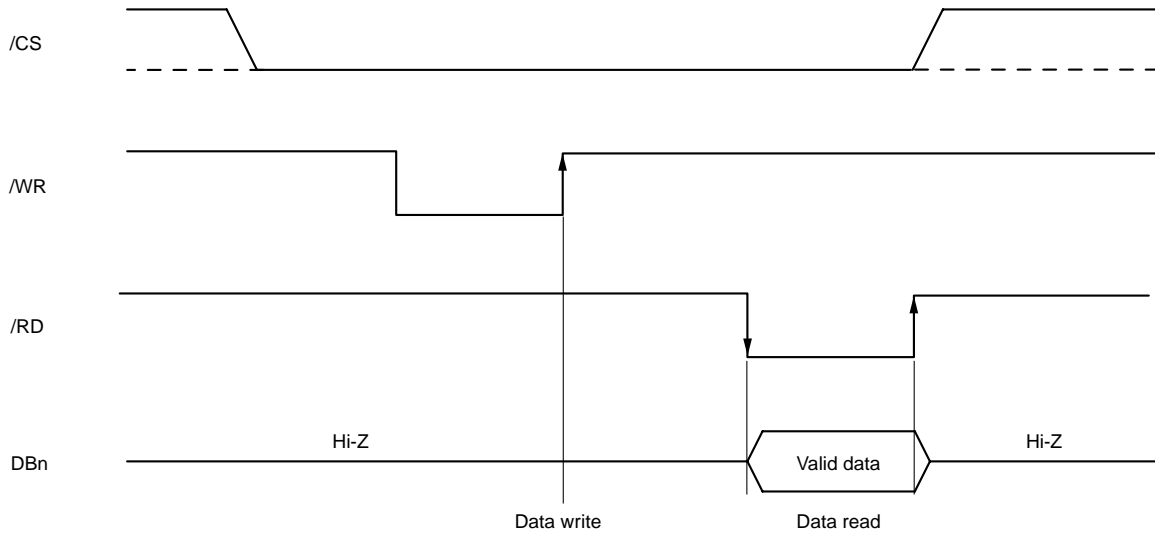
Table 5–5.

| Common | M68 series CPU | i80 series CPU | | Function |
|--------|----------------|----------------|-----|---------------------------------|
| | R, /W | /RD | /WR | |
| H | H | L | H | Read display data |
| H | L | H | L | Write display data |
| L | H | L | H | Prohibited |
| L | L | H | L | Write to control index register |

(1) i80 Series Parallel Interface

When i80 series parallel data transfer has been selected, data is written to the μ PD161623 at L period of the /WR signal. The data is output to the data bus when the /RD signal is L.

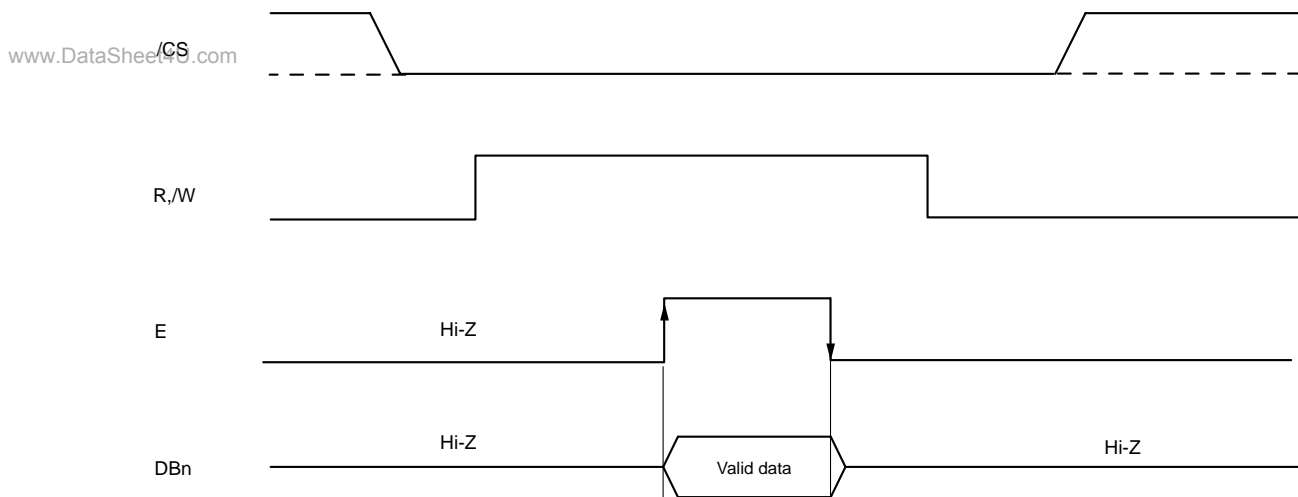
Figure 5-5. i80 Series Interface Data Bus Status



(2) M68 Series Parallel Interface

When M68 series parallel data transfer has been selected, data is written at the H period of the E signal when the R,/W signal is L. In a data read operation, data is output at the rising edge of the E signal in a period when the R,/W signal is H. The data bus is released (Hi-Z) at the falling edge of the E signal.

Figure 5-6. M68 Series Interface Data Bus Status (When data read)



5.1.4 Chip select

The μ PD161623 has two chip select pins (/CS). The CPU parallel interface can be used only when /CS = L. When the chip select pin is inactive, D₀ to D₁₇ are set to high impedance (invalid) and input of RS, /RD, or /WR is not active.

5.1.5 Access to display data RAM and internal registers

When the CPU accessed the μ PD161623, the CPU only has to satisfy the requirement of the cycle time (t_{CYC}) and can transfer data at high speeds. Usually, it is not necessary for the CPU to take wait time into consideration.

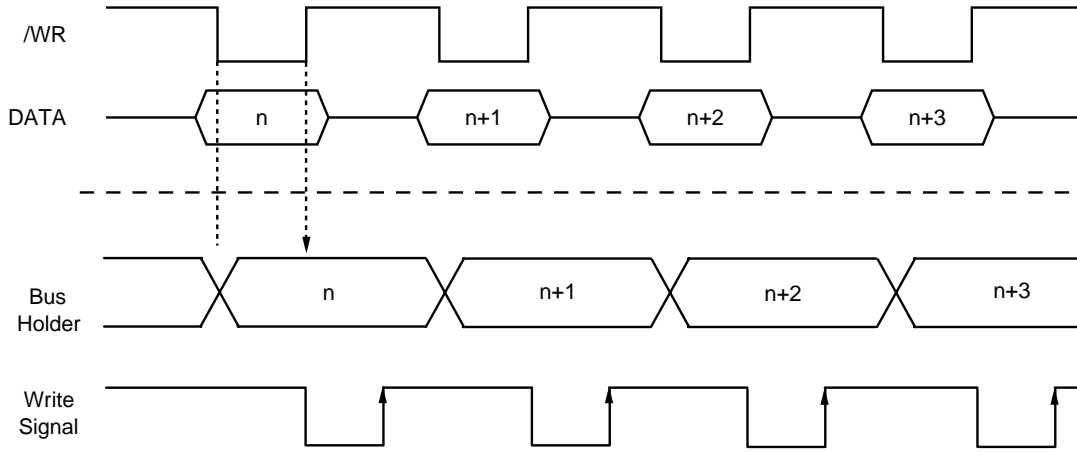
A high-speed RAM write function, as well as the ordinary RAM write function, is provided for writing data to the display data RAM. By using the high-speed write function, data can be written to the display RAM at an access speed two times faster than that of the ordinary RAM write function. Therefore, applications, such as motion picture display where the display data must be rewritten at high speeds, can be supported. For details, refer to **5.2.5 High-speed RAM write mode**

Dummy data is not required when writing data. In the μ PD161623, only for reading display data, needs dummy data. This relationship is shown in Figure 5-7.

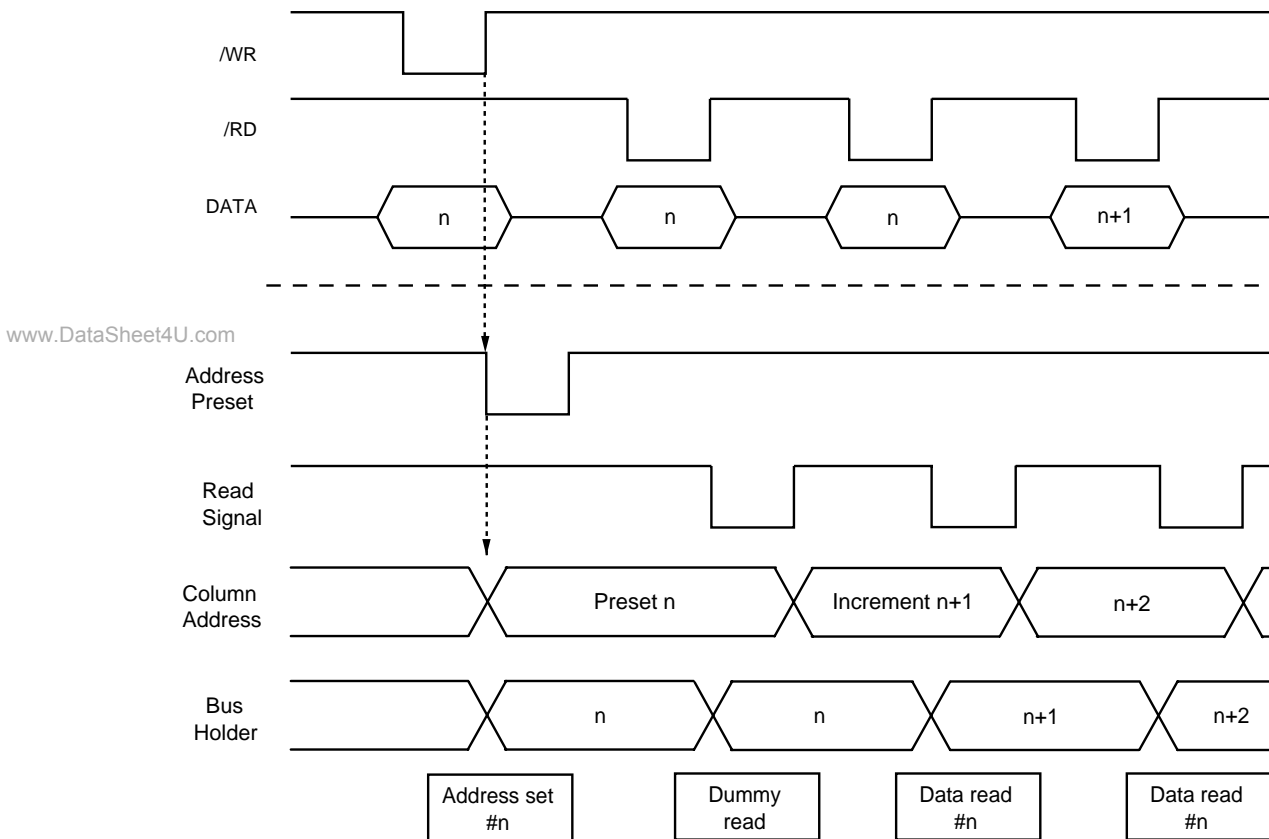
Note that when in write mode of data at high speed for data read mode of read cycle time, this mode equals to normal mode.

Figure 5-7. Image of internal access to display RAM

Writing



Reading



5.2 Display Data RAM

This RAM stores dot data for display and consists of 3,168 bits (176 x 18) x 240 bits. Any address of this RAM can be accessed by specifying an X address and an Y address.

Display data D₀ to D₁₇ transmitted from the CPU corresponds to the pixels on the LCD (refer to Table 5–8).

Figure 5–8. Display Data RAM

| | | | | | | | | | | | | | | | | | |
|-------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| D ₁₇ | D ₁₆ | D ₁₅ | D ₁₄ | D ₁₃ | D ₁₂ | D ₁₁ | D ₁₀ | D ₉ | D ₈ | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
| Dot 1 | | | | | | Dot 2 | | | | | | Dot 3 | | | | | |
| Pixel 1 (= 1 X address) | | | | | | | | | | | | | | | | | |

| | | | | | | | | | |
|-----------|---------|---------|---------|---------|---------|---------|---------|---------|--|
| LCD panel | Pixel 1 | Pixel 2 | Pixel 3 | Pixel 4 | Pixel 5 | Pixel 6 | Pixel 7 | Pixel 8 | |
| | Pixel 1 | Pixel 2 | Pixel 3 | Pixel 4 | Pixel 5 | Pixel 6 | Pixel 7 | Pixel 8 | |
| | 00H | 01H | 02H | 03H | 04H | 05H | 06H | 07H | |

5.2.1 X address circuit

An X address of the display data RAM is specified by using the X address register (R6) as shown in Figure 5–9. The specified X address is incremented by one each time display data is written or read.

In the increment mode, the X address is incremented up to AFH. If more display data is written or read, the Y address is incremented, and the X address returns to 00H.

5.2.2 Y address circuit

A Y address of the display data RAM is specified by using the Y address register (R7) as shown in Figure 5–9.

The Y address is incremented each by one when one each time display is written or read and X address is incremented to last address.

When the Y address has been incremented up to EFH and the X address up to the final address, if further display data is read or written, the X and Y addresses return to 00H.

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5.2.3 Column address circuit

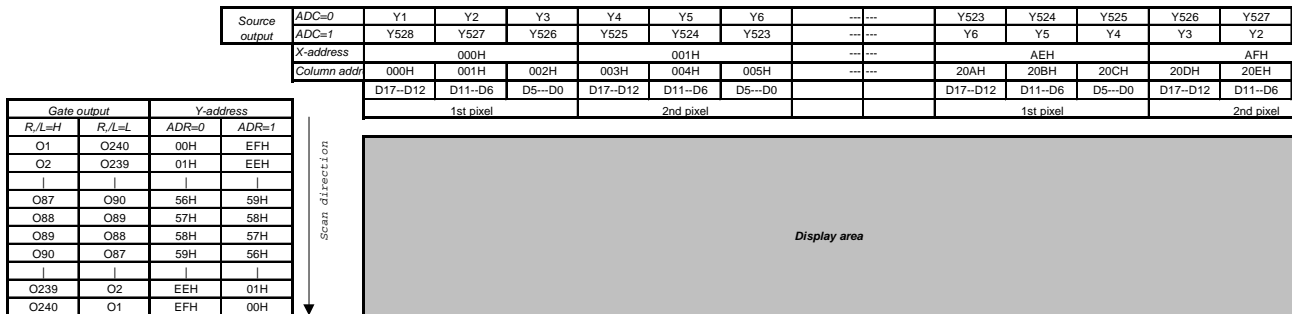
When the contents of the display data RAM are displayed, column addresses are output to the source output pins as shown in Figure 5–9.

The correspondence relationship between the column addresses of the display RAM and source outputs can be reversed by the ADC flag (source driver direction select flag) of control register 1 (R0) as shown in Table 5–6. This reduces the restrictions on chip layout when the LCD module is assembled.

Table 5–6. Relationship between Column Address of Display RAM and Source Output

| | | | | | | | |
|---------------|---|----------------|----------------|---|----------------|------------------|------------------|
| Source Output | | Y ₁ | Y ₂ | → | | Y ₅₂₇ | Y ₅₂₈ |
| ADC | 0 | 000H | 001H | → | Column address | → | 20EH 20FH |
| | 1 | 20FH | 20EH | ← | Column address | ← | 001H 000H |

Figure 5–9. μ PD161623 RAM Addressing



5.2.4 Arbitrary address area access (window access mode (WAS))

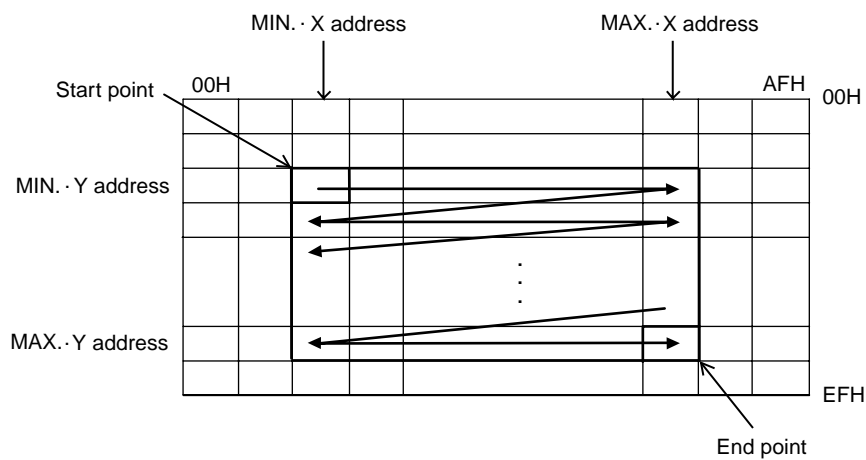
With the μPD161623, any area of the display RAM selected by the MIN.·X/Y address registers (R8 and R10) and MAX.·X/Y address registers (R9 and R11) can be accessed.

- ★ When WAS of data access control register (R5) is set to 1, the window access mode is then selected and accessed by setting only address area of the MIN.·X/Y address registers and MAX.·X/Y address registers.

The address scanning setting is also valid in this mode, in the same manner as when data is normally written to the display RAM. In addition, data can be written from any address by specifying the X address register (R6) and Y address register (R7).

Note that the display RAM must be accessed after setting the X address register (R6) and Y address register (R7) if the window access area has been set or changed by the MIN.·X/Y address register or MAX.·X/Y address register.

Figure 5–10. Example of Incrementing Address when in Window Access Mode



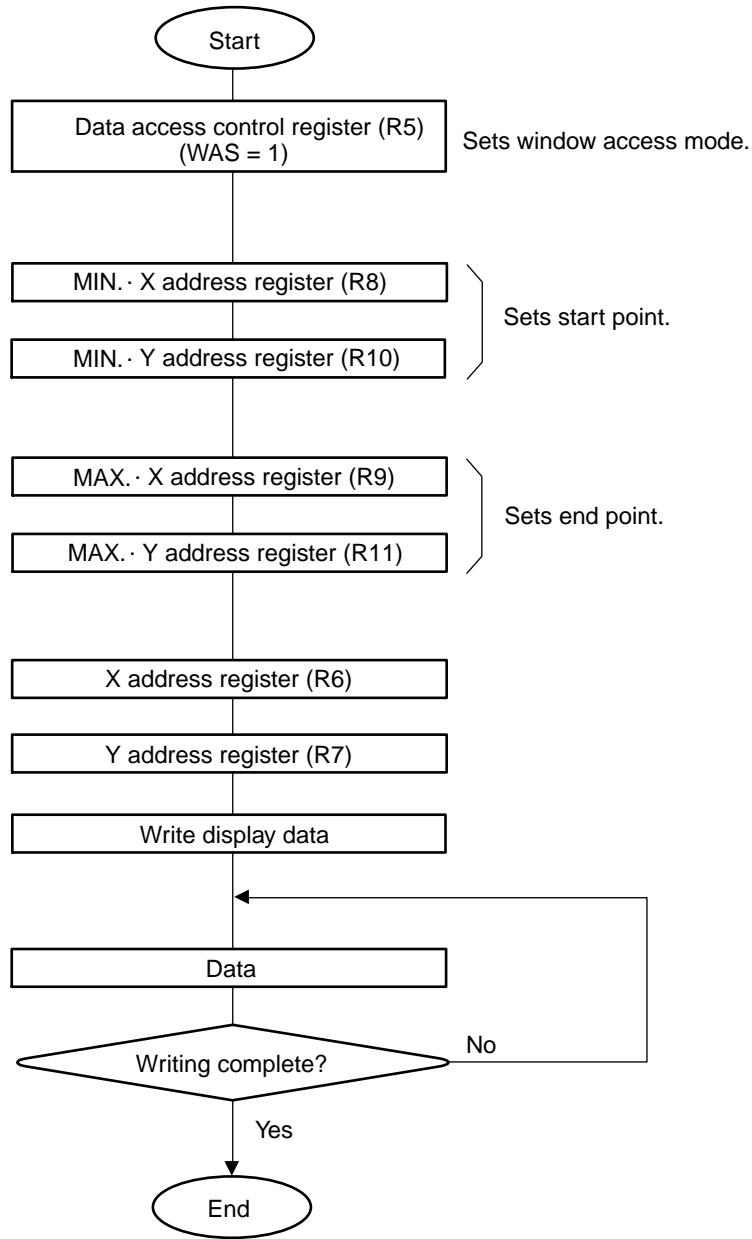
Cautions 1. When using the window access mode, the relationship between the start point and end point shown in the table below must be established.

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| Item | Address Relationship |
|-----------|--|
| X address | $00H \leq \text{MIN.·X address} \leq \text{X address (R6)} \leq \text{MAX.·X address} \leq \text{AFH}$ |
| Y address | $00H \leq \text{MIN.·Y address} \leq \text{Y address (R7)} \leq \text{MAX.·Y address} \leq \text{EFH}$ |

- 2. If invalid address data is set as the MIN./MAX.· address, operation is not guaranteed.
- ★ 3. Do not specify any value other than the address value $2n-2$ ($n = 1$ to 88) for the X address in the high-speed RAM access mode. The operation is not guaranteed if invalid address data is set.
- 4. Access the display RAM after setting the X address register (R6) and Y address register (R7) if the window access area has been set or changed by the MIN.·X/Y address register or MAX.·X/Y address register.

Figure 5-11. Example of Sequence in Window Access Mode



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5.2.5 High-speed RAM write mode

With the μPD161623, two types of access modes can be selected for accessing the display RAM.

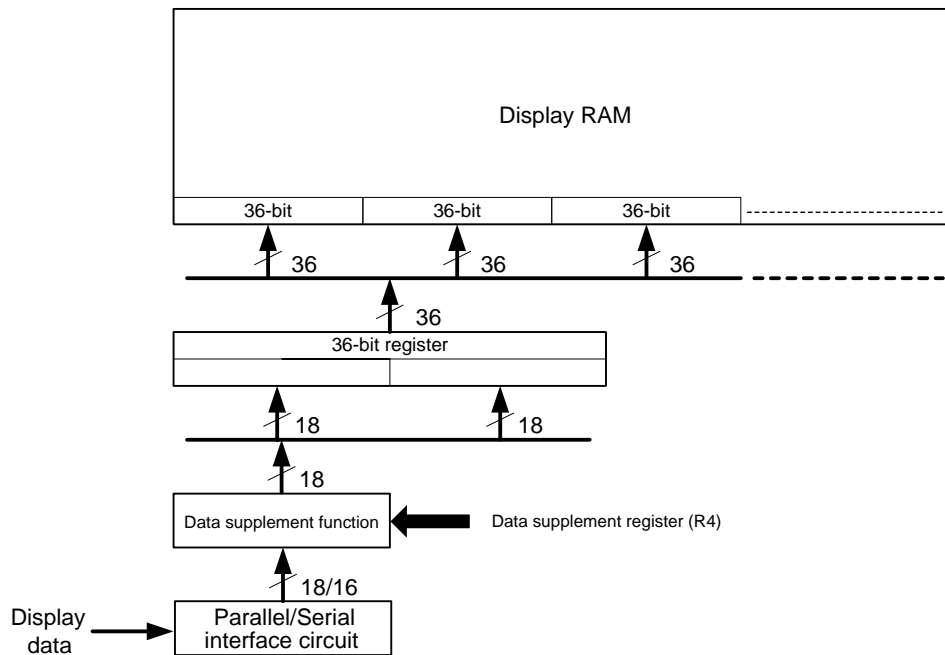
The μPD161623 has a high-speed RAM write function, as well as an ordinary RAM write function. By using the high-speed write function, data can be written to the display RAM at an access speed two times faster than that of the ordinary RAM write function. Therefore, applications, such as motion picture display where the display data must be rewritten at high speeds, can be supported.

When the high-speed RAM write mode is selected by using BSTR of the data access control register (R5), data is temporarily stored in an internal register of the μPD161623. When data of 36 bits (18 bits x 2) has been stored in the register, it is written to the display RAM. It is also possible to write the next data to the internal register while the first data is being written to the RAM.

In the high-speed RAM write mode, however, the CPU must transmit data in units of 2 pixel data (1-pixel/18-bit mode: 36-bit, 1-pixel/16-bit mode: 32-bit) have been written to the internal register. If data of less than 2-pixel data is transmitted in the high-speed RAM write mode, this data is not written to the display RAM. Therefore, CPU data is not reflected on the LCD display even if it is transmitted. In this case, the data that is not reflected remains stored in the register. When the next data is transmitted, it is written to the register from where the preceding data is stored. However, if the chip select signal is asserted inactive (/CS = H) in the middle of data transfer, and then asserted active again and when the display data write is set, the register is initialized. Consequently, the data stored in the register is lost.

It is therefore recommended to transmit display data in 2-pixel units when using the high-speed RAM write mode.

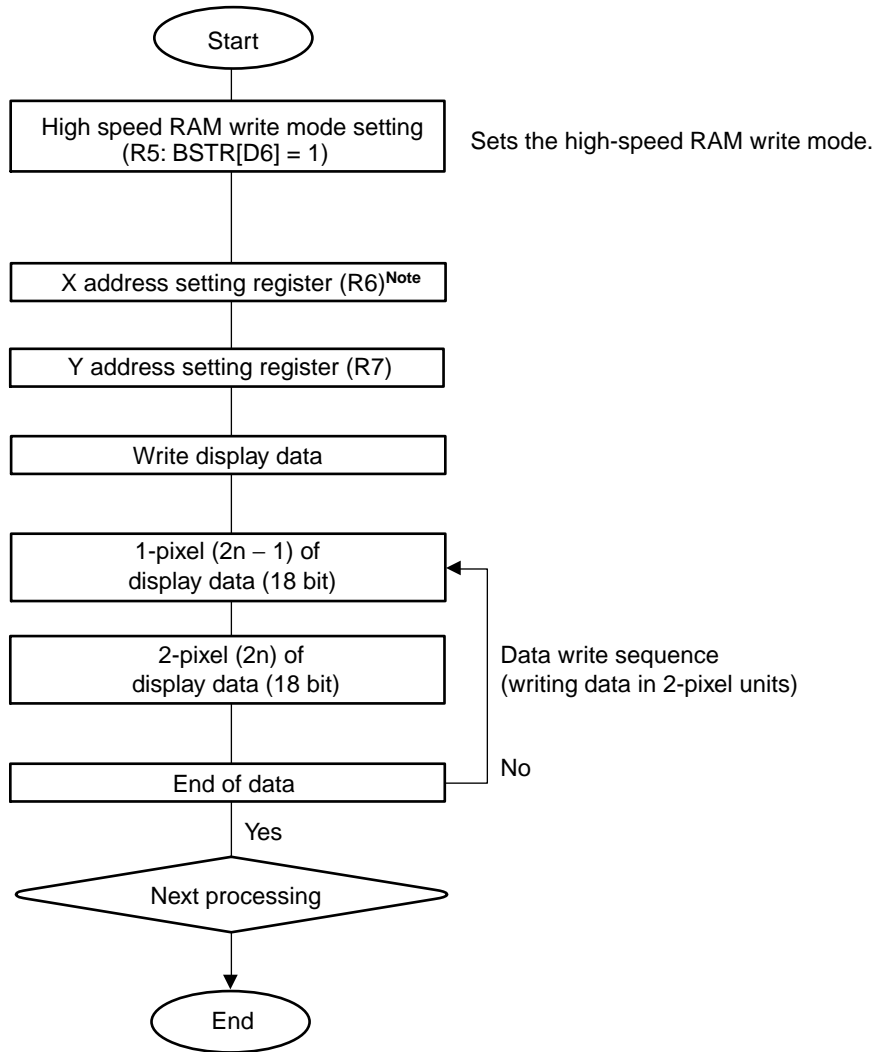
Figure 5-12. Image of Operation in High-speed Write Mode



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Caution Do not specify any value other than the address value $2n - 2$ ($n = 1$ to 88) for the X address (R6) in the high-speed RAM access mode. The operation is not guaranteed if invalid address data is set.

Figure 5–13. Example of Sequence in High-Speed RAM Write Mode (with 18-Bit Parallel Interface)



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n: n ≥ 1

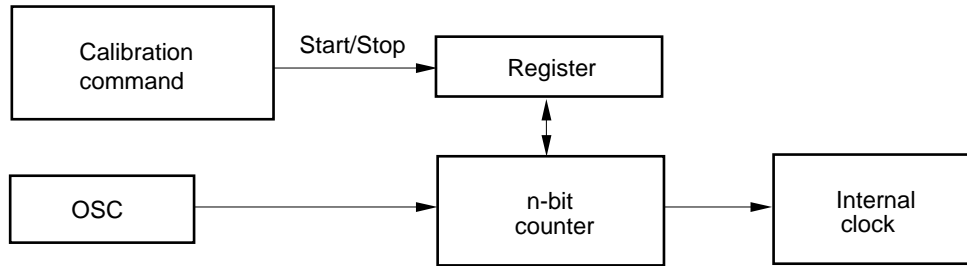
Note Do not specify any value other than the address value 2n - 2 (n = 1 to 88) for the X address (R6) in the high-speed RAM access mode. The operation is not guaranteed if invalid address data is set.

5.3 Oscillator

The μ PD161623 has a CR oscillator (with external R resistance), which generate the display clock. When OSCSEL is L, an internal CR oscillator is selected. On the other hand, leave both OSCIN and OSCOUT pin open. When OSCSEL is H, an external connection oscillator is selected. Connect 42 k Ω resistance between OSCIN an OSCOUT pin (when in used 240 lines).

This oscillator also has a calibration function, which is available by itself to set the number of frame frequency of display driving. Frame frequency calibration is set by calibration register (R45). The time to select one line is set by the calibration start and stop commands.

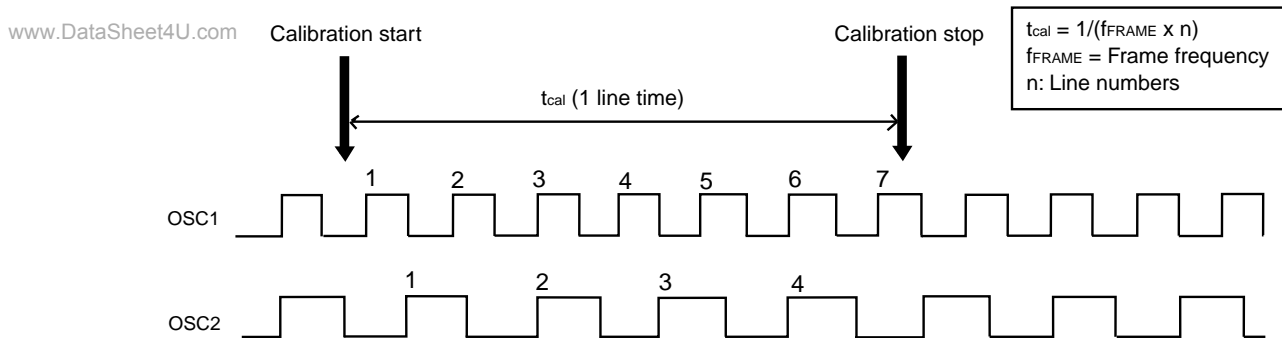
Figure 5–14. Frame Frequency Calibration



The calibration function involves counting the number of oscillation clocks generated between the start and stop signals and storing that number in a register. The number of oscillation clocks is then continually compared with this register value in subsequent operations, and the time of the clock number stored in the register is set as 1 line selection time, and used as the internal reference clock.

Using the time to set calibration (t_{cal}) can be selected either t_{cal} or $t_{cal} \times 2$ through control register 2 (R1): LTS.

Figure 5–15. Calibration Function Timing (LTS [R1] = 0)



5.4 Display Timing Generator

5.4.1 Display timing

The μ PD161623 generates the TFT-:CD drive timing inside the μ PD161623. The TFT-LCD panel is driven at the timing of one line selection period generated based on the calibration time (t_{cal}) set by the calibration function, as shown in the figure below. One line selection period is made up of a pre-charge period, a source output period, and the μ PD161623 output control clock. The pre-charge and source output periods are set by the pre-charge period setting register (R46) and calibration register (R45), respectively, based on the following expressions.

$$1 \text{ line selection period} = t_{cal}$$

$$\text{Pre-charge period} = t_{pr}$$

$$\text{Source output period} = t_{sout}$$

t_{cal} : Calibration setting time [R45]

$$t_{pr} = (1/f_{osc}) \times (\text{CLK}_{pr} + 2 \text{ CLK})$$

$$t_{sout} = t_{cal} - (t_{pr} + 3 \text{ CLK})$$

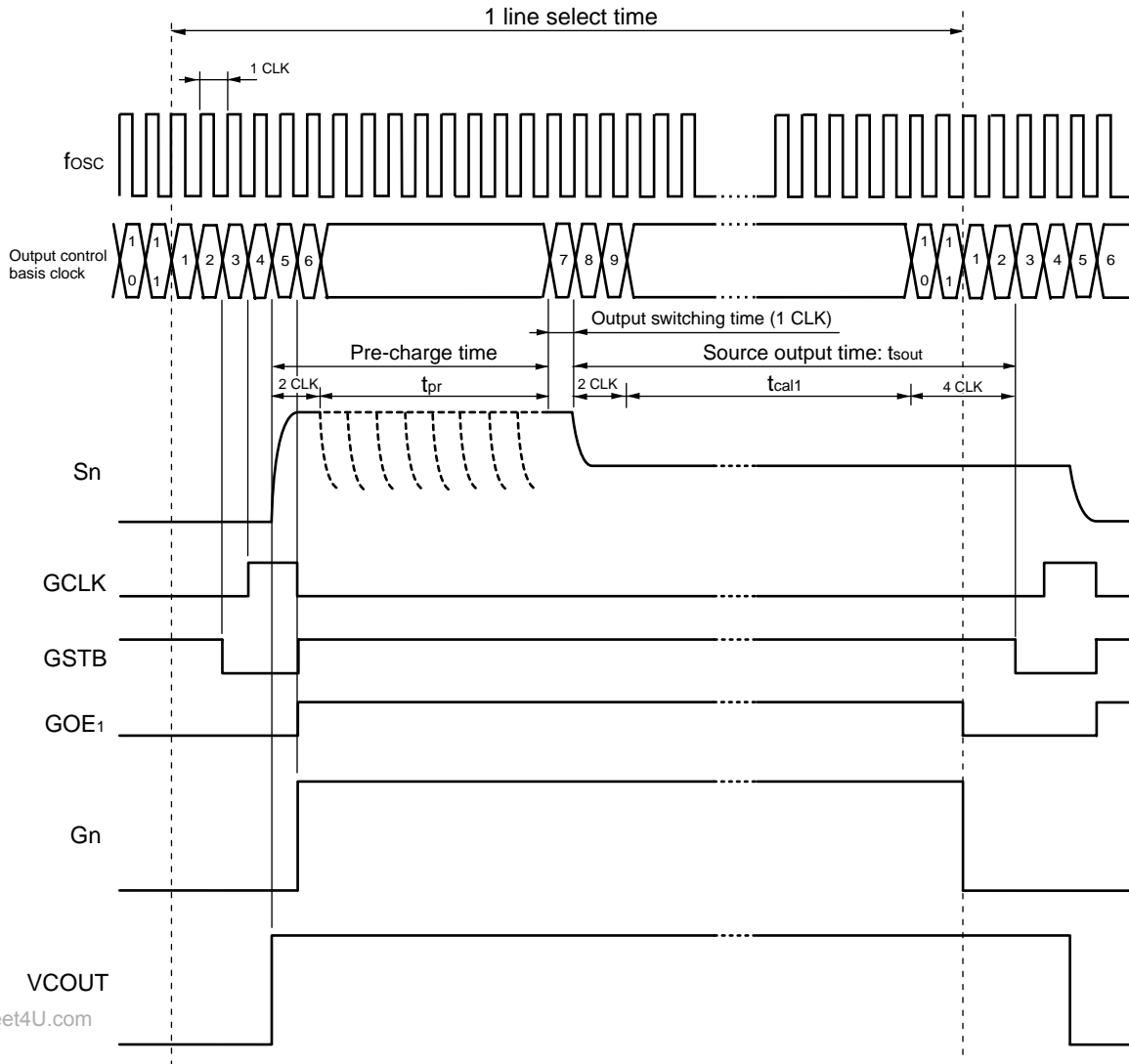
CLK_{cal} : Calibration setting time (t_{cal}) clock number = $t_{cal} \div (1/f_{osc})$

CLK_{pr} : Pre-charge period setting register clock number [R46: PLIMn] n

$$1 \text{ CLK} = 1/f_{osc}$$

f_{osc} : Oscillator frequency

Figure 5-16. 1-line Select Time



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The display timing generator generates the timing signals for the internal timing of the source driver and for the gate driver. The output timings for normal operation, for normal operation → stand-by mode, and for stand-by mode → normal operation, are shown below.

Figure 5-17. During Normal Operation (during line inversion)

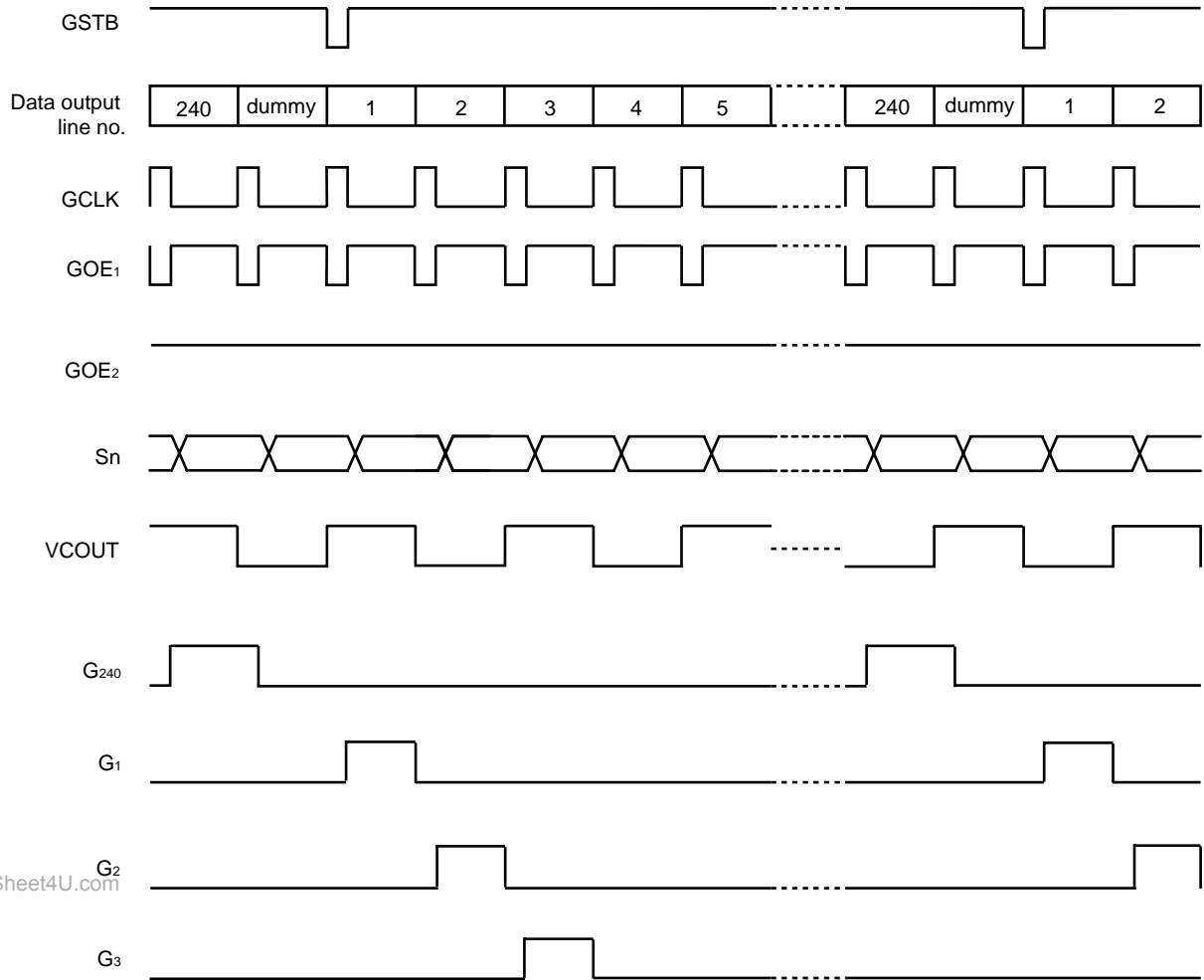
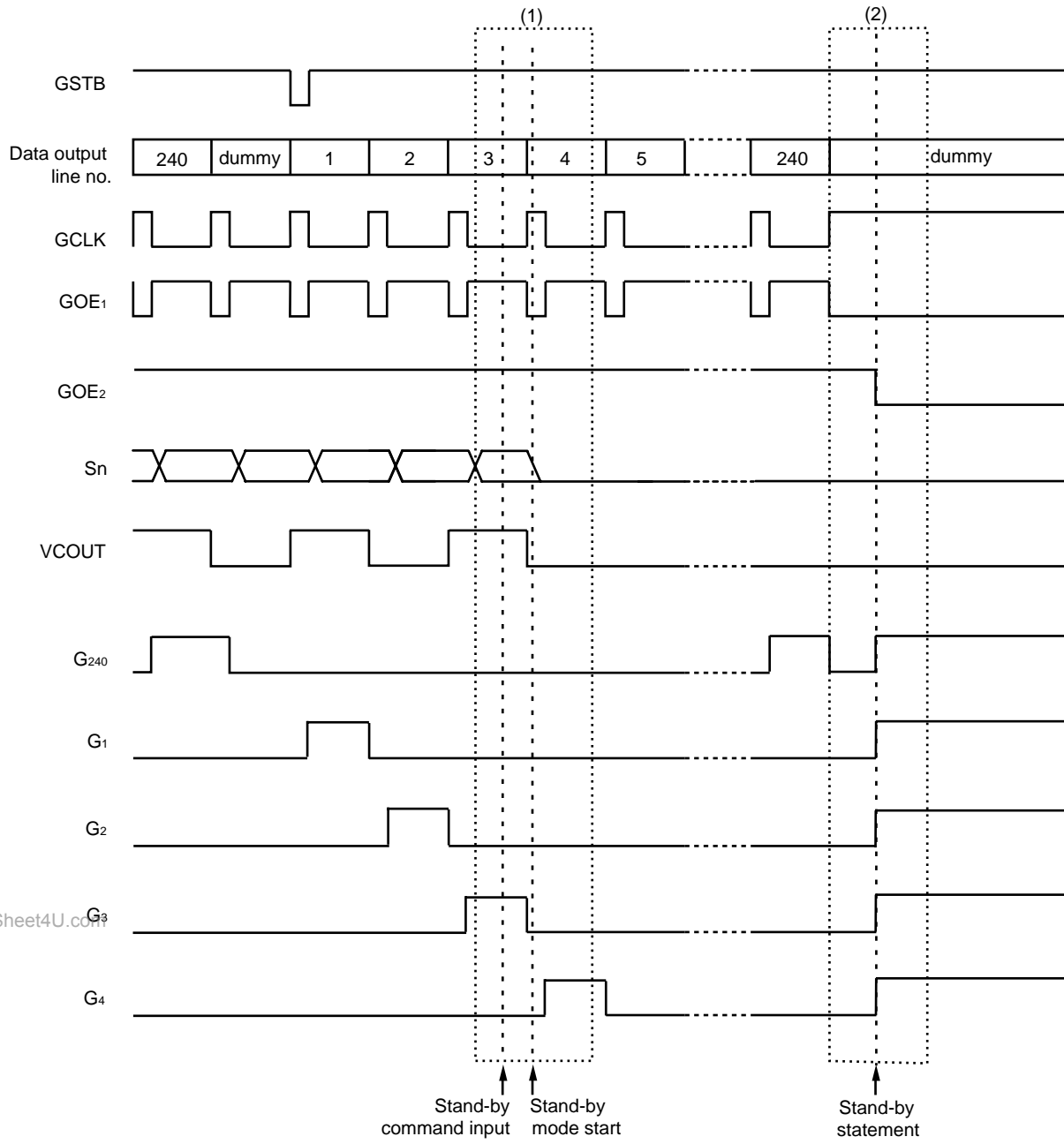


Figure 5-18. Normal Operation → Stand-by Input (during line inversion)



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Figure 5-19. Normal Operation → Stand-by Input (during line inversion) (1) Reference

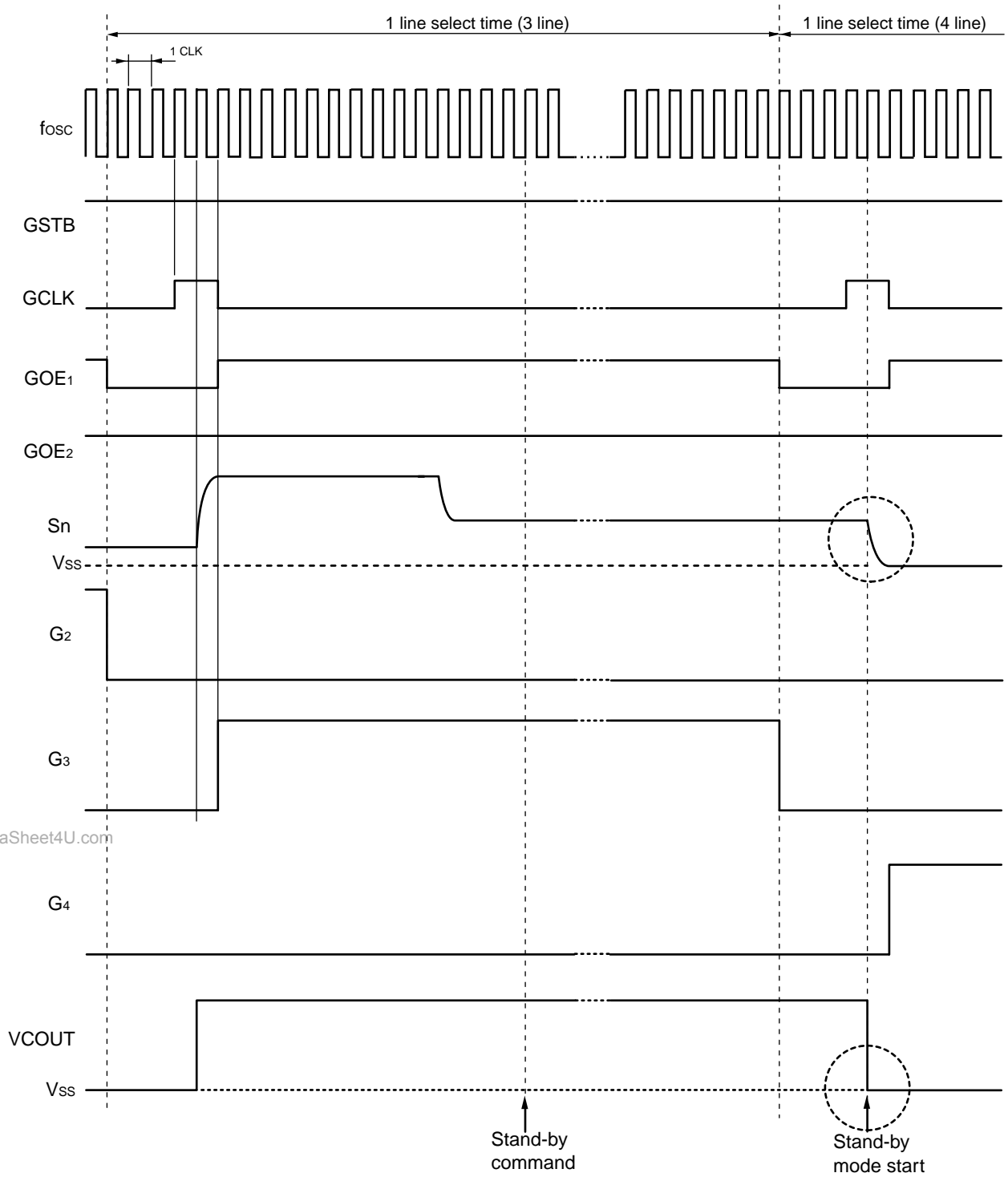
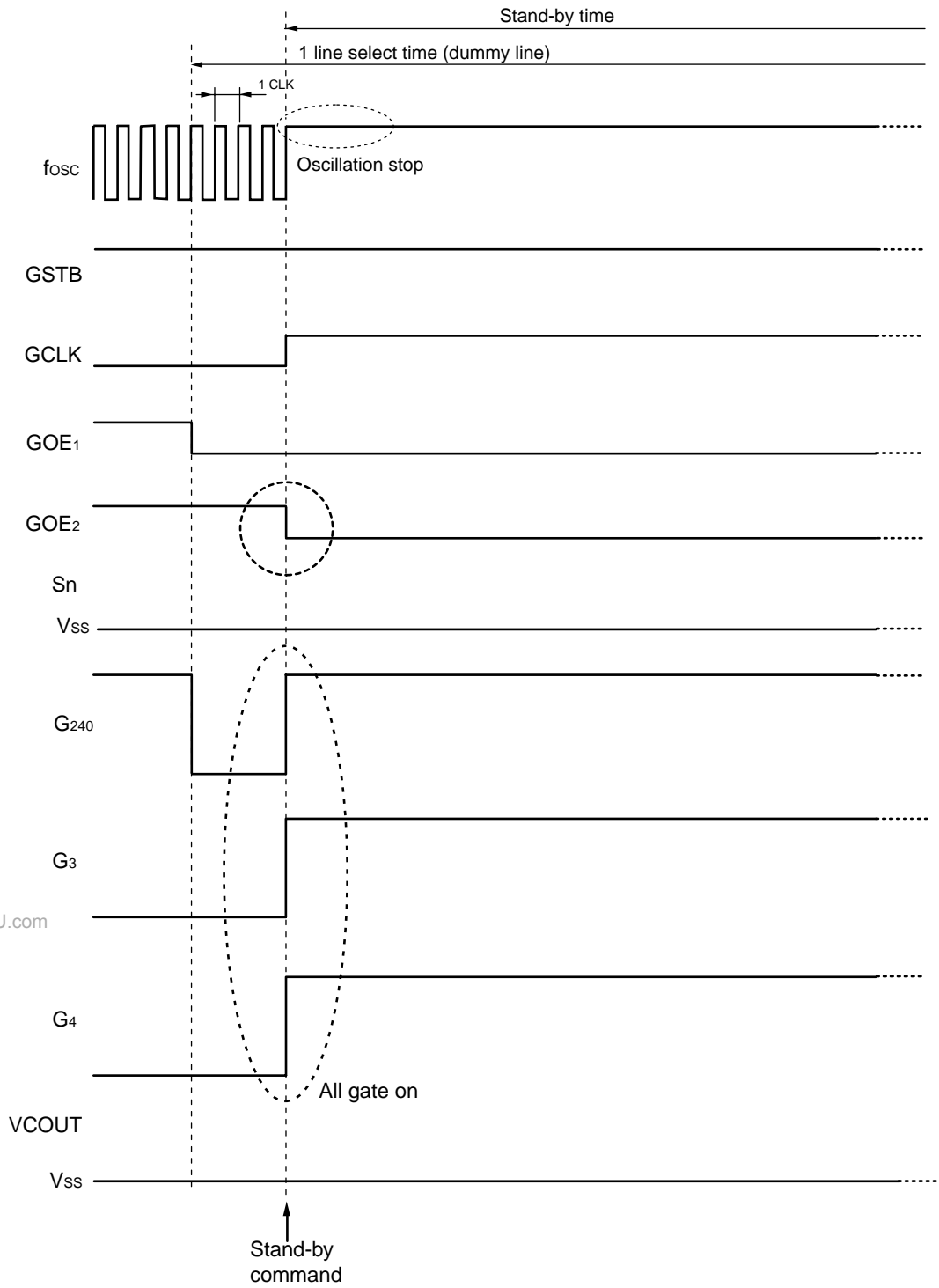
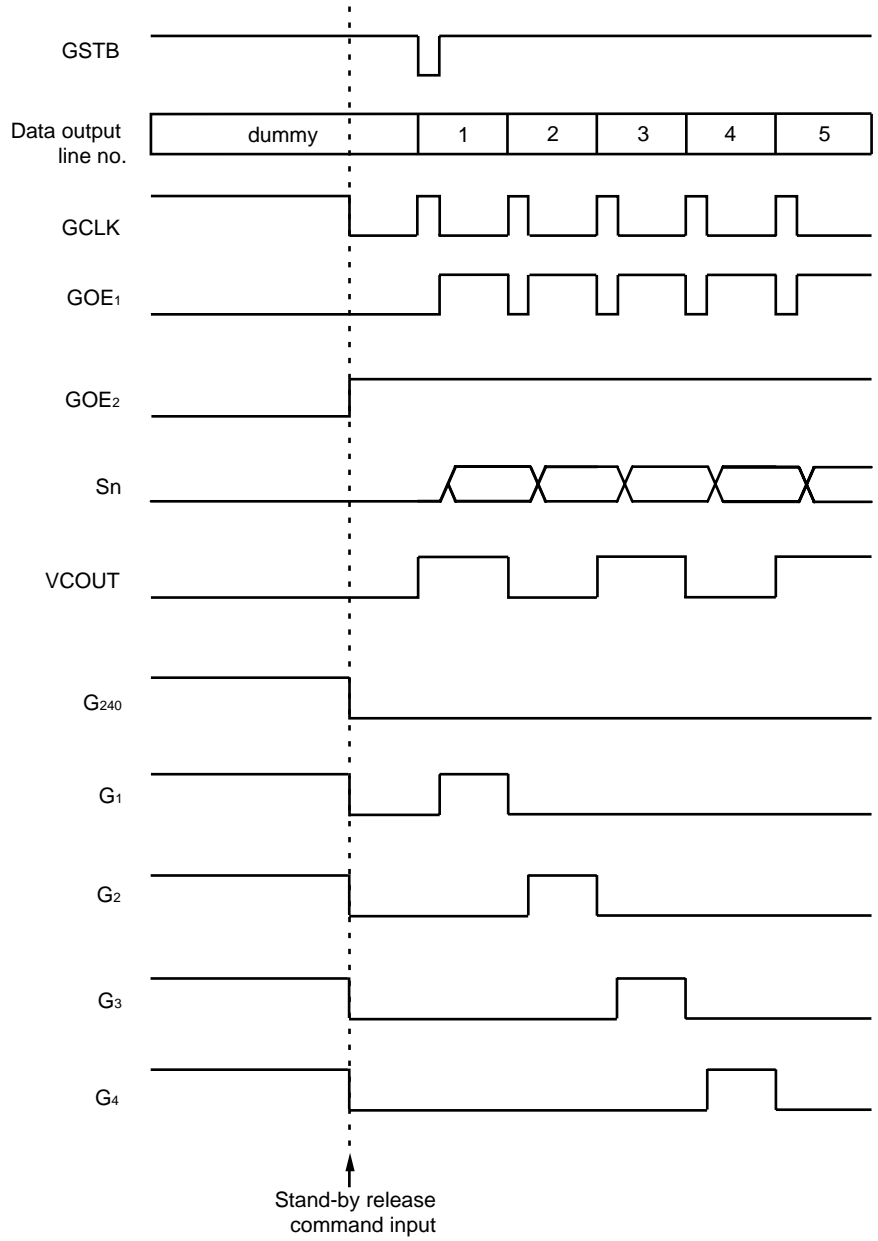


Figure 5-20. Normal Operation → Stand-by Input (during line inversion) (2) Reference



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Figure 5-21. Stand-by → Return to Normal Operation (during line inversion)



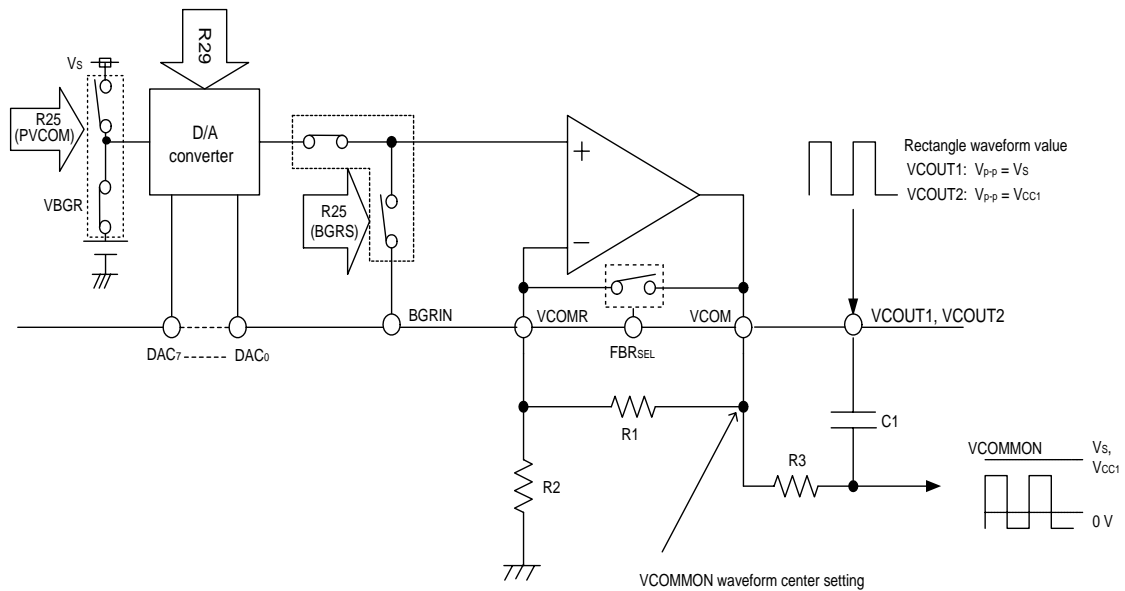
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5.5 Common Adjustment Circuit

To generate common output, the center voltage of the common waveform is output from the VCOM pin along with output of a 0 to V_s (V) square waveform from the VCOUT1 pin and 0 to V_{DD1} (V) from VCOUT2. The level of the VCOM output can be adjusted using as external resistor.

★

Figure 5–22. Common Adjustment Circuit



The VCOM voltage formulas are shown below.

★

<When internal power supply is used 1 (D₆ of R25: BGRS = 0, D₃ of PVCOM = 0) >

$$\text{COM voltage} = (1+R1/R2) \times \text{VBGR} \times (\alpha \div 256)$$

$$\text{VBGR} = 3.0 \text{ V TYP.}$$

α : Setting of VCOM electric volume register (R29)

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★

<When internal power supply is used 2 (D₆ of R25: BGRS = 0, D₃ of PVCOM = 1) >

$$\text{COM voltage} = (1+R1/R2) \times V_s \times (\alpha \div 256)$$

α : Setting of VCOM electric volume register (R29)

★

<When external power supply is used (D₆ of R25: BGRS = 1)>

$$\text{COM voltage} = (1+R1/R2) \times \text{VBGRIN}$$

VBGRIN = External supply voltage (voltage input from BGRIN)

★

<Recommended values for R1 to R3, and C1>

Use the values listed below as a guideline. The user is responsible for ultimately determining the resistance values and recommended values based on careful evaluation on actual panels.

R1: 200 k Ω

R2: 51 to 100 k Ω

R3: 51 to 100 k Ω

C1: 10 μ F

5.6 Rectangular Signal Generator

This circuit generates a common rectangular signal. A rectangular wave of 0 to V_s (V) is output from the VCOUT1 pin, and a wave of 0 to V_{DD2} (V) is output from the VCOUT2 pin. The common output wave necessary for driving an LCD can be generated by connecting an external circuit as shown in Figure 5–22.

5.7 Reference Voltage Generator (VBGR)

The μ PD161623 has a reference voltage generator for the voltage regulator. This reference voltage generator generates a constant voltage from V_{DD2} . The constant voltage generated by this circuit is connected to the input of the operational amplifier that adjusts the center level of the COMMON drive output, via a D/A converter.

By using this voltage, therefore, the center level of the COMMON drive output can be kept constant, without being affected by fluctuations in the supply voltage.

The common waveform output necessary for driving an LCD can be generated by connecting the external circuit show in Figure 5–16.

When the internal reference voltage generator is not used (R25: BGRS = 1), directly input the reference voltage to the operational amplifier that adjusts the center level of the COMMON drive output.

5.8 D/A Converter Circuit

The μ PD161623 is provided with an internal D/A converter to adjust the voltage of the reference voltage generator for the voltage regulator. This D/A converter divides the constant voltage generated by the reference voltage generator (VBFR) by 256, and a level of voltage between VBGR and V_{SS} can be selected by setting the VCOM electronic volume register (R29).

In addition, this D/A converter also has a function to select a level by using an external pin. If the set value of the VCOM electronic volume register (R29) is 00H, the set statuses of the DAC₇ to DAC₀ pins are valid.

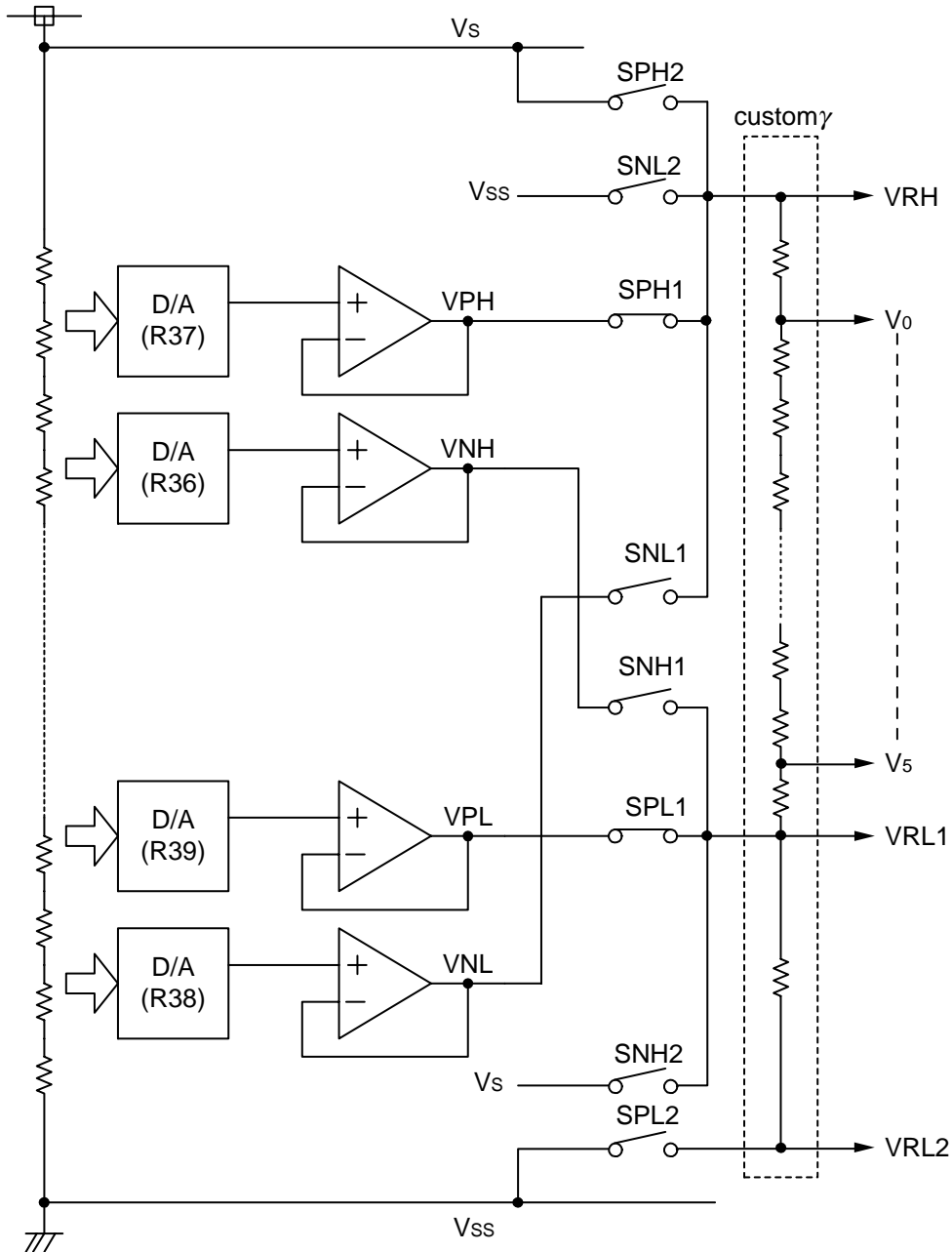
Table 5–7. α Setting of VCOM Electronic Volume Register (R25: BGRS = 0)

| | EV ₇ | EV ₆ | EV ₅ | EV ₄ | EV ₃ | EV ₂ | EV ₁ | EV ₀ | α | Remark |
|-----|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|----------------------------|------------------|
| | DAC ₇ | DAC ₆ | DAC ₅ | DAC ₄ | DAC ₃ | DAC ₂ | DAC ₁ | DAC ₀ | | |
| 00H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DAC _n set value | R29 |
| | | | | | | | | | 0 | DAC _n |
| 01H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 | |
| 02H | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 3 | |
| 03H | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 4 | |
| ⋮ | | | | ⋮ | | | | | ⋮ | |
| FEH | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 255 | |
| FFH | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 256 | |

5.9 γ -Curve Correction Power Supply Circuit

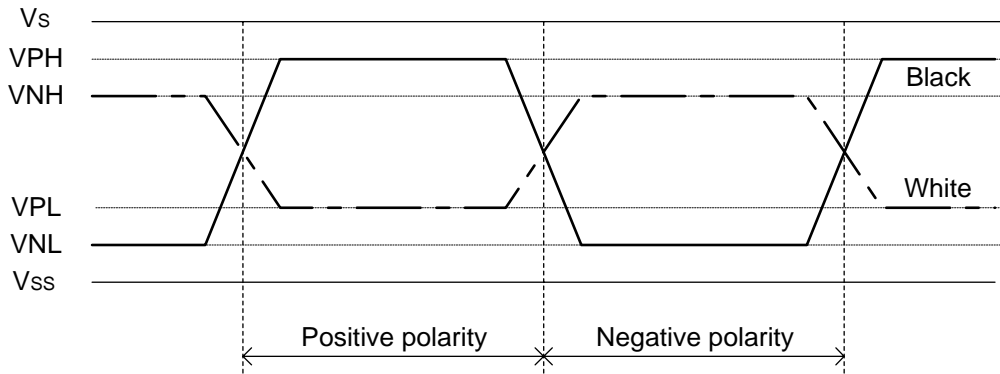
The μ PD161623 includes a γ -curve correction power supply circuit. If the internal γ -curve correction matches the LCD characteristics, no external components are necessary. This power circuit has white level and black level reference voltage generators on the positive and negative polarity sides, and also supports unbalanced driving. The reference voltage generators consist of a D/A converter and an operational amplifier and divide V_s to V_{ss} by 256. One level of voltage can be selected by using the γ -contrast value setting register 1 to 4 (R36 to R39)

Figure 5-23. γ -Curve Correction Circuit



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Figure 5–24. Relationship of TFT Drive Voltage (Normally White)



| | Drive Level | Setting Register | |
|-----|--------------------------|-----------------------------------|-----|
| VPH | Positive polarity, black | Contrast value setting register 1 | R36 |
| VNH | Negative polarity, white | Contrast value setting register 2 | R37 |
| VPL | Positive polarity, black | Contrast value setting register 3 | R38 |
| VNL | Negative polarity, white | Contrast value setting register 4 | R39 |

The value of each amplifier output can be expressed as follows and the value of β can be set as shown in Table 5–8 and 5–9 by using the contrast value registers (R36, R37, R38, and R39)

$$VNL, VPL, VNH, VPH = (\beta \div 256) \times V_s$$

Caution The usable range in which each output level of VPH, VNH, VPL, and VNL can be set depends on the γ -curve.

Table 5–8. γ -Contrast Value Setting and Electronic Volume Register β Setting 1 (VPH, VNL)

| R36 | GPH7 | GPH6 | GPH5 | GPH4 | GPH3 | GPH2 | GPH1 | GPH0 | β value Setting or Status Setting |
|-----|------|------|------|------|------|------|------|------|---|
| R37 | GNH7 | GNH6 | GNH5 | GNH4 | GNH3 | GNH2 | GNH1 | GNH0 | |
| 00H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Fixed to V_s (Amplifier OFF) |
| 01H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 255 |
| 02H | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 254 |
| 03H | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 253 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| FEH | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 2 |
| FFH | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Table 5-9. γ Contrast Value Setting and Electronic Volume Register β Setting 2 (VPL, VNL)

| R36 | GPL7 | GPL6 | GPL5 | GPL4 | GPL3 | GPL2 | GPL1 | GPL0 | β value Setting or Statement Setting |
|-----|------|------|------|------|------|------|------|------|--|
| R37 | GNL7 | GNL6 | GNL5 | GNL4 | GNL3 | GNL2 | GNL1 | GNL0 | |
| 00H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Fixed to V_s (Amplifier OFF) |
| 01H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 02H | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 03H | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| ⋮ | | | | ⋮ | | | | | ⋮ |
| FEH | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 254 |
| FFH | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 255 |

The relationship between the setting of the contrast value setting register and the driven waveform is explained next, taking the γ -curve in Figure 5-23 as an example.

Table 5-10. Switch Status when γ -Curve Correction Power Supply Circuit is not used (R36, R37, R38, R39 = 00H)

| Polarity | Switch Status | | | | | | | |
|----------|---------------|------|------|------|------|------|------|------|
| | SPH1 | SNL1 | SNH1 | SPL1 | SPH2 | SNL2 | SNH2 | SPL2 |
| Positive | X | X | X | X | ON | OFF | OFF | ON |
| Negative | X | X | X | X | OFF | ON | ON | OFF |

Remark X: Switch is normally OFF with the amplifier OFF.

Relationship of drive voltage (normally white)

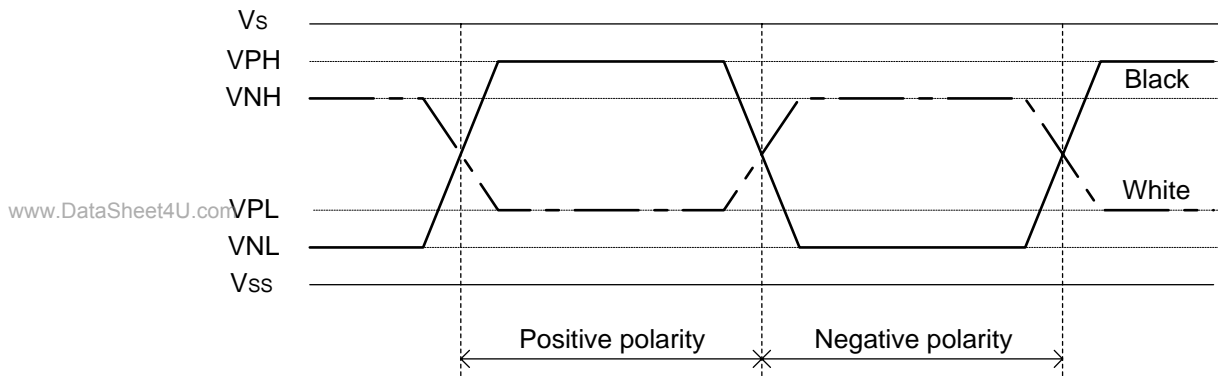


Table 5-11. Switch Status when γ -Curve Correction Power Circuit is used (R36, R37, R38, R39 = other than 00H)

| Polarity | Switch Status | | | | | | | |
|----------|---------------|------|------|------|------|------|------|------|
| | SPH1 | SNL1 | SNH1 | SPL1 | SPH2 | SNL2 | SNH2 | SPL2 |
| Positive | ON | OFF | OFF | ON | x | x | x | x |
| Negative | OFF | ON | ON | OFF | x | x | x | x |

Remark x: Switch is normally OFF

Relationship of drive voltage (normally white)

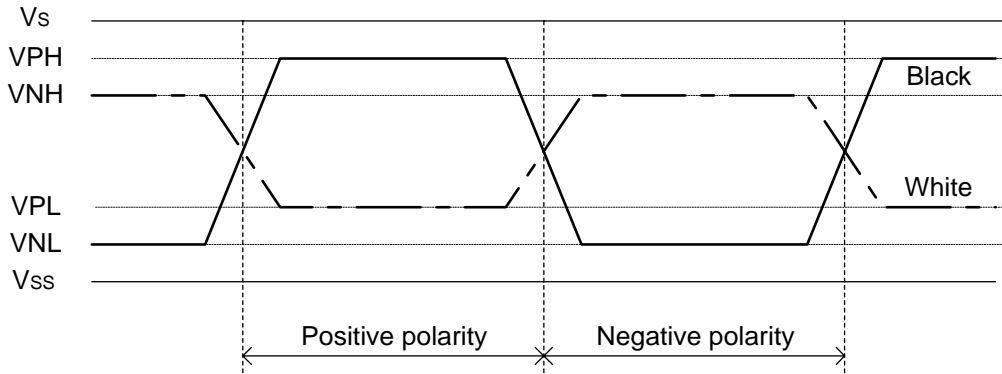
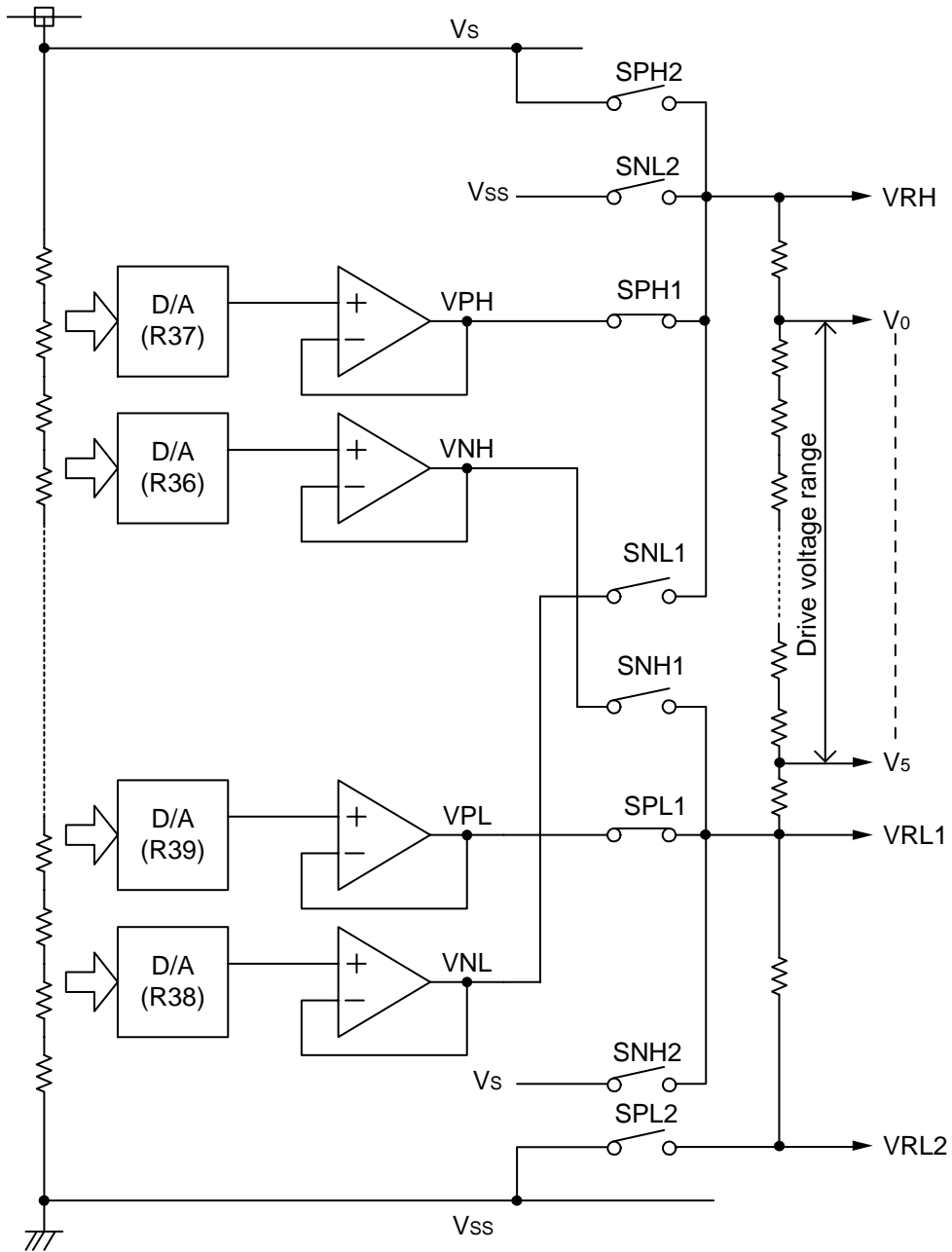


Figure 5-25. TFT Drive Voltage Level



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Table 5-12. γ -Curve Correction Circuit (γ -Correction Resistance)

| Glax Scale | Display Data | | | | | | Resistance (k Ω) | | Output Voltage (V) | |
|------------|--------------|------|------|------|------|----|--------------------------|--------|--------------------|------------------|
| | Dn+5 | Dn+4 | Dn+3 | Dn+2 | Dn+1 | Dn | r 1 | 1.587 | Positive Voltage | Negative Voltage |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | r 2 | 1.226 | 4.901 | 0.107 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | r 3 | 2.453 | 4.824 | 0.190 |
| 2 | 0 | 0 | 0 | 0 | 1 | 0 | r 4 | 3.390 | 4.671 | 0.356 |
| 3 | 0 | 0 | 0 | 0 | 1 | 1 | r 5 | 4.112 | 4.459 | 0.586 |
| 4 | 0 | 0 | 0 | 1 | 0 | 0 | r 6 | 4.905 | 4.202 | 0.864 |
| 5 | 0 | 0 | 0 | 1 | 0 | 1 | r 7 | 1.731 | 3.895 | 1.196 |
| 6 | 0 | 0 | 0 | 1 | 1 | 0 | r 8 | 1.443 | 3.787 | 1.313 |
| 7 | 0 | 0 | 0 | 1 | 1 | 1 | r 9 | 1.587 | 3.697 | 1.411 |
| 8 | 0 | 0 | 1 | 0 | 0 | 0 | r 10 | 1.515 | 3.598 | 1.519 |
| 9 | 0 | 0 | 1 | 0 | 0 | 1 | r 11 | 1.082 | 3.503 | 1.621 |
| 10 | 0 | 0 | 1 | 0 | 1 | 0 | r 12 | 1.082 | 3.436 | 1.694 |
| 11 | 0 | 0 | 1 | 0 | 1 | 1 | r 13 | 1.154 | 3.368 | 1.768 |
| 12 | 0 | 0 | 1 | 1 | 0 | 0 | r 14 | 1.226 | 3.296 | 1.846 |
| 13 | 0 | 0 | 1 | 1 | 0 | 1 | r 15 | 1.298 | 3.219 | 1.929 |
| 14 | 0 | 0 | 1 | 1 | 1 | 0 | r 16 | 1.082 | 3.138 | 2.017 |
| 15 | 0 | 0 | 1 | 1 | 1 | 1 | r 17 | 0.649 | 3.070 | 2.090 |
| 16 | 0 | 1 | 0 | 0 | 0 | 0 | r 18 | 0.721 | 3.030 | 2.134 |
| 17 | 0 | 1 | 0 | 0 | 0 | 1 | r 19 | 0.794 | 2.985 | 2.183 |
| 18 | 0 | 1 | 0 | 0 | 1 | 0 | r 20 | 0.721 | 2.935 | 2.236 |
| 19 | 0 | 1 | 0 | 0 | 1 | 1 | r 21 | 0.794 | 2.890 | 2.285 |
| 20 | 0 | 1 | 0 | 1 | 0 | 0 | r 22 | 0.505 | 2.840 | 2.339 |
| 21 | 0 | 1 | 0 | 1 | 0 | 1 | r 23 | 0.577 | 2.809 | 2.373 |
| 22 | 0 | 1 | 0 | 1 | 1 | 0 | r 24 | 0.577 | 2.773 | 2.412 |
| 23 | 0 | 1 | 0 | 1 | 1 | 1 | r 25 | 0.577 | 2.737 | 2.451 |
| 24 | 0 | 1 | 1 | 0 | 0 | 0 | r 26 | 0.505 | 2.701 | 2.490 |
| 25 | 0 | 1 | 1 | 0 | 0 | 1 | r 27 | 0.433 | 2.669 | 2.524 |
| 26 | 0 | 1 | 1 | 0 | 1 | 0 | r 28 | 0.433 | 2.642 | 2.554 |
| 27 | 0 | 1 | 1 | 0 | 1 | 1 | r 29 | 0.433 | 2.615 | 2.583 |
| 28 | 0 | 1 | 1 | 1 | 0 | 0 | r 30 | 0.433 | 2.588 | 2.612 |
| 29 | 0 | 1 | 1 | 1 | 0 | 1 | r 31 | 0.505 | 2.561 | 2.642 |
| 30 | 0 | 1 | 1 | 1 | 1 | 0 | r 32 | 0.361 | 2.529 | 2.676 |
| 31 | 0 | 1 | 1 | 1 | 1 | 1 | r 33 | 0.433 | 2.507 | 2.700 |
| 32 | 1 | 0 | 0 | 0 | 0 | 0 | r 34 | 0.433 | 2.480 | 2.729 |
| 33 | 1 | 0 | 0 | 0 | 0 | 1 | r 35 | 0.433 | 2.453 | 2.759 |
| 34 | 1 | 0 | 0 | 0 | 1 | 0 | r 36 | 0.433 | 2.426 | 2.788 |
| 35 | 1 | 0 | 0 | 0 | 1 | 1 | r 37 | 0.433 | 2.399 | 2.817 |
| 36 | 1 | 0 | 0 | 1 | 0 | 0 | r 38 | 0.433 | 2.372 | 2.847 |
| 37 | 1 | 0 | 0 | 1 | 0 | 1 | r 39 | 0.505 | 2.344 | 2.876 |
| 38 | 1 | 0 | 0 | 1 | 1 | 0 | r 40 | 0.433 | 2.313 | 2.910 |
| 39 | 1 | 0 | 0 | 1 | 1 | 1 | r 41 | 0.433 | 2.286 | 2.939 |
| 40 | 1 | 0 | 1 | 0 | 0 | 0 | r 42 | 0.433 | 2.259 | 2.969 |
| 41 | 1 | 0 | 1 | 0 | 0 | 1 | r 43 | 0.505 | 2.232 | 2.998 |
| 42 | 1 | 0 | 1 | 0 | 1 | 0 | r 44 | 0.361 | 2.200 | 3.032 |
| 43 | 1 | 0 | 1 | 0 | 1 | 1 | r 45 | 0.433 | 2.178 | 3.057 |
| 44 | 1 | 0 | 1 | 1 | 0 | 0 | r 46 | 0.433 | 2.151 | 3.086 |
| 45 | 1 | 0 | 1 | 1 | 0 | 1 | r 47 | 0.361 | 2.124 | 3.115 |
| 46 | 1 | 0 | 1 | 1 | 1 | 0 | r 48 | 0.361 | 2.101 | 3.140 |
| 47 | 1 | 0 | 1 | 1 | 1 | 1 | r 49 | 0.361 | 2.078 | 3.164 |
| 48 | 1 | 1 | 0 | 0 | 0 | 0 | r 50 | 0.361 | 2.056 | 3.188 |
| 49 | 1 | 1 | 0 | 0 | 0 | 1 | r 51 | 0.433 | 2.033 | 3.213 |
| 50 | 1 | 1 | 0 | 0 | 1 | 0 | r 52 | 0.433 | 2.006 | 3.242 |
| 51 | 1 | 1 | 0 | 0 | 1 | 1 | r 53 | 0.433 | 1.979 | 3.271 |
| 52 | 1 | 1 | 0 | 1 | 0 | 0 | r 54 | 0.505 | 1.952 | 3.301 |
| 53 | 1 | 1 | 0 | 1 | 0 | 1 | r 55 | 0.505 | 1.921 | 3.335 |
| 54 | 1 | 1 | 0 | 1 | 1 | 0 | r 56 | 0.505 | 1.889 | 3.369 |
| 55 | 1 | 1 | 0 | 1 | 1 | 1 | r 57 | 0.721 | 1.858 | 3.403 |
| 56 | 1 | 1 | 1 | 0 | 0 | 0 | r 58 | 0.721 | 1.812 | 3.452 |
| 57 | 1 | 1 | 1 | 0 | 0 | 1 | r 59 | 0.866 | 1.767 | 3.501 |
| 58 | 1 | 1 | 1 | 0 | 1 | 0 | r 60 | 0.866 | 1.713 | 3.560 |
| 59 | 1 | 1 | 1 | 0 | 1 | 1 | r 61 | 1.587 | 1.659 | 3.618 |
| 60 | 1 | 1 | 1 | 1 | 0 | 0 | r 62 | 2.597 | 1.560 | 3.726 |
| 61 | 1 | 1 | 1 | 1 | 0 | 1 | r 63 | 2.597 | 1.398 | 3.901 |
| 62 | 1 | 1 | 1 | 1 | 1 | 0 | r 64 | 12.047 | 1.235 | 4.077 |
| 63 | 1 | 1 | 1 | 1 | 1 | 1 | r 65 | 7.719 | 0.482 | 4.893 |
| Total | | | | | | | | 80.000 | | |

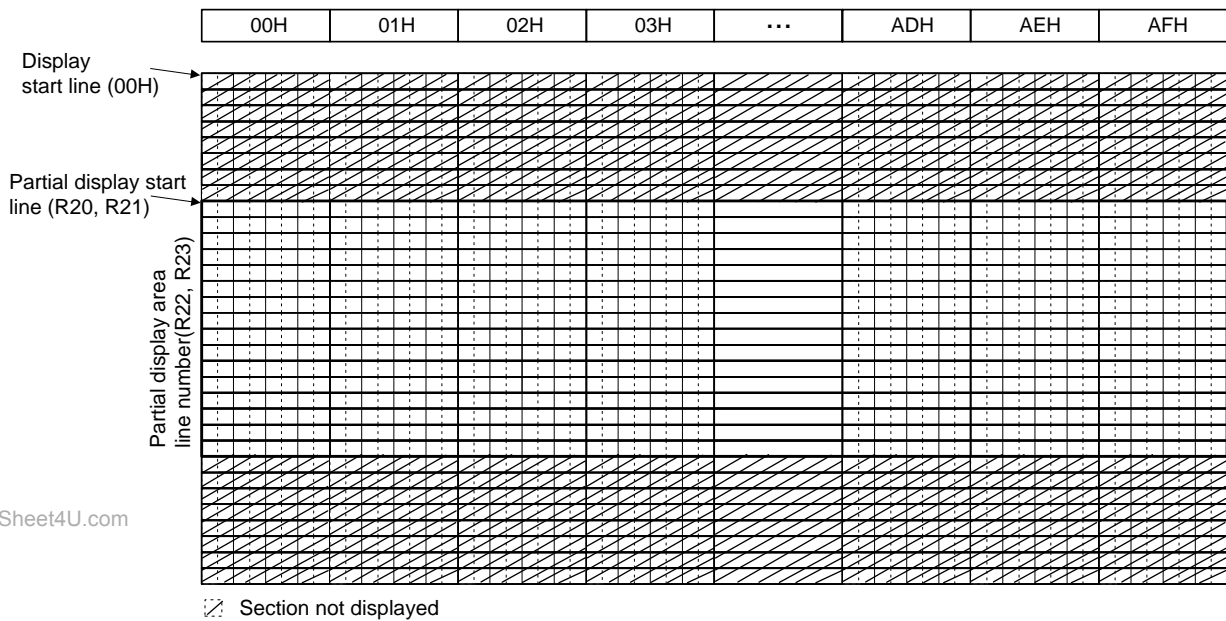
5.10 Partial Display Mode

The μ PD161623 is provided with a function that allows sections within the screen to be displayed separately (partial display mode). The start line of the area to be displayed in partial display mode is set using the partial display area start line register (R20, R21), the number of lines in the area to be displayed is set using the partial display area line count register (R22, R23), and the color of the area not to be displayed is set using the partial off area color register (R19). If "1" is set in the partial display area line count registers (R22, R23), the partial display areas each become 1 line. If "0" is set, there are no partial display areas but only normal display areas.

The non-display area indicated by R20 and R22 is called Partial 1, and the non-display area indicates by R21 and R23 is called Partial 2. The Partial 2 setting is enabled only when the Partial 1 setting has been performed (when R22 \neq 0). Therefore, to set only one area as a non-display area, perform only the setting for Partial 1.

Low power consumption cannot be achieved if only the partial mode is set. If low power consumption is required, the mode must be switched to the 8-color mode.

Figure 5–26. Partial Display Mode



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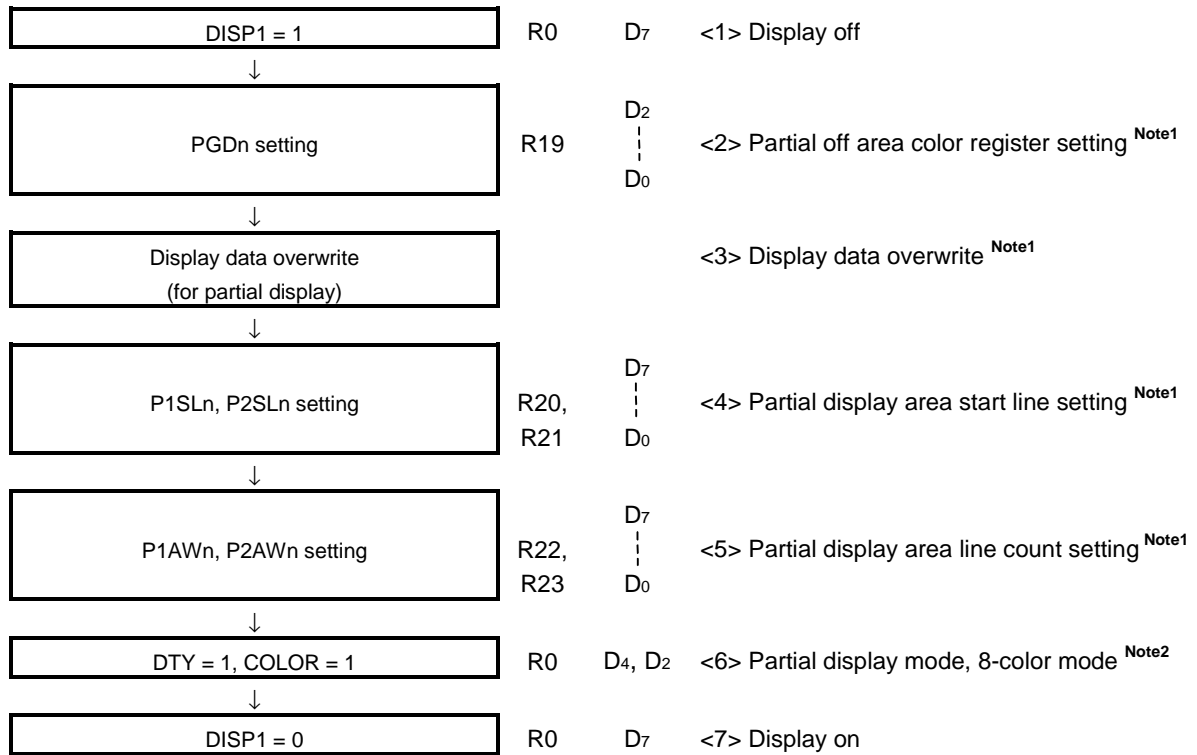
- Cautions**
1. The "scroll step count register (R17)" command is ignored in the partial display mode.
 2. The specified partial areas must not directly overlap, and the Partial 1 area and Partial 2 area must be separated by at least one line. If the areas overlap, only the Partial 1 settings are valid, and partial display is not performed for the Partial 2 area.
 3. When setting the partial display areas, be sure to observe the following relationship.

$$"00H" \leq R20 (R21)$$

$$R22 (R23) \leq "AFH"$$

The following sequence is recommended to avoid display malfunction when switching from normal display mode to partial display mode and vice versa.

(1) Recommended sequence for switching from normal display mode to partial display mode



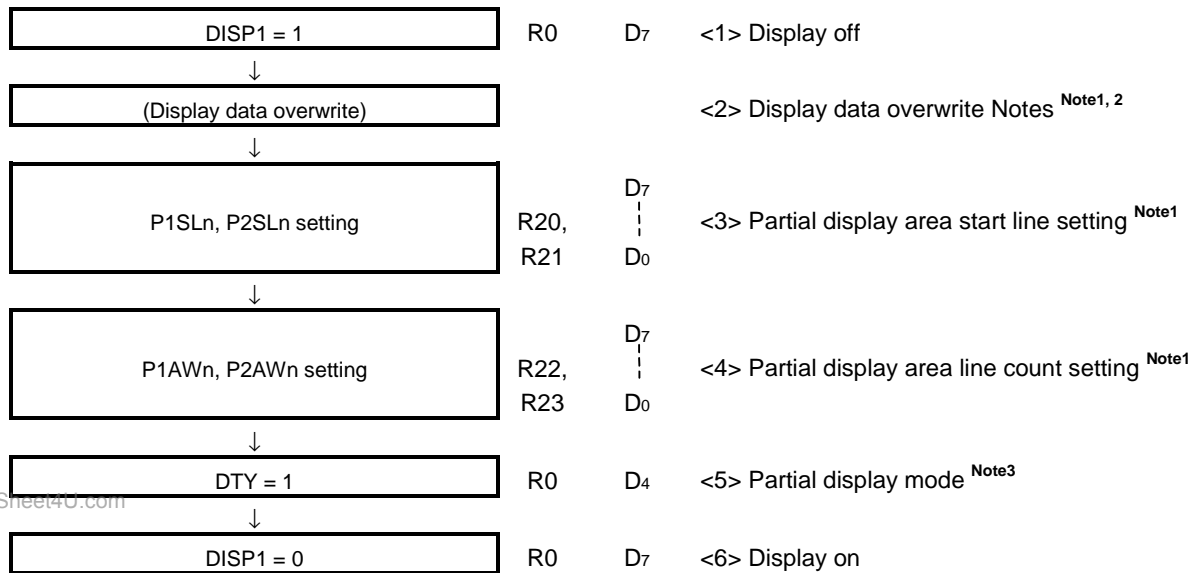
- Notes 1.** <2> to <5> can be executed in any order.
2. <6> must be executed after <4> and <5> have been set.

(2) Recommended sequence for switching from partial display mode to normal display mode



Note <2> to <3> can be executed in any order.

(3) Recommended sequence for switching from partial display mode to partial display mode (switching the partial display area)



Notes 1. <2> to <4> can be executed in any order.

2. Execute <2> only when necessary.

3. <5> must be executed after <3> and <4> have been set.

(4) Partial display setting examples

Setting A-1

| Register | Setting Value | Details of Setting Value |
|---|---------------|---------------------------|
| Partial display area start line register (R20, R21) | 00H | Sets Y address 00H |
| Partial display area line count register (R22, R23) | 78H | Sets an area of 120 lines |

Setting A-2

| Register | Setting Value | Details of Setting Value |
|---|---------------|---------------------------|
| Partial display area start line register (R20, R21) | 78H | Sets Y address 78H |
| Partial display area line count register (R22, R23) | 78H | Sets an area of 120 lines |

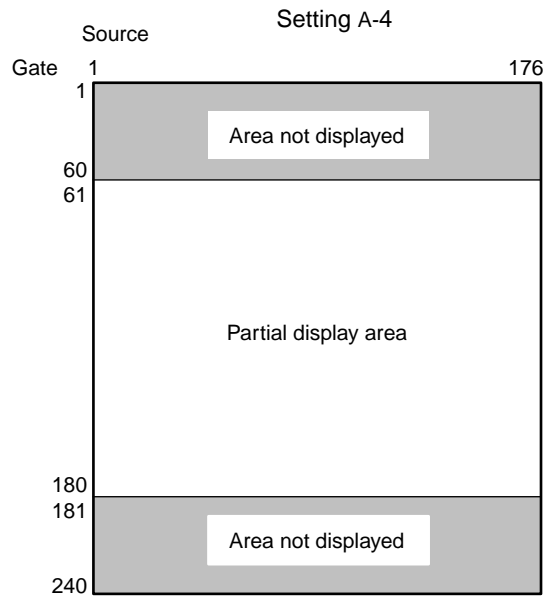
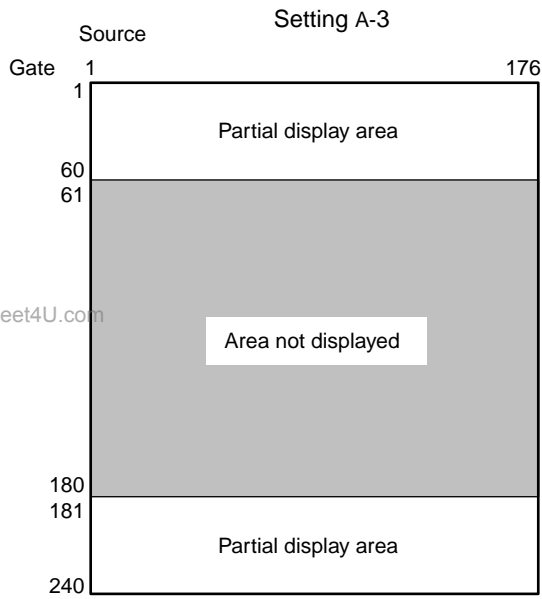
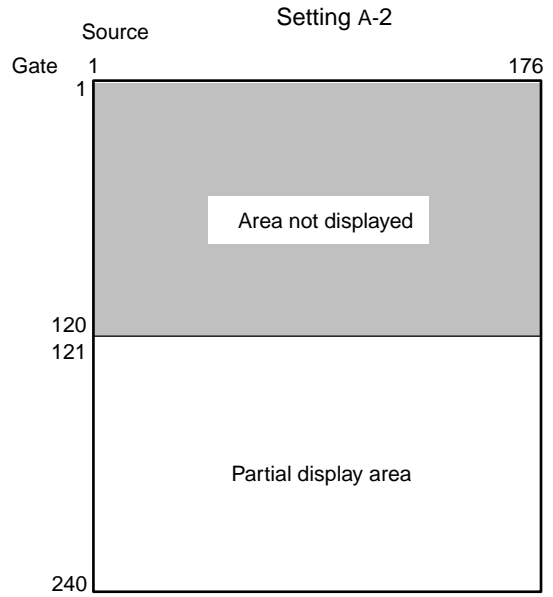
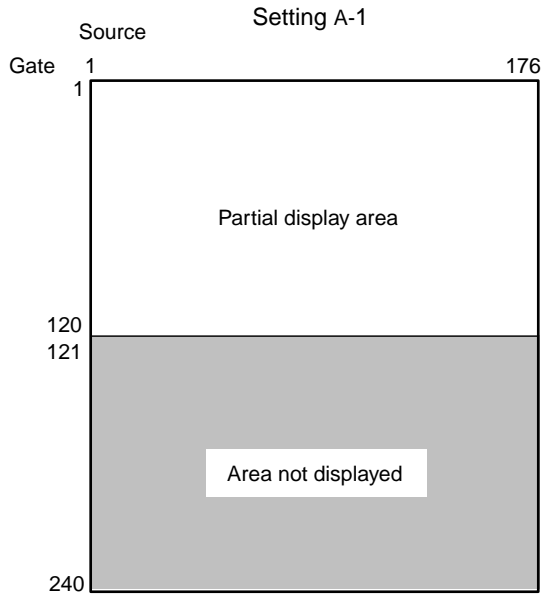
Setting A-3

| Register | Setting Value | Details of Setting Value |
|---|---------------|---------------------------|
| Partial display area start line register (R20, R21) | B4H | Sets Y address B4H |
| Partial display area line count register (R22, R23) | 78H | Sets an area of 120 lines |

Setting A-4

| Register | Setting Value | Details of Setting Value |
|---|---------------|---------------------------|
| Partial display area start line register (R20, R21) | 3CH | Sets Y address 3CH |
| Partial display area line count register (R22, R23) | 78H | Sets an area of 120 lines |

Figure 5-27. Partial Display Setting Examples



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5.11 Screen Scroll

The μ PD161623 has a screen scroll function. Any area of the screen can be scrolled by using the scroll area start line register (R15), scroll area line count register (R16), and scroll step count register (R17) to set the Y address of the top line of the area to be scrolled, the count of lines of the area to be scrolled, and the scroll step number, respectively.

Note that in partial mode, the screen scroll function is disabled.

Table 5–13. Scroll Area Start Line Register (R15)

| SSL7 | SSL6 | SSL5 | SSL4 | SSL3 | SSL2 | SSL1 | SSL0 | Start Line Y Address |
|------|------|------|------|------|------|------|------|----------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01H |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02H |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03H |
| | | | | ⋮ | | | | ⋮ |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | EDH |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | EEH |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | EFH |

Table 5–14. Scroll Area Line Count Register (R16)

| SAW7 | SAW6 | SAW5 | SAW4 | SAW3 | SAW2 | SAW1 | SAW0 | Scroll Area Line Number |
|------|------|------|------|------|------|------|------|-------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 3 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 4 |
| | | | | ⋮ | | | | ⋮ |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 238 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 239 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 240 |

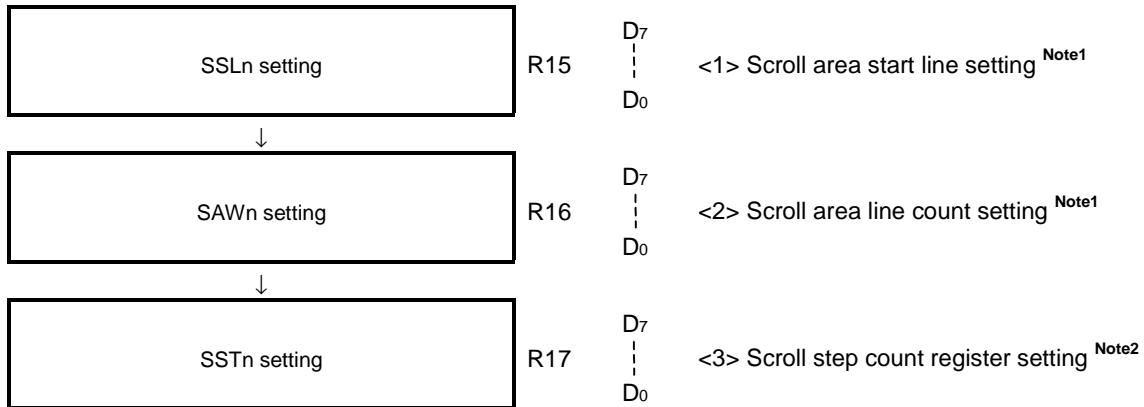
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Table 5–15. Scroll Step Count Register (R17)

| SST7 | SST6 | SST5 | SST4 | SST3 | SST2 | SST1 | SST0 | Scroll Step Number |
|------|------|------|------|------|------|------|------|--------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 (No scroll) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| | | | | ⋮ | | | | ⋮ |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 237 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 238 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 239 |

Scrolling must be set using the following sequence.

(1) Recommended scroll sequence



- Notes**
1. <1> to <2> can be executed in any order.
 2. <3> must be executed after <1> and <2> have been set.

Remark Set SSTn to 00H to disable the scroll operation. No particular sequence is required for this.

- Cautions**
1. If the sum of the values of SSLn and SAWn is 240 (EFH) or over, it is invalid (no scroll operation).
 2. Set the step number SSTn so that it does not exceed the line number SAWn. If a value exceeding SAWn is set, it will be invalid (no scroll operation).

(2) Scroll setting examples

Setting A-1

| Register | Setting Value | Details of Setting Value |
|---------------------------------------|---------------|---------------------------|
| Scroll area start line register (R15) | 00H | Sets Y address 00H |
| Scroll area line count register (R16) | EFH | Sets an area of 240 lines |

Setting A-2

| Register | Setting Value | Details of Setting Value |
|---------------------------------------|---------------|---------------------------|
| Scroll area start line register (R15) | 00H | Sets Y address 00H |
| Scroll area line count register (R16) | 77H | Sets an area of 120 lines |

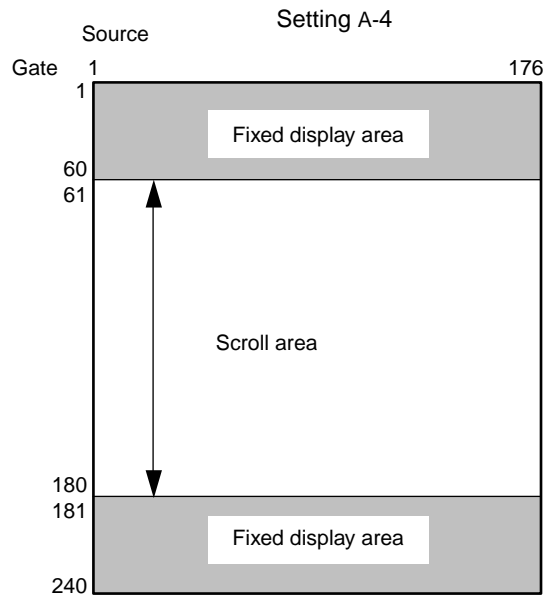
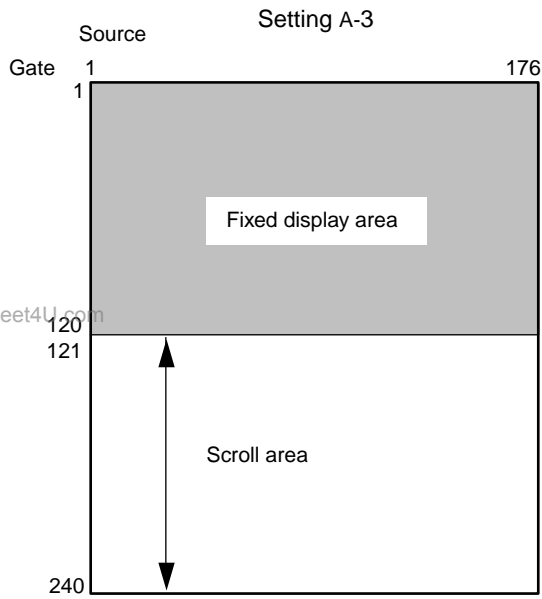
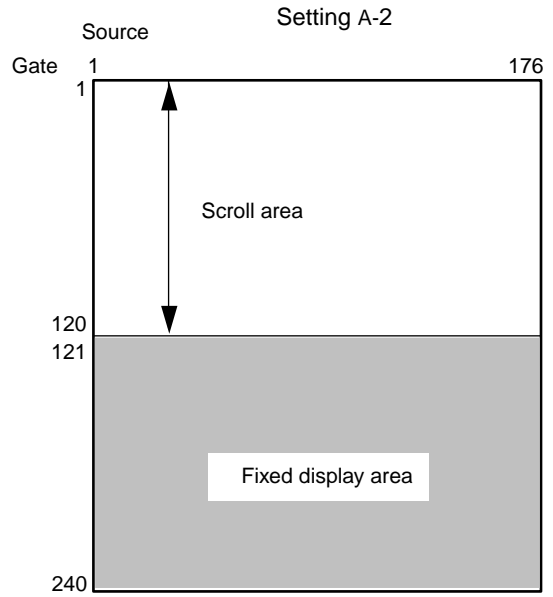
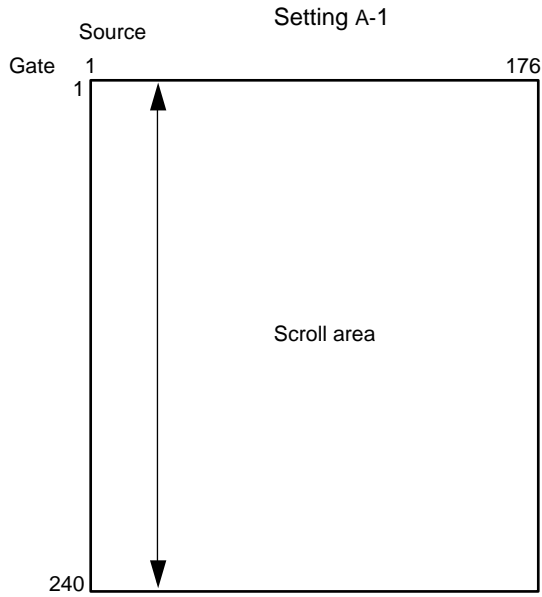
Setting A-3

| Register | Setting Value | Details of Setting Value |
|---------------------------------------|---------------|---------------------------|
| Scroll area start line register (R15) | 78H | Sets Y address 78H |
| Scroll area line count register (R16) | 77H | Sets an area of 120 lines |

Setting A-4

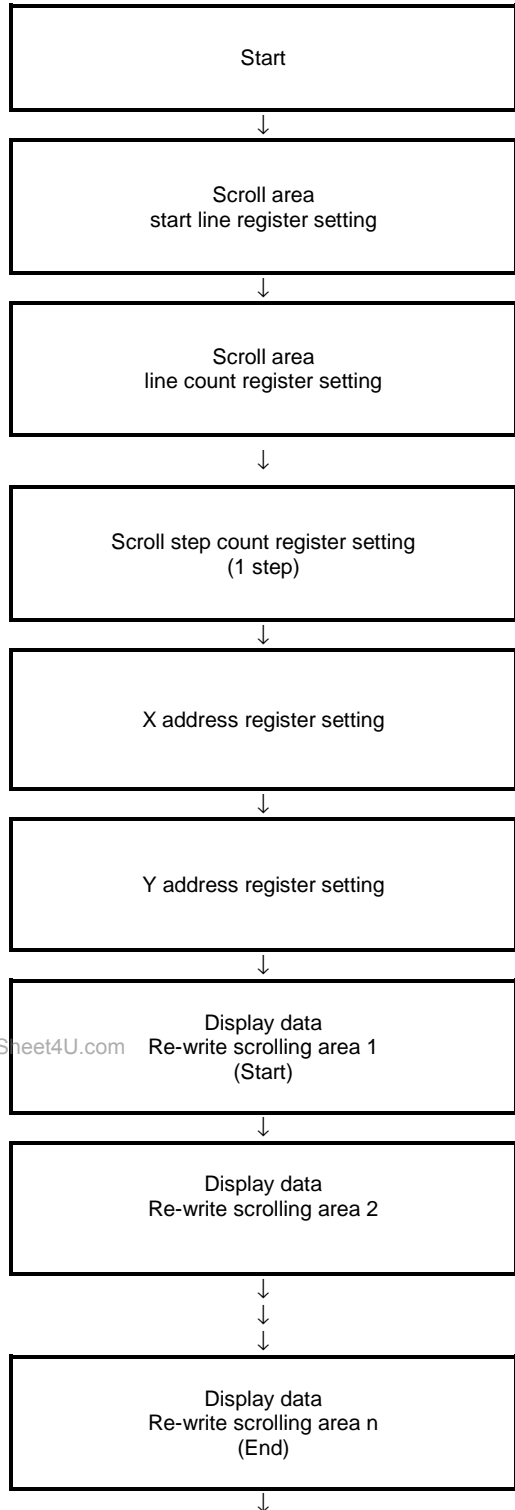
| Register | Setting Value | Details of Setting Value |
|---------------------------------------|---------------|---------------------------|
| Scroll area start line register (R15) | B4H | Sets Y address B4H |
| Scroll area line count register (R16) | 77H | Sets an area of 120 lines |

Figure 5-28. Display Scroll Setting Examples



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(3) Scroll setting flowchart example



R15

| | | | | | | | | | |
|----|----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|--|
| RS | | D ₁₅ | | | | | | D ₈ | |
| | | D ₇ | | | | | | D ₀ | |
| L | X | 0 | 0 | 0 | 1 | 1 | 1 | 1 | |
| | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | |

Caution D₇ to D₀ are the data for Scroll area start line.

R16

| | | | | | | | | | |
|----|----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|--|
| RS | | D ₁₅ | | | | | | D ₈ | |
| | | D ₇ | | | | | | D ₀ | |
| L | X | 0 | 0 | 1 | 0 | 0 | 0 | 0 | |
| | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | |

Caution D₇ to D₀ are the data for Scroll area line count register.

R17

| | | | | | | | | | |
|----|----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|--|
| RS | | D ₁₅ | | | | | | D ₈ | |
| | | D ₇ | | | | | | D ₀ | |
| L | X | 0 | 0 | 1 | 0 | 0 | 0 | 1 | |
| | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | |

R6

| | | | | | | | | | |
|----|----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|--|
| RS | | D ₁₅ | | | | | | D ₈ | |
| | | D ₇ | | | | | | D ₀ | |
| L | X | 0 | 0 | 0 | 0 | 1 | 1 | 0 | |
| | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | |

Caution D₇ to D₀ depend on application condition.

R7

| | | | | | | | | | |
|----|----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|--|
| RS | | D ₁₅ | | | | | | D ₈ | |
| | | D ₇ | | | | | | D ₀ | |
| L | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | |
| | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | |

Caution D₇ to D₀ depend on application condition.

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| | | | | | | | | | |
|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|--|
| RS | | D ₁₅ | | | | | | D ₈ | |
| | | D ₇ | | | | | | D ₀ | |
| H | D ₁₅ | D ₁₄ | D ₁₃ | D ₁₂ | D ₁₁ | D ₁₀ | D ₉ | D ₈ | |
| | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | |

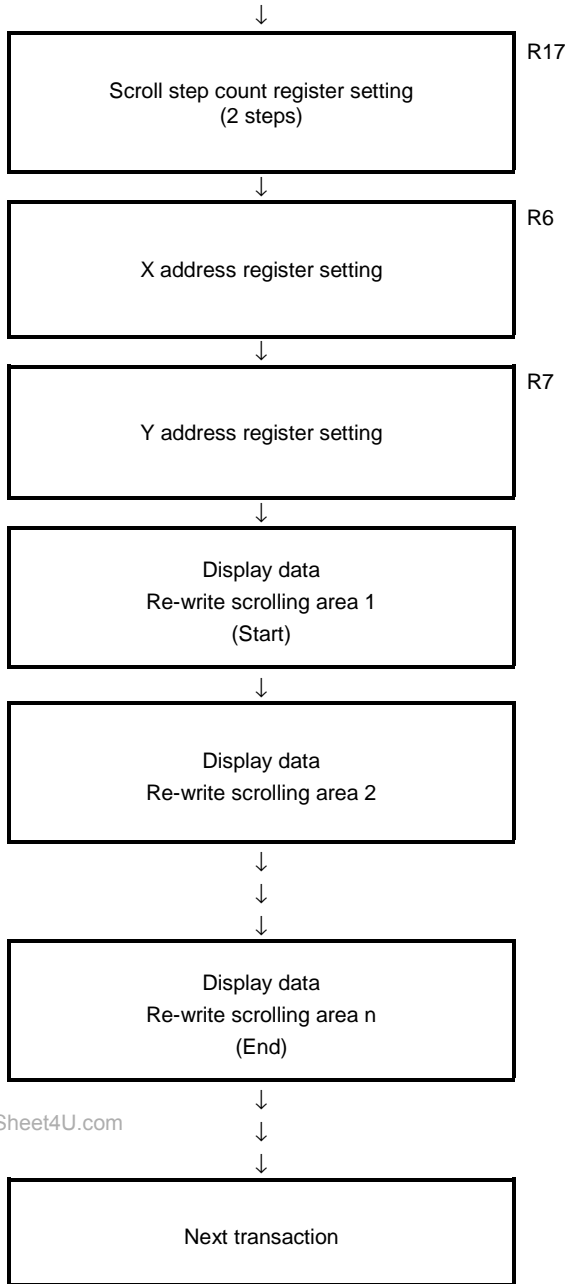
Caution D₁₅ to D₀ are display memory data.

| | | | | | | | | | |
|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|--|
| RS | | D ₁₅ | | | | | | D ₈ | |
| | | D ₇ | | | | | | D ₀ | |
| H | D ₁₅ | D ₁₄ | D ₁₃ | D ₁₂ | D ₁₁ | D ₁₀ | D ₉ | D ₈ | |
| | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | |

Caution D₁₅ to D₀ are display memory data.

| | | | | | | | | | |
|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|--|
| RS | | D ₁₅ | | | | | | D ₈ | |
| | | D ₇ | | | | | | D ₀ | |
| H | D ₁₅ | D ₁₄ | D ₁₃ | D ₁₂ | D ₁₁ | D ₁₀ | D ₉ | D ₈ | |
| | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | |

Caution D₁₅ to D₀ are display memory data.



| | | | | | | | | | |
|----|----------------|-----------------|---|---|---|---|---|----------------|--|
| RS | | D ₁₅ | | | | | | D ₈ | |
| | | D ₇ | | | | | | D ₀ | |
| L | X | 0 | 0 | 1 | 0 | 0 | 1 | 0 | |
| | D ₇ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | |

| | | | | | | | | | |
|----|----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|--|
| RS | | D ₁₅ | | | | | | D ₈ | |
| | | D ₇ | | | | | | D ₀ | |
| L | X | 0 | 0 | 0 | 0 | 1 | 1 | 0 | |
| | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | |

Caution D₇ to D₀ depend on application condition.

| | | | | | | | | | |
|----|----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|--|
| RS | | D ₁₅ | | | | | | D ₈ | |
| | | D ₇ | | | | | | D ₀ | |
| L | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | |
| | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | |

Caution D₇ to D₀ depend on application condition.

| | | | | | | | | | |
|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|--|
| RS | | D ₁₅ | | | | | | D ₈ | |
| | | D ₇ | | | | | | D ₀ | |
| H | D ₁₅ | D ₁₄ | D ₁₃ | D ₁₂ | D ₁₁ | D ₁₀ | D ₉ | D ₈ | |
| | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | |

Caution D₁₅ to D₀ are display memory data.

| | | | | | | | | | |
|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|--|
| RS | | D ₁₅ | | | | | | D ₈ | |
| | | D ₇ | | | | | | D ₀ | |
| H | D ₁₅ | D ₁₄ | D ₁₃ | D ₁₂ | D ₁₁ | D ₁₀ | D ₉ | D ₈ | |
| | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | |

Caution D₁₅ to D₀ are display memory data.

| | | | | | | | | | |
|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|--|
| RS | | D ₁₅ | | | | | | D ₈ | |
| | | D ₇ | | | | | | D ₀ | |
| H | D ₁₅ | D ₁₄ | D ₁₃ | D ₁₂ | D ₁₁ | D ₁₀ | D ₉ | D ₈ | |
| | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | |

Caution D₁₅ to D₀ are display memory data.

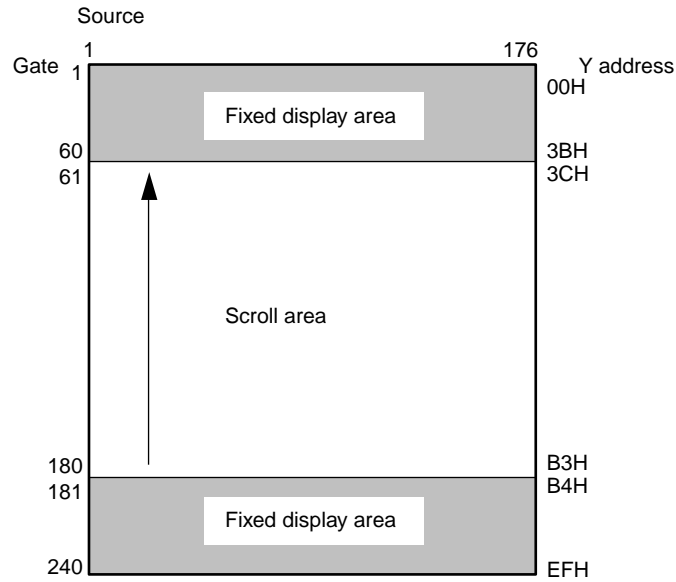
(Repeat)

(4) Scroll function example

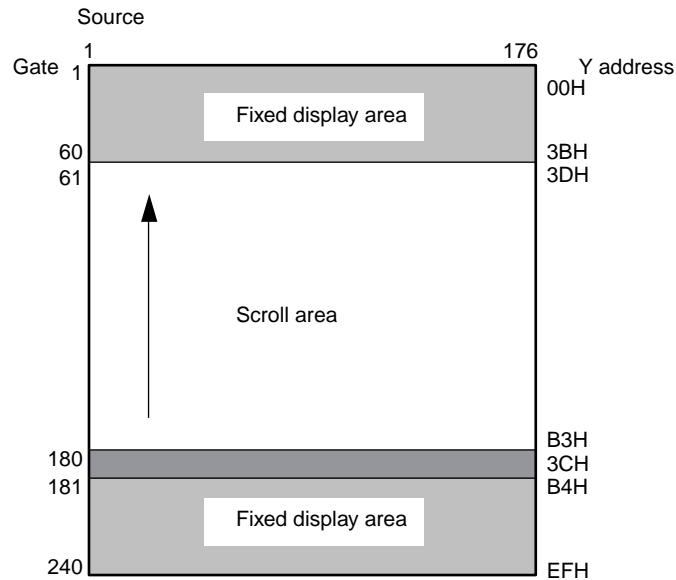
Scroll area start line register (R15): 3CH

Scroll area line count register (R16): 77H

(a) Scroll step count register setting (R17): 00H

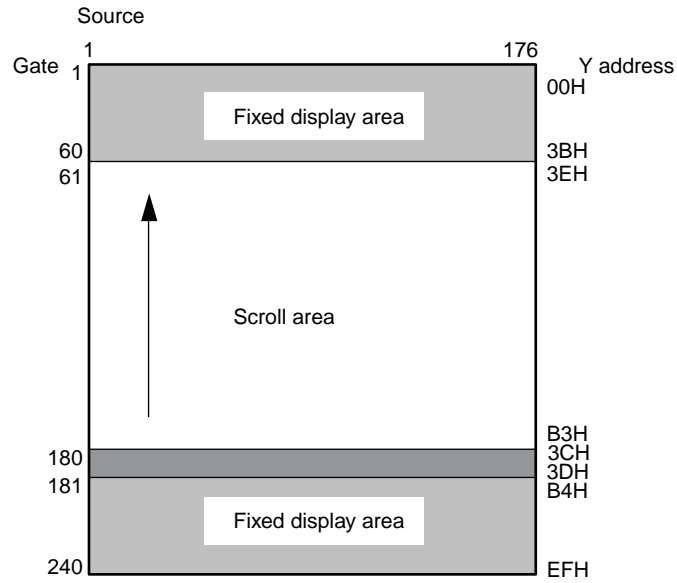


(b) Scroll step count register setting (R17): 01H

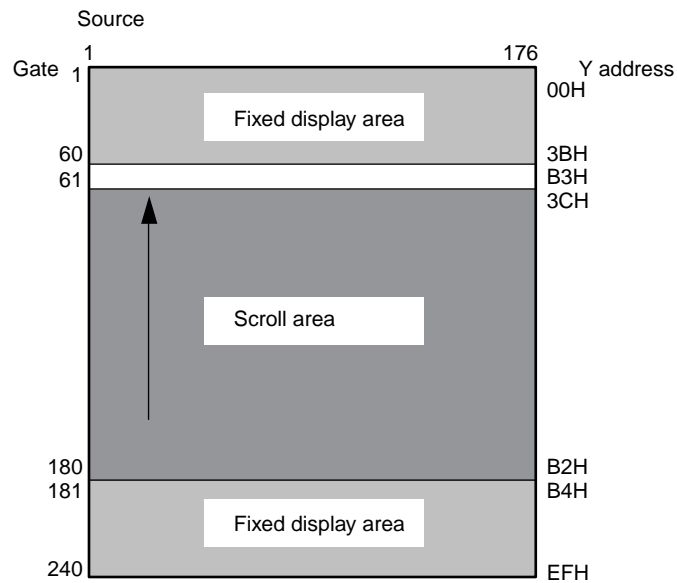


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(c) Scroll step count register setting (R17): 02H



(d) Scroll step count register setting (R17): 57H



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5.12 Stand-by

The μ PD161623 has a stand-by function. Input of a stand-by command is acknowledged when the STBY bit of the control register 1 (R0) is set to 1.

When the stand-by command has been input, the μ PD161623 is forcibly placed in the V_{SS} display status, and scans the frame being display to the end. When scanning is complete, all gate outputs are turned on, the charge of the pixel on the TFT panel is decreased to 0, and the output stage amplifier and internal oscillator are stopped.

The stand-by function is valid for only the source driver IC; the gate IC (μ PD161641) and power IC (μ PD161660) connected to the μ PD161623 are not controlled by this function.

After executing the stand-by command, therefore, execute commands that turn off the regulator for the gate IC and power IC and turn off the DC/DC converter.

When the stand-by status is released, turn on the DC/DC converter and the regulator of the gate IC and power IC, and then issue an ordinary operation command (STBY = 0), in the reverse order to which the stand-by command was input.

(1) Stand-by sequence

Operating status (normal display)

Control register 1 setting

R0

D₁₅ to D₀ Control register 1

| RS | D ₁₅ to D ₇ | | | | | | | D ₆ to D ₀ | |
|----|-----------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------------------------|----------------|
| | D ₁₅ | D ₁₄ | D ₁₃ | D ₁₂ | D ₁₁ | D ₁₀ | D ₉ | D ₈ | D ₀ |
| L | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | X | X | D ₅ | 0 | 1 | 0 | 0 | 0 | 0 |

- D₇: Don't care
- D₆: Don't care
- D₄: Normal display mode (not partial display mode)
- D₃: Stand-by ON
- D₂: 65,000-color display mode
- D₁: Normal power mode
- D₅ is set in accordance with the usage conditions.
- The source output is automatically fixed to the V_{SS} level by stand-by, so D₇ and D₆ can be set to any value.
- At least one frame period

Wait time 1 (t_{OE2RG})

<Power supply control sequence>

Power supply control register 1 setting

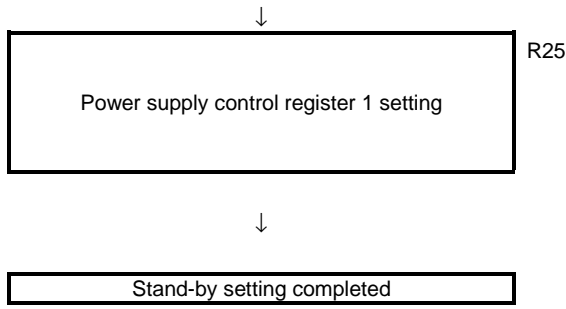
R25

D₁₅ to D₀ Power supply control register 1

| RS | D ₁₅ to D ₇ | | | | | | | D ₆ to D ₀ | |
|----|-----------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------------------------|----------------|
| | D ₁₅ | D ₁₄ | D ₁₃ | D ₁₂ | D ₁₁ | D ₁₀ | D ₉ | D ₈ | D ₀ |
| L | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| | X | D ₆ | D ₅ | D ₄ | D ₃ | X | 0 | 0 | 1 |

- D₆ to D₃ are set in accordance with the usage conditions.
- D₁: Power supply IC regulator OFF
- D₀: DC/DC converter ON
- Although a setting of 0 ns has no negative effect in terms of the device, be sure to finalize the timing after sufficient evaluation with the LCD module.

Wait time 2 (t_{RPDD})



R25

D₁₅ to D₀ Power supply control register 1

| | | | | | | | | | |
|----|--|-----------------|----------------|----------------|----------------|----------------|---|---|----------------|
| RS | | D ₁₅ | | | | | | | D ₈ |
| | | D ₇ | | | | | | | D ₀ |
| L | | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| | | X | D ₆ | D ₅ | D ₄ | D ₃ | X | 0 | 0 |

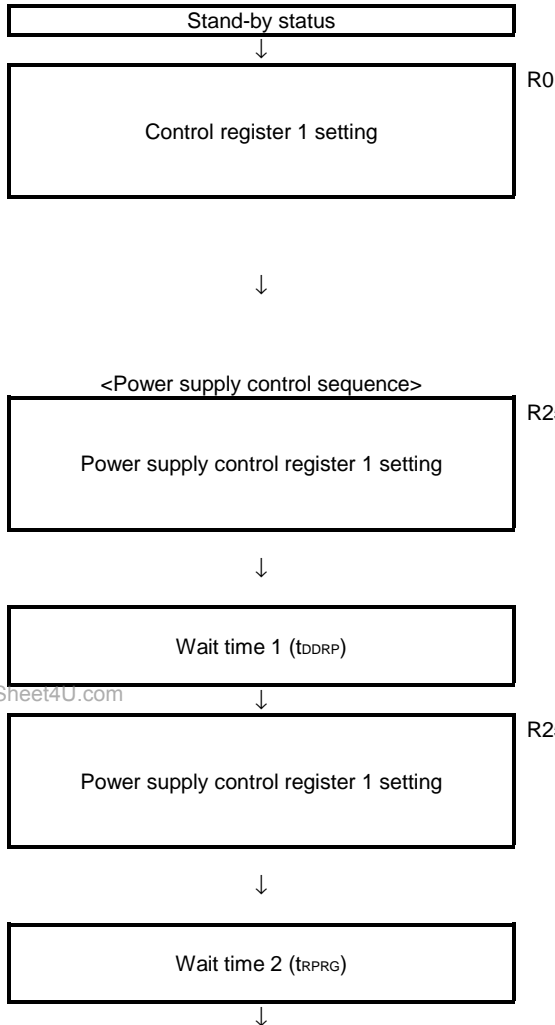
D₆ to D₃ are set in accordance with the usage conditions.

D₂: Gate driver regulator OFF

D₁: Power supply IC regulator OFF

D₀: DC/DC converter OFF

(2) Stand-by release sequence



R0

D₇ to D₀ Control register 1

| | | | | | | | | | |
|----|--|-----------------|---|----------------|---|----------|---|---|----------------|
| RS | | D ₁₅ | | | | | | | D ₈ |
| | | D ₇ | | | | | | | D ₀ |
| L | | X | X | X | X | X | X | X | X |
| | | 1 | 0 | D ₅ | 0 | 0 | 0 | 0 | 0 |

D₇: All data "1" output (normally white: white output)

D₆: Normal display

D₄: Normal display mode (not partial display mode)

D₃: Normal mode (stand-by release)

D₂: 65,000-color display mode

D₁: Normal power mode

D₅ is set in accordance with the usage conditions.

R25

D₁₅ to D₀ Power supply control register 1

| | | | | | | | | | |
|----|--|-----------------|----------------|----------------|----------------|----------------|---|---|----------------|
| RS | | D ₁₅ | | | | | | | D ₈ |
| | | D ₇ | | | | | | | D ₀ |
| L | | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| | | X | D ₆ | D ₅ | D ₄ | D ₃ | X | 0 | 1 |

D₆ to D₃ is set in accordance with the usage conditions.

D₁: Power supply IC regulator OFF

D₀: DC/DC converter ON

t_{DDRP} is the output stable period of the DC/DC converter.

Although a setting of about 50 ms is the target, be sure to finalize the timing after sufficient evaluation with the LCD module.

R25

D₇ to D₀ Power supply control register 1

| | | | | | | | | | |
|----|--|-----------------|----------------|----------------|----------------|----------------|---|----------|----------------|
| RS | | D ₁₅ | | | | | | | D ₈ |
| | | D ₇ | | | | | | | D ₀ |
| L | | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| | | X | D ₆ | D ₅ | D ₄ | D ₃ | 0 | 1 | 1 |

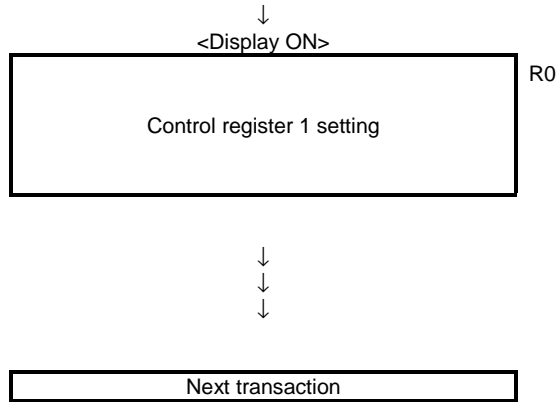
D₆ to D₃ is set in accordance with the usage conditions.

D₁: Power supply IC regulator ON

D₀: DC/DC converter ON

t_{RPRG} is the output stable period of the DC/DC converter.

Although a setting of about 20 ms is the target, be sure to finalize the timing after sufficient evaluation with the LCD module.



D7 to D0 Control register 1

| | | | | | | | | |
|---|-----------------|---|----------------|---|----------|---|---|----------------|
| | RS | | | | | | | D ₈ |
| | D ₁₅ | | | | | | | D ₀ |
| | D ₇ | | | | | | | |
| L | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | D ₅ | 0 | 0 | 0 | 0 | 0 |

D7: Normal display (All data "1" output → display ON)

D6: Normal display

D4: Normal display mode (not partial display mode)

D3: Normal mode (stand-by release)

D2: 65,000-color display mode

D1: Normal power mode

D₅ is set in accordance with the usage conditions.

6 RESET

If the /RESET input becomes L or the reset command is input, the internal timing generator is initialized. The reset command will also initialize each register to its default value. These default values are listed in the table below.

| Register | Rn | /RESET Pin ^{Note1} | Reset Command | Default Value |
|---|------|-----------------------------|---------------|---------------|
| Control register 1 | R0 | X | O | A0H |
| Control register 2 | R1 | X | O | 00H |
| Data supplement register | R4 | X | O | 00H |
| Data access control register | R5 | X | O | 00H |
| X address register | R6 | X | O | 00H |
| Y address register | R7 | X | O | 00H |
| MIN. ·X address register | R8 | X | O | 00H |
| MAX. ·X address register | R9 | X | O | 00H |
| MIN. ·Y address register | R10 | X | O | 00H |
| MIN. ·Y address register | R11 | X | O | 00H |
| Display size setting register | R13 | X | O | 00H |
| Scroll area start line register | R15 | X | O | 00H |
| Scroll area line count register | R16 | X | O | 00H |
| Scroll step count register | R17 | X | O | 00H |
| Partial off area color register | R19 | X | O | 00H |
| Partial 1 display area start line register | R20 | X | O | 00H |
| Partial 2 display area start line register | R21 | X | O | 00H |
| Partial 1 display area line count register | R22 | X | O | 00H |
| Partial 2 display area line count register | R23 | X | O | 00H |
| Power supply control register 1 | R25 | X | O | 00H |
| Power supply control register 2 | R26 | X | O | 00H |
| VCOM output center value setting register | R29 | X | O | 00H |
| Output stage capacity setting register | R30 | X | O | 00H |
| γ-reference-voltage generator capacity setting register | R31 | X | O | 00H |
| γ-contrast value setting register 1 | R36 | X | O | 00H |
| γ-contrast value setting register 2 | R37 | X | O | 00H |
| γ-contrast value setting register 3 | R38 | X | O | 00H |
| γ-contrast value setting register 4 | R39 | X | O | 00H |
| ★ Pre-charge direction setting data register | R40 | X | O | 00H |
| γ-correction input disconnect register | R42 | X | O | 00H |
| Calibration register ^{Note2} | R45 | X | O | 01H |
| ★ Pre-charge period supplement pulse setting register | R46 | X | O | 06H |
| Output port register | R49 | X | O | 00H |
| Interface operating voltage setting register | R114 | X | O | 00H |
| Internal logic operating voltage setting register | R115 | X | O | 00H |
| Test mode | | X | O | 00H |

Remark O: Default value set, X: Default value not set

Notes 1. The internal counters are initialized only by a reset from the /RESET pin. Be sure to perform reset via the /RESET pin at power application.

2. The following value is set as the calibration setting time, t_{cal} , in a reset by reset command.

$$t_{cal} = 1/f_{OSC} \times 37$$

7. COMMAND

7.1 Command List

Display data access

| RAM access | RS | R/W | Data Bit | | | | | | | | | |
|--|----|-----|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|-------------------------------------|--|
| | | | DB ₁₇ | DB ₁₆ | DB ₁₅ | DB ₁₄ | DB ₁₃ | DB ₁₂ | DB ₁₁ | DB ₁₀ | DB ₉ | |
| | | | DB ₈ | DB ₇ | DB ₆ | DB ₅ | DB ₄ | DB ₃ | DB ₂ | DB ₁ | DB ₀ | |
| 18-bit parallel interface | | | | | | | | | | | | |
| Display data read 1 | 1 | 1 | D ₁₇ | D ₁₆ | D ₁₅ | D ₁₄ | D ₁₃ | D ₁₂ | D ₁₁ | D ₁₀ | D ₉ | |
| | | | D ₈ | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | |
| Display data write 1 | 1 | 0 | D ₁₇ | D ₁₆ | D ₁₅ | D ₁₄ | D ₁₃ | D ₁₂ | D ₁₁ | D ₁₀ | D ₉ | |
| | | | D ₈ | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | |
| 16-bit parallel interface (1-pixel/16-bit mode [DTX=L]) | | | | | | | | | | | | |
| Display data read 2 | 1 | 1 | Hi-Z | Hi-Z | D ₁₇ | D ₁₆ | D ₁₅ | D ₁₄ | D ₁₃ | D ₁₁ | D ₁₀ | |
| | | | D ₉ | D ₈ | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | |
| Display data write 2 | 1 | 0 | – | – | D ₁₇ | D ₁₆ | D ₁₅ | D ₁₄ | D ₁₃ | D ₁₁ | D ₁₀ | |
| | | | D ₉ | D ₈ | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | |
| 16-bit parallel interface (1-pixel / 18-bit mode [DTX=H]) | | | | | | | | | | | | |
| Display data read 3 | 1 | 1 | Hi-Z | Hi-Z | “0” | “0” | “0” | “0” | “0” | “0” | “0” | |
| | | | D ₁₇ (D ₈) | D ₁₆ (D ₇) | D ₁₅ (D ₆) | D ₁₄ (D ₅) | D ₁₃ (D ₄) | D ₁₂ (D ₃) | D ₁₁ (D ₂) | D ₁₀ (D ₁) | D ₉ (D ₀) | |
| Display data write 3 | 1 | 0 | Hi-Z | Hi-Z | X | X | X | X | X | X | X | |
| | | | D ₁₇ (D ₈) | D ₁₆ (D ₇) | D ₁₅ (D ₆) | D ₁₄ (D ₅) | D ₁₃ (D ₄) | D ₁₂ (D ₃) | D ₁₁ (D ₂) | D ₁₀ (D ₁) | D ₉ (D ₀) | |
| Common | | | | | | | | | | | | |
| Status Read | 0 | 1 | | | | | | | | | | |

Remark Hi-Z: High impedance, X: Invalid data

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Caution When the 16-bit parallel interface is used in 1-pixel/18-bit mode (DTX = H), data access of two words per pixel is required.

18-bit parallel interface mode, DB₁₇, DB₁₆ = 0

(1/3)

| Rn | Register | RS | R/W | Data Bit | | | | | | | | |
|-----|--|----|-----|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|---|
| | | | | DB ₁₅ | DB ₁₄ | DB ₁₃ | DB ₁₂ | DB ₁₁ | DB ₁₀ | DB ₉ | DB ₈ | |
| | | | | DB ₇ | DB ₆ | DB ₅ | DB ₄ | DB ₃ | DB ₂ | DB ₁ | DB ₀ | |
| R0 | Control register 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | DISP1 | DISP0 | ADC | DTY | STBY | COLOR | LPM | GSM | |
| R1 | Control register 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | | | | | | VSEL | GSEL | 0 | 0 | LTS | INV | |
| R2 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | |
| R3 | Reset register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | | | | | | | | | | RES | |
| R4 | Data supplement register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | |
| | | | | | | | | | | CD12 | CD0 | |
| R5 | Data access control register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | |
| | | | | | BSTR | | WAS | | 0 | 0 | 0 | |
| R6 | X address register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | |
| | | | | XA ₇ | XA ₆ | XA ₅ | XA ₄ | XA ₃ | XA ₂ | XA ₁ | XA ₀ | |
| R7 | Y address register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | |
| | | | | YA ₇ | YA ₆ | YA ₅ | YA ₄ | YA ₃ | YA ₂ | YA ₁ | YA ₀ | |
| R8 | MIN. X address register | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |
| | | | | XMIN ₇ | XMIN ₆ | XMIN ₅ | XMIN ₄ | XMIN ₃ | XMIN ₂ | XMIN ₁ | XMIN ₀ | |
| R9 | MAX. X address register | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | |
| | | | | XMAX ₇ | XMAX ₆ | XMAX ₅ | XMAX ₄ | XMAX ₃ | XMAX ₂ | XMAX ₁ | XMAX ₀ | |
| R10 | MIN. Y address register | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | |
| | | | | YMIN ₇ | YMIN ₆ | YMIN ₅ | YMIN ₄ | YMIN ₃ | YMIN ₂ | YMIN ₁ | YMIN ₀ | |
| R11 | MAX. Y address register | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | |
| | | | | YMAX ₇ | YMAX ₆ | YMAX ₅ | YMAX ₄ | YMAX ₃ | YMAX ₂ | YMAX ₁ | YMAX ₀ | |
| R12 | - | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | |
| R13 | Display size setting register | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | |
| | | | | | | | | | | | NGO0 | |
| R14 | - | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | |
| R15 | Scroll area start line register | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | |
| | | | | SSL ₇ | SSL ₆ | SSL ₅ | SSL ₄ | SSL ₃ | SSL ₂ | SSL ₁ | SSL ₀ | |
| R16 | Scroll area line count register | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | |
| | | | | SAW ₇ | SAW ₆ | SAW ₅ | SAW ₄ | SAW ₃ | SAW ₂ | SAW ₁ | SAW ₀ | |
| R17 | Scroll step count register | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | |
| | | | | SST ₇ | SST ₆ | SST ₅ | SST ₄ | SST ₃ | SST ₂ | SST ₁ | SST ₀ | |
| R18 | - | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | | |
| R19 | Partial off area color register | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | |
| | | | | | | | | | PGR | PGG | PGB | |
| R20 | Partial 1 display area start line register | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | |
| | | | | P1SL ₇ | P1SL ₆ | P1SL ₅ | P1SL ₄ | P1SL ₃ | P1SL ₂ | P1SL ₁ | P1SL ₀ | |
| R21 | Partial 2 display area start line register | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | |
| | | | | P2SL ₇ | P2SL ₆ | P2SL ₅ | P2SL ₄ | P2SL ₃ | P2SL ₂ | P2SL ₁ | P2SL ₀ | |

18-bit parallel interface mode, DB₁₇, DB₁₆ = 0

(2/3)

| Rn | Register | RS | R/W | Data Bit | | | | | | | |
|-----|---|----|-----|------------------|------------------|------------------|------------------|------------------|------------------|-----------------|-----------------|
| | | | | DB ₁₅ | DB ₁₄ | DB ₁₃ | DB ₁₂ | DB ₁₁ | DB ₁₀ | DB ₉ | DB ₈ |
| | | | | DB ₇ | DB ₆ | DB ₅ | DB ₄ | DB ₃ | DB ₂ | DB ₁ | DB ₀ |
| R22 | Partial 1 display area line count register | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| | | | | P1AW7 | P1AW6 | P1AW5 | P1AW4 | P1AW3 | P1AW2 | P1AW1 | P1AW0 |
| R23 | Partial 2 display area line count register | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| | | | | P2AW7 | P2AW6 | P2AW5 | P2AW4 | P2AW3 | P2AW2 | P2AW1 | P2AW0 |
| R24 | – | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| R25 | Power supply control register 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| | | | | | BGRS | VCE | VCD2 | PVCOM | | RGONP | DCON |
| R26 | Power supply control register 2 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| | | | | | | | | | | VCD12 | VCD11 |
| R27 | – | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| | | | | | | | | | | | |
| R28 | – | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| | | | | | | | | | | | |
| R29 | VCOM output center value setting register | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| | | | | EV7 | EV6 | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 |
| R30 | Output stage capacity setting register | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| | | | | BPL | CI2 | CI1 | CI0 | VCOMC | SF2 | SF1 | SF0 |
| R31 | γ-reference-voltage generator capacity setting register | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| | | | | WHP | WI2 | WI1 | WI0 | BHP | BI2 | BI1 | BI0 |
| R32 | – | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | | | | |
| R33 | – | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| | | | | | | | | | | | |
| R34 | – | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| | | | | | | | | | | | |
| R35 | – | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| | | | | | | | | | | | |
| R36 | γ-contrast value setting register 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| | | | | GPH7 | GPH6 | GPH5 | GPH4 | GPH3 | GPH2 | GPH1 | GPH0 |
| R37 | γ-contrast value setting register 2 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| | | | | GNH7 | GNH6 | GNH5 | GNH4 | GNH3 | GNH2 | GNH1 | GNH0 |
| R38 | γ-contrast value setting register 3 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| | | | | GPL7 | GPL6 | GPL5 | GPL4 | GPL3 | GPL2 | GPL1 | GPL0 |
| R39 | γ-contrast value setting register 4 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| | | | | GNL7 | GNL6 | GNL5 | GNL4 | GNL3 | GNL2 | GNL1 | GNL0 |
| R40 | Pre-charge direction setting data register | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| | | | | RDTP3 | RDTP2 | RDTP1 | RDTP0 | RDTN3 | RDTN2 | RDTN1 | RDTN0 |
| R41 | – | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| | | | | | | | | | | | |
| R42 | γ-correction input disconnect register | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| | | | | | | | | | | | GHSW |
| R43 | – | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| | | | | | | | | | | | |

18-bit parallel interface mode, DB₁₇, DB₁₆ = 0

(3/3)

| Rn | Register | RS | R/W | Data Bit | | | | | | | | |
|------|---|----|-----|------------------|------------------|------------------|------------------|------------------|------------------|-----------------|-----------------|--|
| | | | | DB ₁₅ | DB ₁₄ | DB ₁₃ | DB ₁₂ | DB ₁₁ | DB ₁₀ | DB ₉ | DB ₈ | |
| | | | | DB ₇ | DB ₆ | DB ₅ | DB ₄ | DB ₃ | DB ₂ | DB ₁ | DB ₀ | |
| R44 | – | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | |
| R45 | Calibration register | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | |
| R46 | Pre-charge period supplement pulse setting register | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | |
| R47 | – | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | |
| R48 | – | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | |
| R49 | Output port register | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | |
| R50 | – | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | |
| R51 | – | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | |
| R52 | – | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | |
| R53 | – | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | |
| R54 | – | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | |
| R55 | – | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | |
| R56 | – | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | |
| R57 | – | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | |
| R58 | – | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | |
| R59 | – | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | |
| R60 | – | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | |
| R61 | – | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | |
| R62 | – | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | |
| R63 | – | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | |
| R114 | Interface operating voltage setting register | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | |
| R115 | Internal logic operating voltage setting register | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | |

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7.2 Command Explanation

(1/8)

| Register | Bit | Symbol | Function |
|----------------|----------------|--|---|
| R0 | D ₇ | DISP1 | This command performs the same output as when all data is 1, independently of the internal RAM data (white display in the case of normally white). This command is executed, after it has been transferred, when the next line is output. 0: Normal operation 1: Ignores data of RAM and outputs all data as 1. DISP1 takes precedence over DISP0. When DISP1 = H, DISP0 = H is ignored. |
| | D ₆ | DISP0 | This command performs the same output as when all data is 0, independently of the internal RAM data (black display in the case of normally white). This command is executed, after it has been transferred, when the next line is output. 0: Normal operation 1: Ignores data of RAM and outputs all data as 0. |
| | D ₅ | ADC | Column address direction This command can be used to select the direction of source driver output. For more detail, refer to 5.2.3 Column address circuit . |
| | D ₄ | DTY | This pin selects the partial function. When the partial function is selected in the 260,000-color mode, set the partial-OFF area-color selection register (R27) to 00H. In the 8-color mode, the partial OFF area color can be set to any value from 00H to 07 H. The power consumption cannot be reduced with the partial function. To reduce the power consumption, select the 8-color mode. This command is executed following transfer from the time the next line data is output. 0: Normal display mode 1: Partial display mode |
| | D ₃ | STBY | This bit selects the stand-by function. When the stand-by function is selected, a display OFF operation is executed and the amplifiers at each output stage and the operation of internal oscillation circuit are stopped. However, stand-by control cannot be performed for the power supply ICs (μ PD161660 and others) connected to μ PD161623. Therefore, after executing the stand-by function using this bit, set both the regulator for the power supply IC to off and set the DC/DC converter to OFF. For the sequence, refer to the data sheets of the power supply IC. Note that when releasing stand-by, perform the opposite operation, i.e., after setting the DC/DC converter to ON and setting the regulators of the power supply IC to ON, execute the normal operation command. 0: Normal operation 1: Stand-by function (Display read off from RAM, stop both OSC and VCOM, display off = entire data is output as 1) |
| D ₂ | COLOR | This pin switches the 260,000-color mode and the 8-color mode. When the 8-color mode is selected, low power supply can be selected in order to stop the amplifier at each output stage. In the 8-color mode, the value of the MSB of the internal RAM data is used as the color data. This command is executed following transfer from the time the next line data is output. 0: 260,000-color mode (18-bits/pixels) 1: 8-color mode (3-bits/pixels) | |

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(2/8)

| Register | Bit | Symbol | Function |
|----------|----------------|--------|---|
| R0 | D ₁ | LPM | This bit is used when setting the power supply IC (μ PD161660) to the low-power mode. When the low-power mode is selected, the LPMP pin signal change from low to high (output changes immediately following command execution.). The LPMP pin must be connected to the LPM pin of the power supply IC. 0: Normal 1: Low power mode |
| | D ₀ | GSM | Sets output of the gate scanning signal during partial display. When 1 is selected, gate scanning of the line set in the partial non-display area is stopped. 0: Normal mode 1: Stops gate scanning in partial non-display area |
| R1 | D ₅ | VSEL | Sets the potential of the pre-charge output of the LCD driver. The maximum/minimum output potential of the pre-charge output is: 0: Maximum output level of internal γ -output adjustment circuit (uses VPH, VNH, VPL, VNL) 1: Partial voltage (outputs V _s and V _{ss}) IF VSEL = 0, V _s or V _{ss} is automatically output as the pre-charge output. |
| | D ₄ | GSEL | Sets the maximum/minimum output voltage of the γ -correction register. If the internal γ -output adjustment circuit is selected, the maximum/minimum output potential of the γ -correction register is: 0: Supply voltage (outputs V _s and V _{ss}). 1: Voltage of internal γ -output adjustment circuit (uses VPH, VNH, VPL, VNL) 8-color mode (3 bits/pixels) |
| | D ₁ | LTS | Selects set time of calibration. The calibration function adjusts the frame frequency by setting time of one line. This command can select the set time of a line from the following: 0: 1 line time = t _{cal} 1: 1 line time = t _{cal} x 2 (t _{cal} : Calibration set time = 1 ÷ Frame frequency ÷ Number of displayed lines) |
| | D ₀ | INV | This bit selects between the line inversion function and the frame inversion function. The mode selected by this command is executed from the start of the next scan after the gate scan in progress when this command was executed has completed 176 lines. 0: Line inversion 1: Frame inversion |
| R3 | D ₀ | RES | Command reset function. Be sure to execute this bit after power ON. Command reset automatically clears this bit following execution (RES = 1). Therefore, it is not necessary to set 0 (select normal operation) again by software. Moreover, since the time required for the value of this bit to change (1 → 0) following command reset execution is extremely short, it is not necessary to secure time until the next command is set following command reset setting. 0: Normal operation 1: Command reset |
| R4 | D ₁ | CD12 | When using the 1-pixel/16-bit mode (DTX = L) and the 18-bit parallel interface, when the data from the CPU is stored in the display RAM, this register supplements data (display RAM data: D ₁₂ , D ₀) for the two bits of deficient data using the set data and writes 18-bit data to the display RAM. For details, refer to 5.1.2 Selection of data transfer mode. CD12: Display RAM data D ₁₂ is supplemented CD0: Display RAM data D ₀ is supplemented |
| | D ₀ | CD0 | |

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| Register | Bit | Symbol | Function | | | | | | |
|----------|----------------------------------|--------|---|------|--------------------|---|------------------|---|------------------|
| R5 | D ₆ | BSTR | Sets the write mode for writing data to the display RAM. If the high-speed RAM write mode is selected, data is written to the display RAM in 2-pixel units inside the μ PD161623. When selecting the high-speed RAM write mode, be sure to write data to the display RAM in 2-pixel units. 0: Normal write mode (18-bit access: 4 MHz MAX.) 1: High-speed RAM write mode (36-bit access: 8 MHz MAX.) | | | | | | |
| | D ₄ | WAS | Window access mode setting When the window access mode is set, the address is incremented/decremented only in the range set by the MIN. ·X address setting register (R8), MAX. ·X address setting register (R9), MIN. ·Y address setting register (R10), and MAX. ·Y address setting register (R11). 0: Normal operation 1: Window access mode | | | | | | |
| R6 | D ₇ to D ₀ | XAn | This register sets the X address of the display RAM. Set a value between 00H and AFH. | | | | | | |
| R7 | D ₇ to D ₀ | YAn | This register sets the Y address of the display RAM. Set a value between 00H and EFH. | | | | | | |
| R8 | D ₇ to D ₀ | XMINn | Sets the minimum value of the X address in the window access mode. The X address is incremented up to the maximum value set by the MAX. ·X address register (R9), and then initialized to the address value set by this command. Set this register to 00H to AEH. | | | | | | |
| R9 | D ₇ to D ₀ | XMAXn | Sets the maximum value of the X address in the window access mode. The X address is incremented up to the maximum value set by the MIN. ·X address register (R8), and then initialized to the address value set by this command. Set this register to 01H to AFH. | | | | | | |
| R10 | D ₇ to D ₀ | YMINn | Sets the minimum value of the T address in the window access mode. The Y address is incremented up to the maximum value set by the MAX. ·Y address register (R11), and then initialized to the address value set by this command. Set 00H to EEH. | | | | | | |
| R11 | D ₇ to D ₀ | YMAXn | Sets the maximum value of the Y address in the window access mode. The Y address is incremented up to the address value set by this command, and then initialized to the minimum address value set by the MIN. ·Y address register (R10). Set 01H to EFH. | | | | | | |
| R13 | D ₀ | NGOO | Selects output number (gate scan) of gate driver. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>NGOO</th> <th>Gate Output Number</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>240-gate outputs</td> </tr> <tr> <td>1</td> <td>220-gate outputs</td> </tr> </tbody> </table> | NGOO | Gate Output Number | 0 | 240-gate outputs | 1 | 220-gate outputs |
| NGOO | Gate Output Number | | | | | | | | |
| 0 | 240-gate outputs | | | | | | | | |
| 1 | 220-gate outputs | | | | | | | | |
| R15 | D ₇ to D ₀ | SSLn | Scroll area start line register (00H to EFH) When the screen is scrolled, the screen of the number of lines set by the scroll area line count register (R16) is scrolled up by the number of steps set by the scroll step count register (R17), starting from the line set by this command. | | | | | | |
| R16 | D ₇ to D ₀ | SAWn | Scroll area line count register (00H to EFH) When the screen is scrolled, the screen of the number of lines set by this command is scrolled up by the number of steps set by the scroll step count register (R17), starting from the line set by the scroll area start line register (R15). | | | | | | |

(4/8)

| Register | Bit | Symbol | Function |
|----------|----------------------------------|-------------------|---|
| R17 | D ₇ to D ₀ | SST _n | <p>Scroll step count register (00H to EFH)</p> <p>When the screen is scrolled, the screen of the number of lines set by the scroll area line count register (R16) and the scroll step count register (R17) is scrolled up by the number of steps set by this command.</p> <p>Note that because this command is invalid in the partial display mode, the scroll function cannot be used.</p> |
| R19 | D ₂ | PGR | <p>Partial off area color register</p> <p>Sets the color of the screen other than the partial display area during partial display (R0: DTY = 1). One of eight colors can be selected (RGB: 1 bit each) as the off color.</p> <p>The relationship between each color data and the bits of this register is as follows.</p> <p>This relationship is not dependent upon the value of ADC.</p> <p>PGR: R OFF= 0, ON = 1 PGG: G OFF= 0, ON = 1 PGB: B OFF= 0, ON = 1</p> |
| | D ₁ | PGG | |
| | D ₀ | PGB | |
| R20 | D ₇ to D ₀ | P1SL _n | <p>Partial1 display area start line register (00H to EFH)</p> <p>During partial display (R0: DTY = 1), the area starting from the line set by this command and ending as set by the partial 1 display area line count register (R22) is the partial 1 display area.</p> |
| R21 | D ₇ to D ₀ | P2SL _n | <p>Partial2 display area start line register (00H to EFH)</p> <p>During partial display (R0: DTY = 1), the area starting from the line set by this command and ending as set by the partial 2 display area line count register (R23) is the partial 2 display area.</p> |
| R22 | D ₇ to D ₀ | P1AW _n | <p>Partial1 display area line count register (00H to EFH)</p> <p>An area starting from the line set by the partial 1 display area start register (R20) and ending as set by this command is the partial 1 display area.</p> <p>If this register is 0, the values of the partial 2 display area start line register (R29) and the partial 2 display area line count register (R31) are not valid.</p> |
| R23 | D ₇ to D ₀ | P2AW _n | <p>Partial 2 display area line count register (00H to EFH)</p> <p>An area starting from the line set by the partial 2 display area start register (R21) and ending as set by this command is the partial 2 display area.</p> <p>If the partial 1 display area line count register is 0, the values of the partial 2 display area start line register (R21) and partial 2 display area line count register (R23) are not valid.</p> |
| R25 | D ₆ | BGRS | <p>This pin selects whether to use the internal power supply or an external power supply (input from the BGRIN pin) for generation the common center voltage output from the VCOM pin.</p> <p>0: The internal power supply is selected as the VCOM power supply 1: Input from the external power supply BGRIN is selected as the BCOM power supply</p> |
| | D ₅ | VCE | <p>Selects the V_O output level of the power supply IC (μ PD161660).</p> <p>The V_{CE} pin of the μ PD161623 and the V_{CE} pin of the power supply IC must be connected.</p> <p>0: The V_O high-level booster voltage level is V_{DD2} minus 1 level 1: The V_O high-level booster voltage level is the same level as V_{DD2}</p> |
| | D ₄ | VCD2 | <p>Selects the V_{DD2} output level of the power supply IC (μ PD161660).</p> <p>The V_{CD2} pin of the μ PD161623 and the V_{CD2} pin of the power supply IC must be connected.</p> <p>0: V_{DD2} = V_{CD} × 2 1: V_{DD2} = V_{CD} × 3</p> |
| | D ₃ | PVCOM | <p>Selects the voltage supplied to the VCOM output circuit.</p> <p>0: VCOM output circuit power supply, V_{DD2} 1: VCOM output circuit power supply, V_S</p> |

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| Register | Bit | Symbol | Function |
|----------|----------------------------------|--------|--|
| R25 | D ₁ | RGONP | Switches the internal DC/DC converter of the power supply IC (μ PD161660) ON/OFF. When OFF is selected, a low level is output from the RGONP pin, and when ON is selected, a high level is output from the RGONP pin. The RGONP pin of this IC and the RGONP pin of the power supply IC must be connected. 0: Regulators of power supply IC (V_T , V_S) are OFF 1: Regulators of power supply IC (V_T , V_S) are ON |
| | D ₀ | DCON | Switches the internal DC/DC converter of the power supply IC (μ PD161660) ON/OFF. When OFF is selected, a low level is output from the DCON pin, and when ON is selected, a high level is output from the DCON pin. The DCON pin of the μ PD161623 and the DCONP pin of the power supply IC must be connected. 0: DC/DC converter is OFF 1: DC/DC converter is ON |
| R26 | D ₁ | VCD12 | Performs booster control for the DC/DC converter in the power supply IC (μ PD161660) The data set with this bit is output from the VCD11 pin and the VCD12 pin. The VCD11 pin and VCD12 pin of the μ PD161623 must be connected to the VCD11 pin and the VCD12 pin of the power supply IC. |
| | D ₀ | VCD11 | VCD12, VCD11 = 0, 0: $V_{DD2} = V_{DC} \times 4$ = 0, 1: $V_{DD2} = V_{DC} \times 5$ = 1, 0: $V_{DD2} = V_{DC} \times 6$ = 1, 1: $V_{DD2} = V_{DC} \times 7$ |
| R29 | D ₇ to D ₀ | EVn | Sets the D/A converter circuit used to adjust the voltage of the reference voltage generator circuit (VBGR) input to the voltage regulator that sets the center value of the panel common drive output. The D/A converter divides the constant voltage generated by the reference voltage generator (VBGR) by 256, and one level can be selected between VBGR and V_{SS} by setting this command. For more detail, refer to 5.5 Common Adjustment Circuit and 5.8 D/A Converter Circuit . |
| R30 | D ₇ | BPL | Switched the capacity of the γ -correction circuit reference voltage generation amplifiers on the side not being used (VPH, VPL, VNH, VNL) to the minimum value based on the polarity inversion timing in order to reduce the current consumption. Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used. 0: Normal 1: Reference voltage generation amplifier capacity switch drive |
| | D ₆ to D ₄ | CIn | Sets the bias current of the amplifier for setting the panel's COMMON drive waveform center value (VCOM), as shown in the table below. Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used. |

| C12 | C11 | C10 | VCOM Center Value Setting Amplifier Bias Current Value |
|-----|-----|-----|--|
| 0 | 0 | 0 | 0.20 μ A |
| 0 | 0 | 1 | 0.50 μ A |
| 0 | 1 | 0 | 0.10 μ A |
| 0 | 1 | 1 | 0.05 μ A |
| 1 | 0 | 0 | 1.00 μ A |
| 1 | 0 | 1 | 1.50 μ A |
| 1 | 1 | 0 | 2.00 μ A |
| 1 | 1 | 1 | 3.00 μ A |

| Register | Bit | Symbol | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----------------------------------|--------|--|----------------------------------|-----|-----|----------------------------------|---|---|---|---------|---|---|---|---------|---|---|---|---------|---|---|---|---------|---|---|---|---------|---|---|---|---------|---|---|---|---------|---|---|---|---------|
| R30 | D ₃ | VCOMC | <p>Selects whether to use the amplifier for setting the panel's COMMON drive waveform center value (VCOM) or not.</p> <p>This amplifier can be used under conditions such as when an external COMMON drive circuit is being used.</p> <p>0: VCOM amplifier operating 1: VCOM amplifier stopped</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | D ₂ to D ₀ | SFn | <p>Sets the capacity of the source output (Y₁ to Y₅₂₆), as shown in the table below.</p> <p>Determine the output capacity after sufficient evaluation with the actual TFT panel to be used.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>SF2</th> <th>SF1</th> <th>SF0</th> <th>Source Output Bias Current Value</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0.20 μA</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0.15 μA</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0.25 μA</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0.10 μA</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0.20 μA</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0.30 μA</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0.40 μA</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0.05 μA</td></tr> </tbody> </table> | SF2 | SF1 | SF0 | Source Output Bias Current Value | 0 | 0 | 0 | 0.20 μA | 0 | 0 | 1 | 0.15 μA | 0 | 1 | 0 | 0.25 μA | 0 | 1 | 1 | 0.10 μA | 1 | 0 | 0 | 0.20 μA | 1 | 0 | 1 | 0.30 μA | 1 | 1 | 0 | 0.40 μA | 1 | 1 | 1 | 0.05 μA |
| | SF2 | SF1 | SF0 | Source Output Bias Current Value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0.20 μA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0.15 μA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0.25 μA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0.10 μA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0.20 μA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0.30 μA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 0.40 μA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 0.05 μA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R31 | D ₇ | WHP | <p>Sets the output mode of the reference voltage generator amplifier for setting the white level of the positive-polarity and negative-polarity sides (when VPL and VNL are normally white), as shown below.</p> <p>Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.</p> <p>0: Normal mode 1: High-power mode (output stage capacity: twice that of normal mode)</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | D ₆ to D ₄ | WIn | <p>Sets the output bias current of the reference voltage generator amplifier for setting the white level of the positive-polarity and negative-polarity sides (when VPL and VNL are normally white), as shown below.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>WI2</th> <th>WI1</th> <th>WI0</th> <th>Amplifier Bias Current</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0.20 μA</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0.50 μA</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0.10 μA</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0.05 μA</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1.00 μA</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1.50 μA</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>2.00 μA</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>3.00 μA</td></tr> </tbody> </table> | WI2 | WI1 | WI0 | Amplifier Bias Current | 0 | 0 | 0 | 0.20 μA | 0 | 0 | 1 | 0.50 μA | 0 | 1 | 0 | 0.10 μA | 0 | 1 | 1 | 0.05 μA | 1 | 0 | 0 | 1.00 μA | 1 | 0 | 1 | 1.50 μA | 1 | 1 | 0 | 2.00 μA | 1 | 1 | 1 | 3.00 μA |
| WI2 | WI1 | WI0 | Amplifier Bias Current | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0.20 μA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0.50 μA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0.10 μA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0.05 μA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1.00 μA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1.50 μA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 2.00 μA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 3.00 μA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | D ₃ | BHP | <p>Sets the output mode of the reference voltage generator amplifier for setting the black level of the positive-polarity and negative-polarity sides (when VPH and VNH are normally white), as shown below.</p> <p>Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.</p> <p>0: Normal mode 1: High-power mode (output stage capacity: twice that of normal mode)</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

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| Register | Bit | Symbol | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------------|----------------------------------|--|---|-----------------|-------|-------|------------------------|-----------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|---|---|---|--------------|---|---|---|--------------|---|---|---|--------------|---|---|---|--------------|
| R31 | D ₂ to D ₀ | BI _n | <p>Sets the output bias current of the reference voltage generator amplifier for setting the black level of the positive-polarity and negative-polarity sides (when VPH and VNH are normally white), as shown below.</p> <p>Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BI2</th> <th>BI1</th> <th>BI0</th> <th>Amplifier Bias Current</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0.20 μA</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0.50 μA</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0.10 μA</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0.05 μA</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1.00 μA</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1.50 μA</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>2.00 μA</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>3.00 μA</td> </tr> </tbody> </table> | BI2 | BI1 | BI0 | Amplifier Bias Current | 0 | 0 | 0 | 0.20 μ A | 0 | 0 | 1 | 0.50 μ A | 0 | 1 | 0 | 0.10 μ A | 0 | 1 | 1 | 0.05 μ A | 1 | 0 | 0 | 1.00 μ A | 1 | 0 | 1 | 1.50 μ A | 1 | 1 | 0 | 2.00 μ A | 1 | 1 | 1 | 3.00 μ A |
| BI2 | BI1 | BI0 | Amplifier Bias Current | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0.20 μ A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0.50 μ A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0.10 μ A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0.05 μ A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1.00 μ A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1.50 μ A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 2.00 μ A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 3.00 μ A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R36 | D ₇ to D ₀ | GPH _n | <p>Sets the voltage value of the black level of positive polarity.</p> <p>For more detail, refer to 5.9 γ-Curve Correction Power Supply Circuit.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R37 | D ₇ to D ₀ | GNH _n | <p>Sets the voltage value of the white level of negative polarity.</p> <p>For more detail, refer to 5.9 γ-Curve Correction Power Supply Circuit.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R38 | D ₇ to D ₀ | GPL _n | <p>Sets the voltage value of the white level of positive polarity.</p> <p>For more detail, refer to 5.9 γ-Curve Correction Power Supply Circuit.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R39 | D ₇ to D ₀ | GNL _n | <p>Sets the voltage value of the white level of positive polarity.</p> <p>For more detail, refer to 5.9 γ-Curve Correction Power Supply Circuit.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R40 | D ₇ to D ₄ | RDTP _n | <p>Sets the data value at which the pre-charge direction is switched during positive-polarity drive. The value set to RDTP_n corresponds to the higher 4bits of display RAM data DB_n (6 bits for each of RFB), as shown below.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th>RDTP3</th> <th>RDTP2</th> <th>RDTP1</th> <th>RDTP0</th> </tr> </thead> <tbody> <tr> <td>Dot 1 (R)</td> <td>D₁₇</td> <td>D₁₆</td> <td>D₁₅</td> <td>D₁₄</td> </tr> <tr> <td>Dot 2 (G)</td> <td>D₁₁</td> <td>D₁₀</td> <td>D₉</td> <td>D₈</td> </tr> <tr> <td>Dot 3 (B)</td> <td>D₅</td> <td>D₄</td> <td>D₃</td> <td>D₂</td> </tr> </tbody> </table> | | RDTP3 | RDTP2 | RDTP1 | RDTP0 | Dot 1 (R) | D ₁₇ | D ₁₆ | D ₁₅ | D ₁₄ | Dot 2 (G) | D ₁₁ | D ₁₀ | D ₉ | D ₈ | Dot 3 (B) | D ₅ | D ₄ | D ₃ | D ₂ | | | | | | | | | | | | | | | | |
| | | RDTP3 | RDTP2 | RDTP1 | RDTP0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Dot 1 (R) | D ₁₇ | D ₁₆ | D ₁₅ | D ₁₄ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Dot 2 (G) | D ₁₁ | D ₁₀ | D ₉ | D ₈ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Dot 3 (B) | D ₅ | D ₄ | D ₃ | D ₂ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D ₃ to D ₀ | RDTN _n | <p>Sets the data value at which the pre-charge direction is switched during negative-polarity drive. The value set to RDTN_n corresponds to the higher 4 bits of display RAM data DB_n (6 bits for each of RGB), as shown below.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th>RDTN3</th> <th>RDTN2</th> <th>RDTN1</th> <th>RDTN0</th> </tr> </thead> <tbody> <tr> <td>Dot 1 (R)</td> <td>D₁₇</td> <td>D₁₆</td> <td>D₁₅</td> <td>D₁₄</td> </tr> <tr> <td>Dot 2 (G)</td> <td>D₁₁</td> <td>D₁₀</td> <td>D₉</td> <td>D₈</td> </tr> <tr> <td>Dot 3 (B)</td> <td>D₅</td> <td>D₄</td> <td>D₃</td> <td>D₂</td> </tr> </tbody> </table> | | RDTN3 | RDTN2 | RDTN1 | RDTN0 | Dot 1 (R) | D ₁₇ | D ₁₆ | D ₁₅ | D ₁₄ | Dot 2 (G) | D ₁₁ | D ₁₀ | D ₉ | D ₈ | Dot 3 (B) | D ₅ | D ₄ | D ₃ | D ₂ | | | | | | | | | | | | | | | | | |
| | RDTN3 | RDTN2 | RDTN1 | RDTN0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Dot 1 (R) | D ₁₇ | D ₁₆ | D ₁₅ | D ₁₄ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Dot 2 (G) | D ₁₁ | D ₁₀ | D ₉ | D ₈ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Dot 3 (B) | D ₅ | D ₄ | D ₃ | D ₂ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R42 | D ₀ | GHSW | <p>Controls the γ-correction voltage input pins (V₀ to V₅) and the switch for connecting the μPD161623 internal γ-correction resistor.</p> <p>0: Switch OFF (disconnected) 1: Switch ON (connected)</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R45 | D ₀ | OC | <p>This bit is used for calibration.</p> <p>The time from calibration start command execution until calibration stop command execution becomes the time for 1 line.</p> <p>0: Calibration stop 1: Calibration start</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Register | Bit | Symbol | Function | | | | |
|----------|----------------------------------|--------|--|-------|-------|---|---|
| R46 | D ₆ to D ₀ | PLIMn | Sets the clock count for the pre-charge period. The value written to this register is set as the clock count (1/f _{ocs}) of the pre-charge period. For details, refer to 5.4.1 Display timing | | | | |
| R49 | D ₇ to D ₀ | OPn | Output port (OP ₇ to OP ₀) write When after the output port register is specified in the index register, writing to the output port register is performed, the values written to the OP ₇ to OP ₀ pins are output. | | | | |
| ★ R114 | D ₁ , D ₀ | RTSCn | <p>Selects the optimum internal circuit operation based on the operating voltage of the interface circuits. To set by this register, we recommend as follow setting.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>RTSC1</td> <td>RTSC0</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> </table> <p>Caution Always set this register and internal logic operating voltage setting register (R115) to the same value.</p> | RTSC1 | RTSC0 | 0 | 1 |
| RTSC1 | RTSC0 | | | | | | |
| 0 | 1 | | | | | | |
| ★ R115 | D ₁ , D ₀ | RTSLn | <p>Selects the optimum internal circuit operation based on the operating voltage of the internal logic circuits. To set by this register, we recommend as follow setting.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>RTSC1</td> <td>RTSC0</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> </table> <p>Caution Always set this register and interface operating voltage setting register (R114) to the same value.</p> | RTSC1 | RTSC0 | 0 | 1 |
| RTSC1 | RTSC0 | | | | | | |
| 0 | 1 | | | | | | |

8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

| Parameter | Symbol | Ratings | Unit |
|---|----------------------------------|--------------------------------|------|
| Power supply voltage | V _S | -0.5 to +6.5 | V |
| Power supply voltage | V _{DD1} | -0.5 to V _{DD2} + 0.5 | V |
| Power supply voltage | V _{DD2} | -0.5 to +4.0 | V |
| Power supply voltage for γ -curve correction | V ₀ to V ₅ | -0.5 to V _S + 0.5 | V |
| Input voltage | V _I | -0.5 to V _{DD2} + 0.5 | V |
| Input current | I _I | ±10 | mA |
| Operating ambient temperature | T _A | -40 to +85 | °C |
| Storage temperature | T _{stg} | -55 to +125 | °C |

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = -40 to +85°C, V_{SS} = 0 V)

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit |
|----------------------|------------------------------|------|------|------------------|------|
| Power supply voltage | V _S | 4.3 | 5.0 | 5.5 | V |
| | V _{DD1} | 1.7 | 1.8 | V _{DD2} | V |
| | V _{DD2} | 2.5 | 2.7 | 3.6 | V |
| Input voltage | V _{I1} Note1 | 0 | | V _{DD2} | V |
| | V _{I2} Note2 | 0 | | V _{DD1} | V |

Notes 1. Pins of V_{DD1} power supply system: PSX, C86, TOUT0 to TOUT17, OP0 to OP7, LPMP, GOE1, GOE2, GSTB, GCLK, DCON, RGONP, VCD11, VCD12, VCD2, VCE, OSCSEL, TESTIN, TSTRST, TSTVIHL, TOSCI

2. Pins of V_{DD2} power supply system: /CS, /RD (E), /WR (R,/W), D0 to D17, RS, /RESET, OSCIN

Electrical Specifications (Unless Otherwise Specified, $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD1} = 1.7$ V to V_{DD2} , $V_{DD2} = 2.5$ to 3.6 V, $V_S = 4.3$ to 5.5 V)

| Parameter | Symbol | Condition | Specification | | | Unit | |
|--|------------------|---|-----------------|-----------------------|-----------------|---------------|---------------|
| | | | MIN. | TYP. ^{Note1} | MAX. | | |
| High level input voltage | V_{IH1} | V_{DD2} | $0.8 V_{DD2}$ | | | V | |
| | V_{IH2} | V_{DD1} | $0.8 V_{DD1}$ | | | V | |
| Low level input voltage | V_{IL1} | V_{DD2} | | | $0.2 V_{DD2}$ | V | |
| | V_{IL2} | V_{DD1} | | | $0.2 V_{DD1}$ | V | |
| High level output voltage | V_{OH1} | V_{DD2} , $I_{OUT} = -100 \mu\text{A}$ | $0.9 V_{DD2}$ | | | V | |
| | V_{OH2} | V_{DD1} , $I_{OUT} = -1 \text{ mA}$ | $0.8 V_{DD1}$ | | | V | |
| | V_{OH3} | V_{COU1} , V_{COU2} , $I_{OUT} = -100 \mu\text{A}$ | 0.9 V | | | V | |
| Low level output voltage | V_{OL1} | V_{DD2} , $I_{OUT} = 100 \mu\text{A}$ | | | $0.1 V_{DD2}$ | V | |
| | V_{OL2} | V_{DD1} , $I_{OUT} = 1 \text{ mA}$ | | | $0.2 V_{DD1}$ | V | |
| | V_{OL3} | V_{COU1} , V_{COU2} , $I_{OUT} = 100 \mu\text{A}$ | | | $0.1 V_S$ | V | |
| VCOM output voltage | V_{COMH} | $I_{SOURCE} = 100 \mu\text{A}$ | $V_{COM} - 0.3$ | | | V | |
| | V_{COML} | $I_{SINK} = -100 \mu\text{A}$ | | | $V_{COM} - 0.3$ | V | |
| High level input current | I_{IH1} | Except D_0 to D_{17} | | | 1 | μA | |
| Low level input current | I_{IL1} | Except D_0 to D_{17} | | | -1 | μA | |
| High level leakage current | I_{LIH} | D_0 to D_{17} | | | 10 | μA | |
| Low level leakage current | I_{LIL} | D_0 to D_{17} | | | -10 | μA | |
| High level driver output current | I_{VOH} | $V_X = 3.5 \text{ V}$, $V_{OUT} = 4.5 \text{ V}$, $V_S = 5.0 \text{ V}$ ^{Note2} | | | -100 | μA | |
| Low level driver output current | I_{VOL} | $V_X = 2.0 \text{ V}$, $V_{OUT} = 1.0 \text{ V}$, $V_S = 5.0 \text{ V}$ ^{Note2} | 150 | | | μA | |
| VCOM common output voltage fluctuation parameter | ΔV_{COM} | | -10 | | 10 | % | |
| Current consumption | I_{DD1} | V_{DD1} (when non-access CPU) | | 0.1 | 2 | μA | |
| | I_{DD2} | V_{DD2} (when non-access CPU) | | 200 | 350 | μA | |
| | I_{STBY} | Stand-by mode, V_{DD2} pin | | 0.1 | 10 | μA | |
| | I_S | 260,000-color mode ^{Note3} | | | 650 | 1250 | μA |
| | | 8-color mode ^{Note3} | | | 50 | 200 | μA |
| Driver output Current (pre-charge) | I_{VOH} | $V_{OUT} = V_S - 0.1 \text{ V}$, $V_S = 5.0 \text{ V}$ ^{Note2} | | | -5 | μA | |
| | I_{VOL} | $V_{OUT} = V_{SS} + 0.1 \text{ V}$, $V_S = 5.0 \text{ V}$ ^{Note2} | 2 | | | μA | |
| Output voltage deviation | ΔV_{O1} | $V_O = 1.3 \text{ V}$ to $V_S - 1.3 \text{ V}$ | -20 | | +20 | mV | |
| | ΔV_{O2} | $V_O = 0.3$ to 1.3 V $V_O = V_S - 1.3 \text{ V}$ to $V_S - 0.3 \text{ V}$ | -30 | | +20 | mV | |
| Output voltage period | V_O | Input data: H to H | $V_{SS} + 0.2$ | | $V_S - 0.2$ | V | |

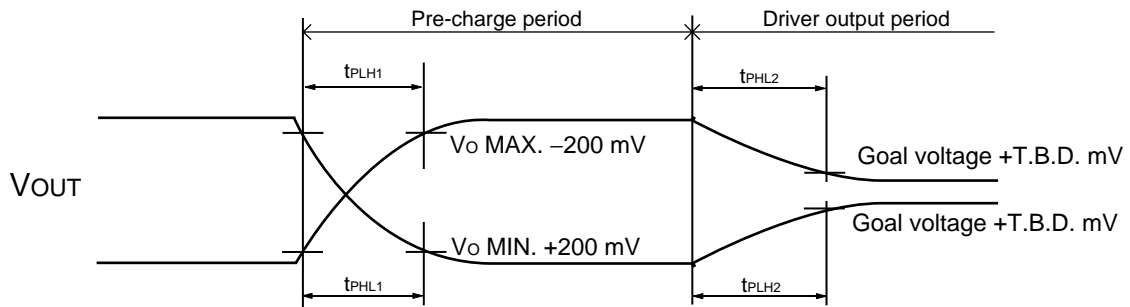
Notes 1. TYP. values are reference values when $T_A = 25^\circ\text{C}$

2. V_X refers to the output voltage of analog output pins Y_1 to Y_{528} .

V_{OUT} refers to the voltage applied to analog output pins Y_1 to Y_{528} .

★ **3.** Frame frequency: 60 Hz, line inversion mode select, dot checkerboard input pattern, no load.

Switching characteristics (Unless Otherwise Specified, $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD1} = 1.7\text{ V}$ to V_{DD2} ,
 $V_{DD2} = 2.5$ to 3.6 V , $V_s = 4.3$ to 5.5 V)

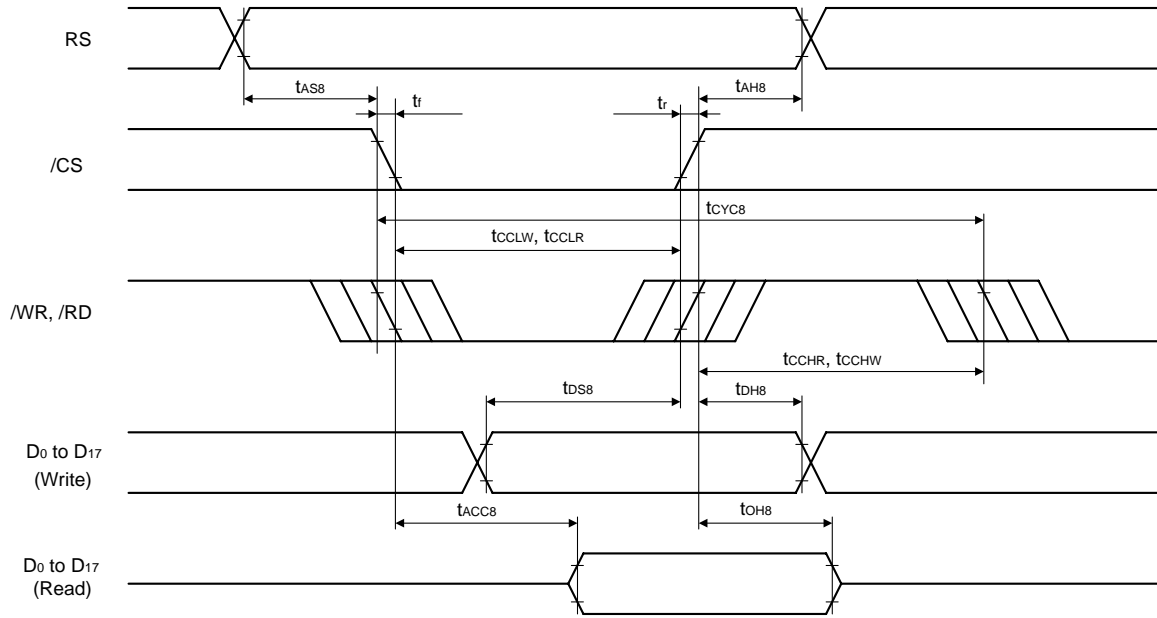


| Parameter | Symbol | Condition | MIN. | TYP. ^{Note} | MAX. | Unit | |
|--|------------|---|------------------------------------|----------------------|------|------|---------------|
| Driver output delay time 1 (pre-charge period) | t_{PLH1} | $V_s = 5.0\text{ V}$, $4\text{ k}\Omega + 27\text{ pF}$ | $V_O \text{ MAX. } -200\text{ mV}$ | | | 7.0 | μs |
| | t_{PHL1} | | $V_O \text{ MIN. } +200\text{ mV}$ | | | 9.5 | μs |
| Driver output delay time 2 (driver output period) | t_{PLH2} | Pre-charge completed → goal voltage | | | | 50 | μs |
| | t_{PHL2} | | | | | 52 | μs |

Note TYP. values are reference values when $T_A = 25^\circ\text{C}$.

AC Characteristics (Unless Otherwise Specified, $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD1} = 1.7$ V to V_{DD2} , $V_{DD2} = 2.5$ to 3.6 V, $V_S = 4.3$ to 5.5 V)

(a) i80 series CPU interface



When V_{DD1} = 2.5 to 3.6 V, V_{DD2} = 2.5 to 3.6 V, V_{DD2} ≥ V_{DD1} (normal write mode, R114 = R115 = 01H)

| Parameter | Symbol | Condition | MIN. | TYP. ^{Note} | MAX. | Unit |
|--------------------------------------|-------------------|---|------|----------------------|------|------|
| Address hold time | t _{AH8} | RS | 0 | | | ns |
| Address setup time | t _{AS8} | RS | 0 | | | ns |
| System cycle time | t _{CYC8} | | 250 | | | ns |
| Control low-level pulse width (/WR) | t _{CCLW} | /WR | 120 | | | ns |
| Control low-level pulse width (/RD) | t _{CCLR} | /RD | 140 | | | ns |
| Control high-level pulse width (/WR) | t _{CCHW} | /WR | 60 | | | ns |
| Control high-level pulse width (/RD) | t _{CCHR} | /RD | 80 | | | ns |
| Data setup time | t _{DS8} | D ₀ to D ₁₇ | 80 | | | ns |
| Data hold time | t _{DH8} | D ₀ to D ₁₇ | 0 | | | ns |
| /RD access time | t _{ACC8} | D ₀ to D ₁₇ , C _L = 100 pF | | | 110 | ns |
| Output disable time | t _{OH8} | D ₀ to D ₁₇ , C _L = 100 pF | 10 | | 100 | ns |

Note TYP. values are reference values when T_A = 25°C.

- Remarks 1.** The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.
2. All timing is rated based on 20 to 80% of V_{DD1}.

When V_{DD1} = 1.7 to 2.5 V, V_{DD2} = 2.5 to 3.6 V, V_{DD2} ≥ V_{DD1} (normal write mode, R114 = R115 = 01H)

| Parameter | Symbol | Condition | MIN. | TYP. ^{Note} | MAX. | Unit |
|--------------------------------------|-------------------|---|------|----------------------|------|------|
| Address hold time | t _{AH8} | RS | 0 | | | ns |
| Address setup time | t _{AS8} | RS | 0 | | | ns |
| System cycle time | t _{CYC8} | | 333 | | | ns |
| Control low-level pulse width (/WR) | t _{CCLW} | /WR | 120 | | | ns |
| Control low-level pulse width (/RD) | t _{CCLR} | /RD | 160 | | | ns |
| Control high-level pulse width (/WR) | t _{CCHW} | /WR | 100 | | | ns |
| Control high-level pulse width (/RD) | t _{CCHR} | /RD | 140 | | | ns |
| Data setup time | t _{DS8} | D ₀ to D ₁₇ | 100 | | | ns |
| Data hold time | t _{DH8} | D ₀ to D ₁₇ | 0 | | | ns |
| /RD access time | t _{ACC8} | D ₀ to D ₁₇ , C _L = 100 pF | | | 150 | ns |
| Output disable time | t _{OH8} | D ₀ to D ₁₇ , C _L = 100 pF | 10 | | 150 | ns |

Note TYP. values are reference values when T_A = 25°C.

- Remarks 1.** The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.
2. All timing is rated based on 20 to 80% of V_{DD1}.

When $V_{DD1} = 2.5$ to 3.6 V, $V_{DD2} = 2.5$ to 3.6 V, $V_{DD2} \geq V_{DD1}$ (high-speed RAM write mode, valid only for writing data, R114 = R115 = 01H)

| Parameter | Symbol | Condition | MIN. | TYP. ^{Note} | MAX. | Unit |
|--------------------------------------|------------|-----------------------------------|------|----------------------|------|------|
| Address hold time | t_{AH8} | RS | 0 | | | ns |
| Address setup time | t_{AS8} | RS | 0 | | | ns |
| System cycle time | t_{CYC8} | | 125 | | | ns |
| Control low-level pulse width (/WR) | t_{CCLW} | /WR | 60 | | | ns |
| Control high-level pulse width (/WR) | t_{CCHW} | /WR | 30 | | | ns |
| Data setup time | t_{DS8} | D ₀ to D ₁₇ | 80 | | | ns |
| Data hold time | t_{DH8} | D ₀ to D ₁₇ | 0 | | | ns |

Note TYP. values are reference values when $T_A = 25^\circ\text{C}$.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{DD1} .

When $V_{DD1} = 1.7$ to 2.5 V, $V_{DD2} = 2.5$ to 3.6 V, $V_{DD2} \geq V_{DD1}$, (high-speed RAM write mode, valid only for writing data, R114 = R115 = 01H)

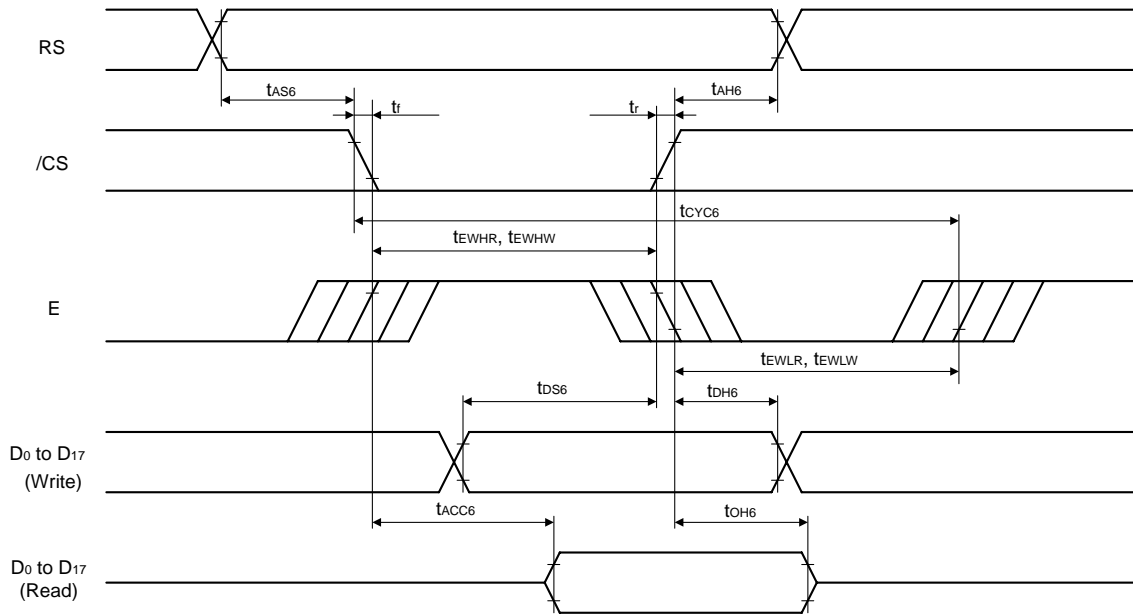
| Parameter | Symbol | Condition | MIN. | TYP. ^{Note} | MAX. | Unit |
|--------------------------------------|------------|-----------------------------------|------|----------------------|------|------|
| Address hold time | t_{AH8} | RS | 0 | | | ns |
| Address setup time | t_{AS8} | RS | 0 | | | ns |
| System cycle time | t_{CYC8} | | 167 | | | ns |
| Control low-level pulse width (/WR) | t_{CCLW} | /WR | 60 | | | ns |
| Control high-level pulse width (/WR) | t_{CCHW} | /WR | 50 | | | ns |
| Data setup time | t_{DS8} | D ₀ to D ₁₇ | 100 | | | ns |
| Data hold time | t_{DH8} | D ₀ to D ₁₇ | 0 | | | ns |

Note TYP. values are reference values when $T_A = 25^\circ\text{C}$.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{DD1} .

(b) M68 series CPU interface



When V_{DD1} = 2.5 to 3.6 V, V_{DD2} = 2.5 to 3.6 V, V_{DD2} ≥ V_{DD1} (normal mode, R114 = R115 = 01H)

| Parameter | Symbol | Condition | MIN. | TYP. ^{Note} | MAX. | Unit |
|-------------------------|-------------------|---|------|----------------------|------|------|
| Address hold time | t _{AH6} | RS | 0 | | | ns |
| Address setup time | t _{AS6} | RS | 0 | | | ns |
| System cycle time | t _{CYC6} | | 250 | | | ns |
| Data setup time | t _{DS6} | D ₀ to D ₁₇ | 80 | | | ns |
| Data hold time | t _{DH6} | D ₀ to D ₁₇ | 0 | | | ns |
| Access time | t _{ACC6} | D ₀ to D ₁₇ , C _L = 100 pF | | | 110 | ns |
| Output disable time | t _{OH6} | D ₀ to D ₁₇ , C _L = 100 pF | 10 | | 100 | ns |
| Enable high pulse width | Read | t _{EWHR} | E | 140 | | ns |
| | Write | t _{EWHW} | E | 120 | | ns |
| Enable low pulse width | Read | t _{EWLR} | E | 80 | | ns |
| | Write | t _{EWLW} | E | 60 | | ns |

Note TYP. values are reference values when T_A = 25°C.

- Remarks 1.** The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either (t_r + t_f) < (t_{CYC6} - t_{EWLR} - t_{EWHR}) or (t_r + t_f) < (t_{CYC6} - t_{EWLW} - t_{EWHW}).
- 2.** All timing is rated based on 20 to 80% of V_{DD1}.

When V_{DD1} = 1.7 to 2.5 V, V_{DD2} = 2.5 to 3.6 V, V_{DD2} ≥ V_{DD1} (normal mode, R114 = R115 = 01H)

| Parameter | Symbol | Condition | MIN. | TYP. ^{Note} | MAX. | Unit |
|-------------------------|-------------------|---|------|----------------------|------|------|
| Address hold time | t _{AH6} | RS | 0 | | | ns |
| Address setup time | t _{AS6} | RS | 0 | | | ns |
| System cycle time | t _{CYC6} | | 333 | | | ns |
| Data setup time | t _{DS6} | D ₀ to D ₁₇ | 100 | | | ns |
| Data hold time | t _{DH6} | D ₀ to D ₁₇ | 0 | | | ns |
| Access time | t _{ACC6} | D ₀ to D ₁₇ , C _L = 100 pF | | | 150 | ns |
| Output disable time | t _{OH6} | D ₀ to D ₁₇ , C _L = 100 pF | 10 | | 150 | ns |
| Enable high pulse width | Read | t _{EWHR} | E | 160 | | ns |
| | Write | t _{EWHW} | E | 160 | | ns |
| Enable low pulse width | Read | t _{EWLR} | E | 140 | | ns |
| | Write | t _{EWLW} | E | 100 | | ns |

Note TYP. values are reference values when T_A = 25°C.

- Remarks 1.** The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either (t_r + t_f) < (t_{CYC6} - t_{EWLR} - t_{EWHR}) or (t_r + t_f) < (t_{CYC6} - t_{EWLW} - t_{EWHW}).
- 2.** All timing is rated based on 20 to 80% of V_{DD1}.

When $V_{DD1} = 2.5$ to 3.6 V, $V_{DD2} = 2.5$ to 3.6 V, $V_{DD2} \geq V_{DD1}$ (high-speed RAM write mode, valid only for writing data, R114 = R115 = 01H)

| Parameter | Symbol | Condition | MIN. | TYP. ^{Note} | MAX. | Unit |
|-------------------------|------------|-----------------------------------|------|----------------------|------|------|
| Address hold time | t_{AH6} | RS | 0 | | | ns |
| Address setup time | t_{AS6} | RS | 0 | | | ns |
| System cycle time | t_{CYC6} | | 125 | | | ns |
| Data setup time | t_{DS6} | D ₀ to D ₁₇ | 80 | | | ns |
| Data hold time | t_{DH6} | D ₀ to D ₁₇ | 0 | | | ns |
| Enable high pulse width | t_{EWHR} | E | 60 | | | ns |
| Enable low pulse width | t_{EWLR} | E | 30 | | | ns |

Note TYP. values are reference values when $T_A = 25^\circ\text{C}$.

- Remarks 1.** The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either $(t_r + t_f) < (t_{CYC6} - t_{EWLR} - t_{EWHR})$ or $(t_r + t_f) < (t_{CYC6} - t_{EWLW} - t_{EWHW})$.
- 2.** All timing is rated based on 20 to 80% of V_{DD1} .

When $V_{DD1} = 1.7$ to 2.5 V, $V_{DD2} = 2.5$ to 3.6 V, $V_{DD2} \geq V_{DD1}$ (high-speed RAM write mode, valid only for writing data, R114 = R115 = 01H)

| Parameter | Symbol | Condition | MIN. | TYP. ^{Note} | MAX. | Unit |
|-------------------------|------------|-----------------------------------|------|----------------------|------|------|
| Address hold time | t_{AH6} | RS | 0 | | | ns |
| Address setup time | t_{AS6} | RS | 0 | | | ns |
| System cycle time | t_{CYC6} | | 167 | | | ns |
| Data setup time | t_{DS6} | D ₀ to D ₁₇ | 100 | | | ns |
| Data hold time | t_{DH6} | D ₀ to D ₁₇ | 0 | | | ns |
| Enable high pulse width | t_{EWHR} | E | 60 | | | ns |
| Enable low pulse width | t_{EWLR} | E | 50 | | | ns |

Note TYP. values are reference values when $T_A = 25^\circ\text{C}$.

- Remarks 1.** The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either $(t_r + t_f) < (t_{CYC6} - t_{EWLR} - t_{EWHR})$ or $(t_r + t_f) < (t_{CYC6} - t_{EWLW} - t_{EWHW})$.
- 2.** All timing is rated based on 20 to 80% of V_{DD1} .

(c) Common

| Parameter | Symbol | Condition | MIN. | TYP. ^{Note1} | MAX. | Unit |
|---|--|--|-----------------|------------------------|-----------------|-----------------|
| Oscillation frequency | f _{OSC1} | Internal oscillator, 240 line (NGO = 0) | 370 | 535 | 850 | kHz |
| | f _{OSC2} | Internal oscillator, 220 line (NGO = 1) | 300 | 490 | 760 | kHz |
| | f _{OSC3} | External oscillator, 240 line (NGO = 0), resistance for oscillator R _L = 42 k Ω | | 536.2 ^{Note5} | | kHz |
| ★ Calibration setting time (frame frequency) | t _{cal1} (f _{FRAME01}) | Internal oscillator, 240 line (NGO = 0), Note2 | 29.7 (139.6) | 69.1 (60) | 162.4 (25.6) | μ s (Hz) |
| | t _{cal2} (f _{FRAME02}) | Internal oscillator, 220 line (NGO = 1), Note2 | 36.7 (123.4) | 69.1 (60) | 181.6 (24.9) | μ s (Hz) |
| | Frame frequency | f _{FRAME1} | Uncalibrated | 40 | 60 | 95 |
| f _{FRAME2} | | Calibrated ^{Note3} | 54 | 60 | 66 | Hz |
| f _{FRAME3} | | Calibrated ^{Note4} | 56 | 60 | 64 | Hz |
| Input oscillation frequency | f _{OSCIN1} | External oscillator, 240 line (NGO = 0) | | 535 | | kHz |
| | f _{OSCIN2} | External oscillator, 220 line (NGO = 1) | | 490 | | kHz |
| Reset pulse width at power on | t _{VR} | V _{DD2} OR V _{DD1} TO /RESET \uparrow | 100 | | | ns |
| Reset pulse width | t _{RW} | | 100 | | | ns |
| Reset time | t _R | /RESET \uparrow to interface operation | 100 | | | ns |

Notes 1. TYP. values are reference values when T_A = 25°C.

★ 2. The relationship between the frame frequency and the calibration setting time is as follows.

$$f_{FRAME01} = \frac{1}{t_{cal} \times 241} \quad f_{FRAME02} = \frac{1}{t_{cal} \times 221}$$

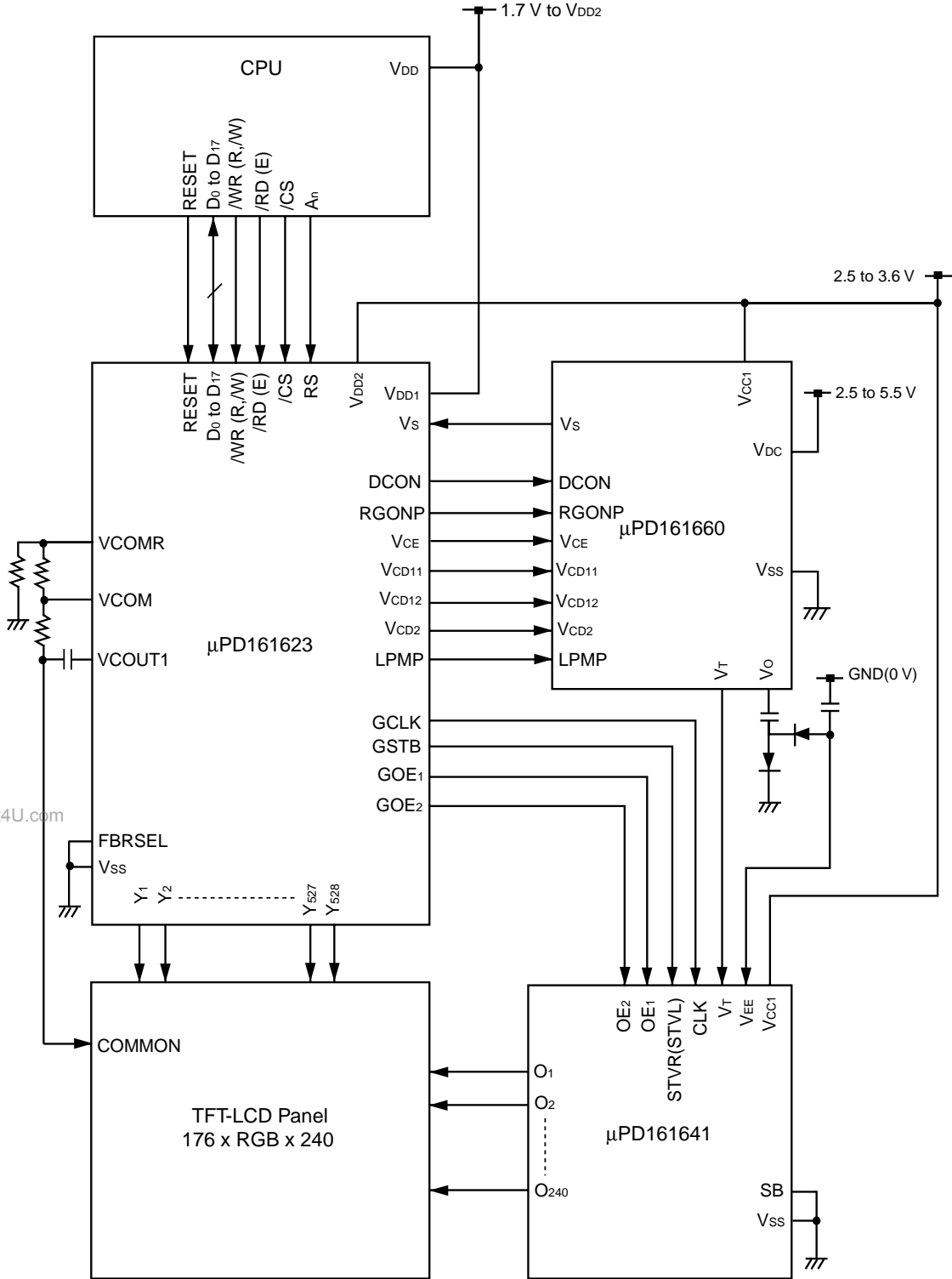
3. Measured at T_A = -40 to +85°C, after calibration at frame frequency = 60 Hz, T_A = 25°C exactly.

4. Measured at $\pm 5^\circ\text{C}$, after calibration at frame frequency = 60 Hz exactly.

5. This value is a reference value in some measurement conditions. Note that be able to use and obtain after a real board's fully estimating.

9. μPD161623, 161641, and 161660 CONNECTION DIAGRAM EXAMPLE

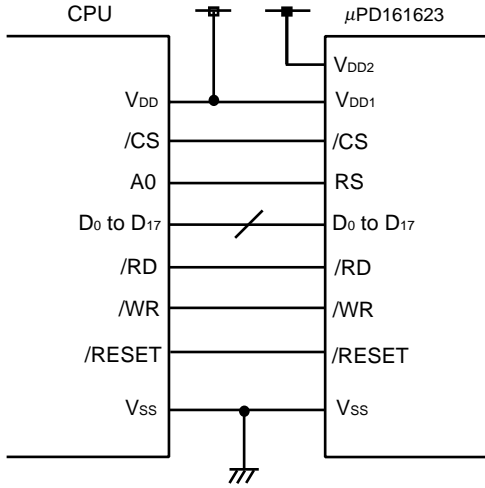
Connection diagram examples for the μPD161623, 161641, and 161660 are shown below.



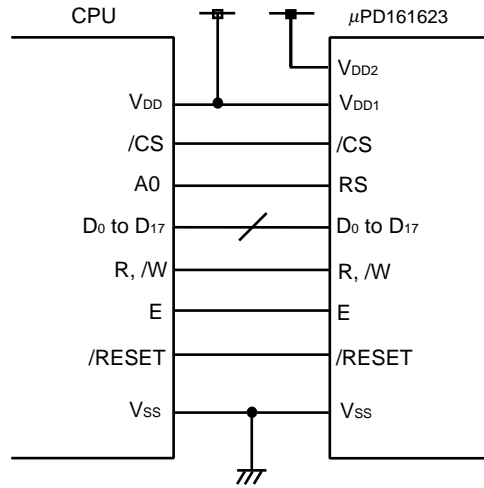
10. EXAMPLE of μ PD161623 and CPU CONNECTION

Examples of μ PD161623 and CPU connection are shown below. In the example below, RS pin control in parallel interface mode is described for the case when the least significant bit of the address bus is being used.

(1) i80 series format



(2) M68 series format



NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.