NEC

MOS INTEGRATED CIRCUIT

μPD16306A

64-BIT HIGH-VOLTAGE CMOS DRIVER

The μPD16306A is a high-voltage CMOS driver for flat display panels such as FIPs and ELs. It consists of a 64-bit bidirectional shift register, a 64-bit latch, and a high-voltage CMOS driver. The logic operates on 5 V (CMOS level input) so that it can be directly connected to a microcomputer. The drivers can output a voltage as high as 80 V at 25 mA$_{MAX.}$ Because both the logic and drivers are created by CMOS process, they dissipate only a tiny amount of power.

FEATURES

- 64-bit bidirectional shift driver
- Data control through transfer lock (external) and latch
- High-speed data transfer ($f_{max.}$ = 16 MHz$_{MIN.}$, in cascade connection)
- Wide operating temperature range ($T_{A.}$ = –40 to 85 °C)
- High-voltage output (80 V, 25 mA$_{MAX.}$)
- High-voltage CMOS process
- Polarities of all drivers can be reversed by using $\overline{PC}$ pin.

ORDERING INFORMATION

Part Number	Package
μPD16306AGF-3BA	100-pin plastic QFP (Iron lead frame: PD = 1.0 W)
μPD16306AGF-3RA	100-pin plastic QFP (Copper lead frame: PD = 1.3 W)

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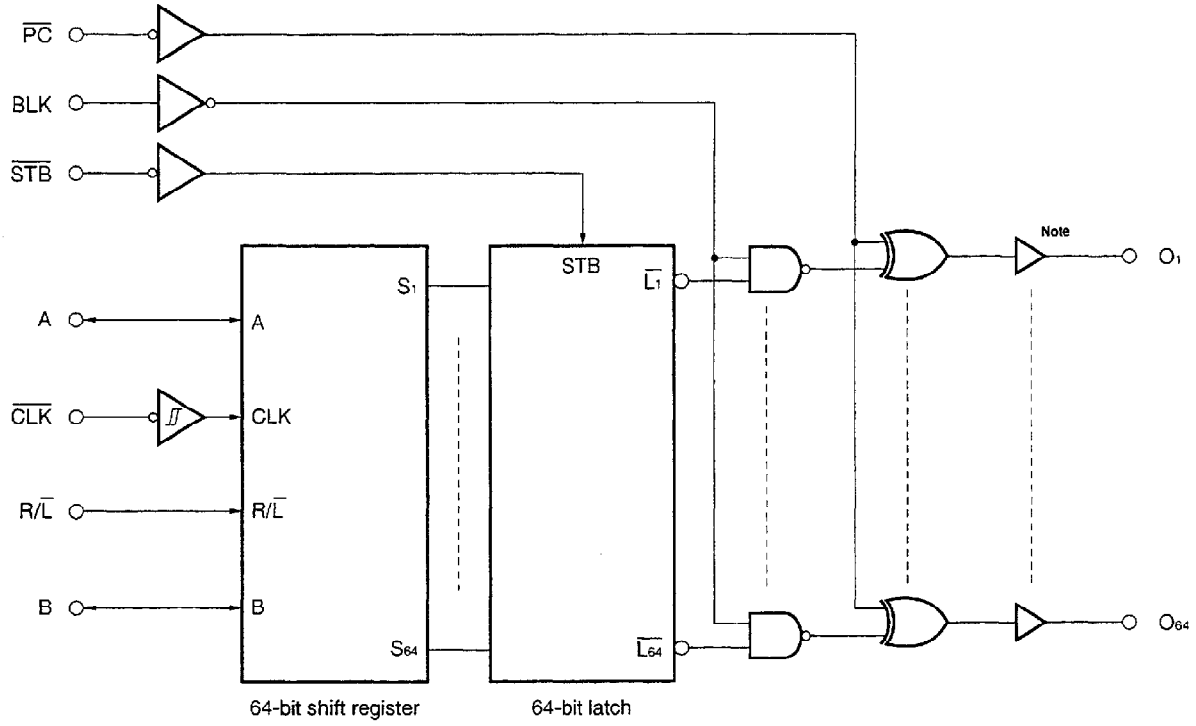
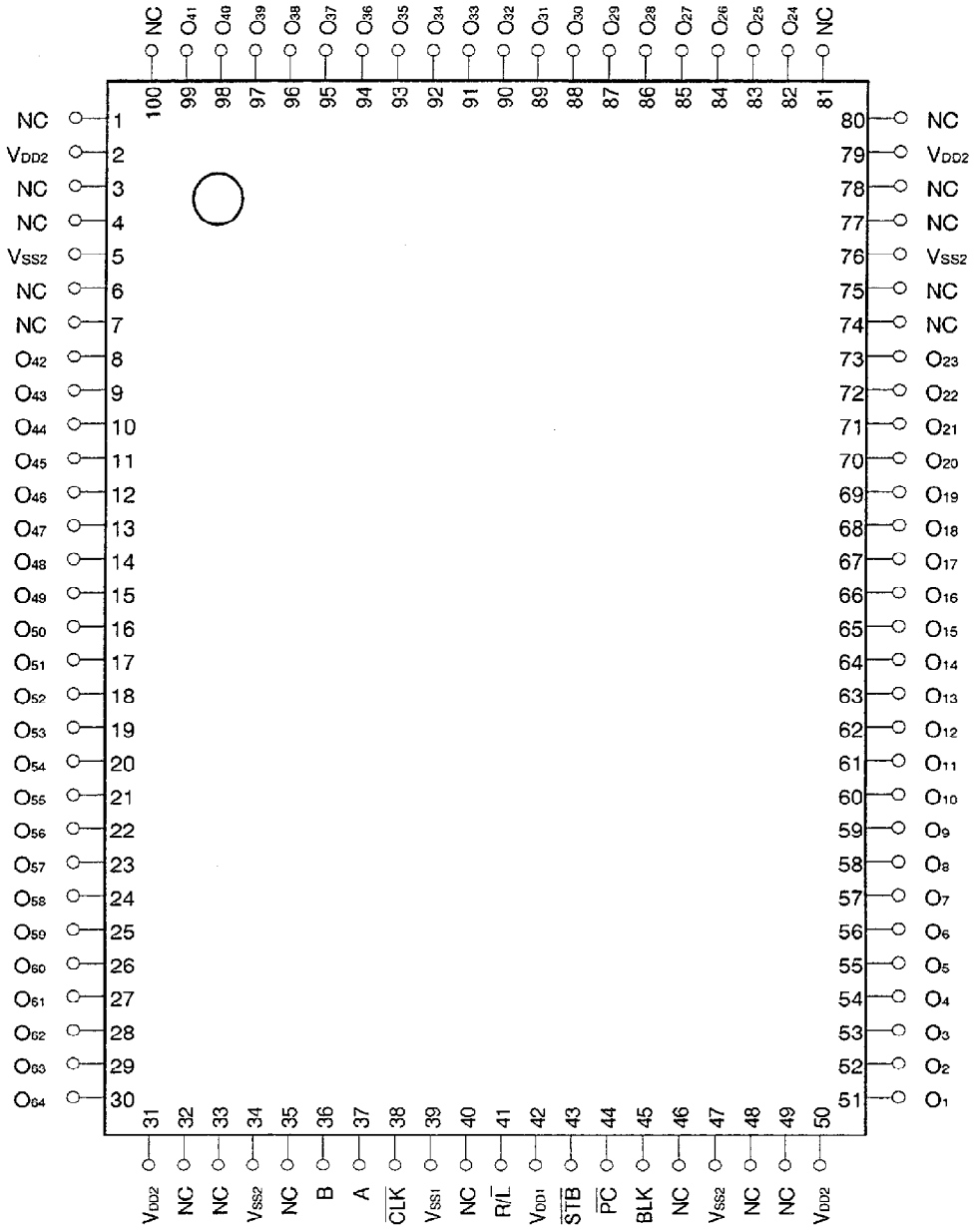
Printed in Japan

BLOCK DIAGRAM



Note High-voltage CMOS drivers (80 V ±25 mA MAX.)

PIN CONFIGURATION (Top View)



Cautions 1. Be sure to leave pin 40 open because it is connected to the lead frame.

2. Be sure to use all the V_{DD1}, V_{DD2}, V_{SS1}, and V_{SS2} pins. Keep the V_{SS1} and V_{SS2} pins at the same voltage level.

3. Supply power to V_{DD1}, logic inputs, and V_{DD2} in this order to protect the device from destruction due to latch up. Turn off power in the reverse order.
   Observe these power sequences even during a transition period.

PIN FUNCTIONS

Pin Symbol	Pin Name	Pin Number	Remark
$\overline{PC}$	Polarity reverse input	44	$\overline{PC}$ = L: Reverses polarities of all outputs
BLK	Blank input	45	BLK = H: All outputs = H or L
$\overline{STB}$	Latch strobe input	43	Through at L, holds data at H
A	RIGHT data I/O	37	R/$\overline{L}$ = H: A input, B output
B	LEFT data I/O	36	R/$\overline{L}$ = L: B input, A output
$\overline{CLK}$	Clock input	38	Executes shift at falling edge
R/$\overline{L}$	Shift direction control input	41	Right shift mode at H A → O_1 ... O_{64} → B Left shift mode at L B → O_{64} ... O_1 → A
O_1 to O_{64}	High-voltage output	51 to 73, 82 to 99, 8 to 30	80 V 25 $mA_{MAX.}$
V_{DD1}	Logic power supply	42	5 V ± 10 %
V_{DD2}	Driver power supply	2, 31, 50, 79	10 to 70 V
V_{SS1}	Logic ground	39	Connected to GND of system
V_{SS2}	Power ground	5, 34, 47, 76	Connected to GND of system
NC	Vacant pin	1, 3, 4, 6, 7, 32, 33, 35, 40, 46, 48, 49, 74, 75, 77, 78, 80, 81, 100	No connection. Be sure to leave pin 40 open.

TRUTH TABLE 1 (SHIFT REGISTER)

Input		I/O		Shift Register
R/$\overline{L}$	$\overline{CLK}$	A	B	
H	↓	Input	Output Note 1	Right shift
H	H or L		Output	Hold
L	↓	Output Note 2	Input	Left shift
L	H or L	Output		Hold

Notes 1. S_{63} is shifted to the position of S_{64} and output from B at the falling edge of the clock.

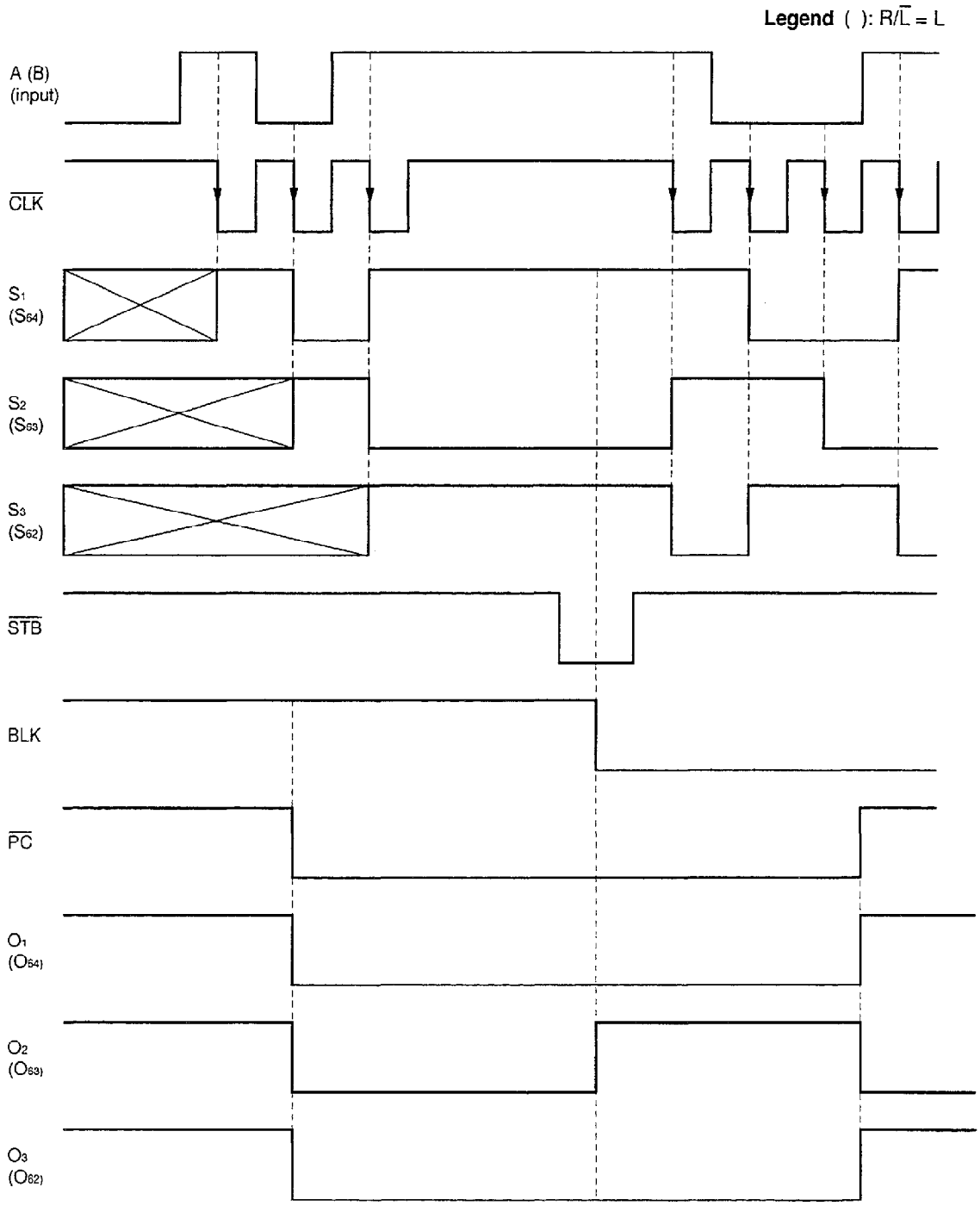
2. S_2 is shifted to the position of S_1 and output from A at the falling edge of the clock.

TRUTH TABLE 2 (LATCH AND DRIVER)

Input				Driver Output Stage
A (B)	$\overline{STB}$	BLK	$\overline{PC}$	
X	X	H	H	H (all drivers: H)
X	X	H	L	L (all drivers: L)
H	L	L	H	H
H	L	L	L	L
L	L	L	H	L
L	L	L	L	H
X	H	L	H	Outputs data immediately before $\overline{STB}$ goes to H
X	H	L	L	Reverses and outputs data immediately before $\overline{STB}$ goes to H

Remark X = H or L, H = high level, L = low level

TIMING CHART



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{DD1}	−0.5 to + 7.0	V
Logic input voltage	V_I	−0.5 to V_{DD1} + 0.5	V
Logic output voltage	V_{O1}	−0.5 to V_{DD1} + 0.5	V
Driver supply voltage	V_{DD2}	−0.5 to 80	V
Driver output voltage	V_{O2}	−0.5 to V_{DD2} + 0.5	V
Driver output current	I_{O2}	± 25	mA
Permissible package dissipation	P_D	1000	mW
Operating temperature range	T_A	−40 to +85	°C
Storage temperature range	$T_{stg.}$	−65 to +150	°C

RECOMMENDED OPERATING RANGE (T_A = −40 to 85 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD1}	4.5	5.0	5.5	V
High-level input voltage	V_{IH}	0.7 • V_{DD1}		V_{DD1}	V
Low-level input voltage	V_{IL}	0		0.2 • V_{DD1}	V
Driver supply voltage	V_{DD2}	10		70	V
Driver output current	I_{OL2}			+20	mA
	I_{OH2}			−20	mA

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, V_{DD1} = 5.0 V, V_{DD2} = 70 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level output voltage	V_{OH1}	Logic I_{OH1} = −1.0 mA	0.9 • V_{DD1}			V
Low-level output voltage	V_{OL1}	Logic I_{OL1} = 1.0 mA			0.1 • V_{DD1}	V
High-level output voltage	V_{OH21}	O_1 to O_{64}, I_{OH2} = −0.5 mA	69			V
	V_{OH22}	O_1 to O_{64}, I_{OH2} = −5.0 mA	65			V
Low-level output voltage	V_{OL21}	O_1 to O_{64}, I_{OL2} = 2.5 mA			1.0	V
	V_{OL22}	O_1 to O_{64}, I_{OL2} = 20 mA			10	V
High-level input current	I_{IH}	V_I = V_{DD1}			1.0	μA
Low-level input current	I_{IL}	V_I = 0 V			−1.0	μA
High-level input voltage	V_{IH}		0.7 • V_{DD1}			V
Low-level input voltage	V_{IL}				0.2 • V_{DD1}	V
Static current dissipation	I_{DD1}	Logic, T_A = 25 °C			10	μA
	I_{DD1}	Logic, T_A = −40 to +85 °C			100	μA
	I_{DD2}	Driver, T_A = 25 °C			100	μA
	I_{DD2}	Driver, T_A = −40 to +85 °C			1000	μA

SWITCHING CHARACTERISTICS

(T_A = 25 °C, V_{DD1} = 5.0 V, V_{DD2} = 70 V, V_{SS1} = V_{SS2} = 0 V, logic C_L = 15 pF, driver C_L = 50 pF)

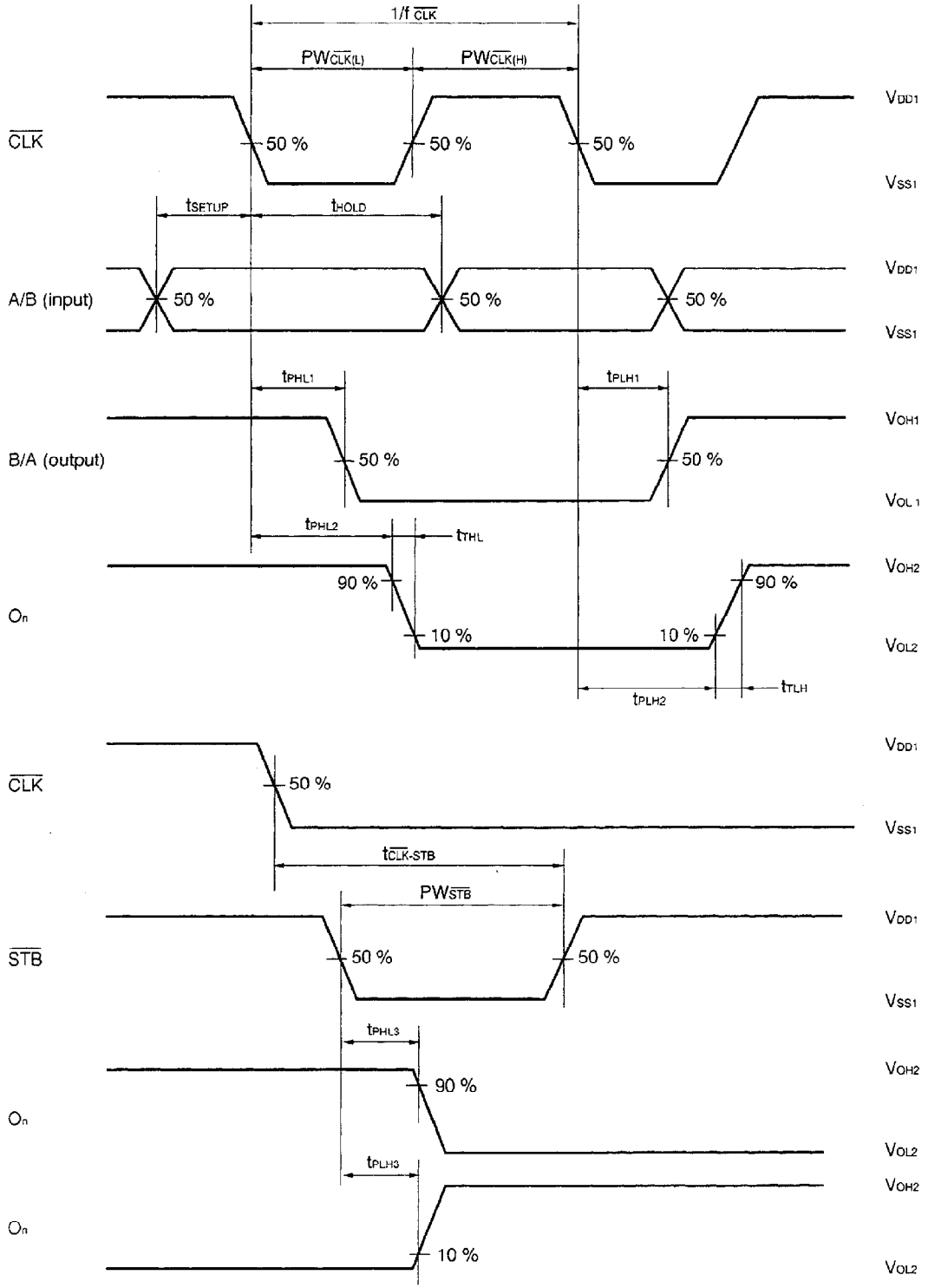
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Propagation delay time	t_{PHL1}	$\overline{CLK}$ → A/B			50	ns
	t_{PLH1}				50	ns
	t_{PHL2}	$\overline{CLK}$ → O_1 to O_{64}			300	ns
	t_{PLH2}				300	ns
	t_{PHL3}	$\overline{STB}$ → O_1 to O_{64}			300	ns
	t_{PLH3}				300	ns
	t_{PHL4}	BLK → O_1 to O_{64}			300	ns
	t_{PLH4}				300	ns
	t_{PHL5}	$\overline{PC}$ → O_1 to O_{64}			300	ns
	t_{PLH5}				300	ns
Rise time	t_{TLH}	O_1 to O_{64}			200	ns
Fall time	t_{THL}	O_1 to O_{64}			200	ns
Maximum clock frequency	$f_{max.}$	Duty = 50%, data loading	25			MHz
		In cascade connection	16			MHz
Input capacitance	C_I				20	pF

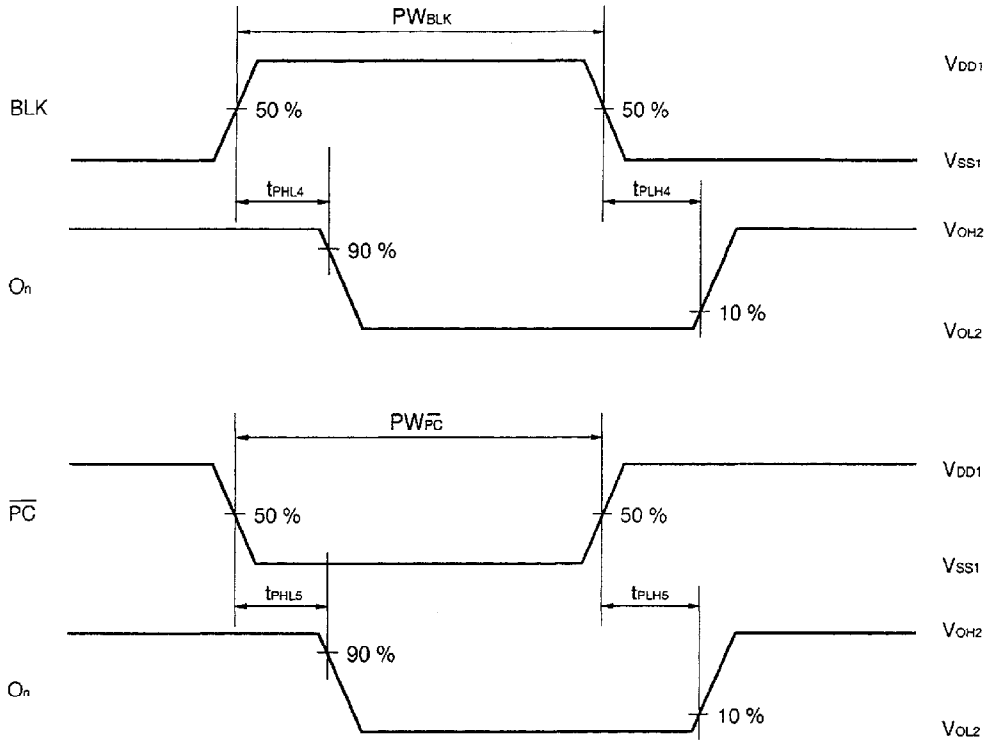
TIMING REQUIREMENTS

(T_A = –40 to 85 °C, V_{DD1} = 4.5 to 5.5 V, V_{DD2} = 10 to 70 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock pulse width	$PW_{\overline{CLK}}$		20			ns
Strobe pulse width	$PW_{\overline{STB}}$		20			ns
Blank pulse width	PW_{BLK}		560			ns
$\overline{PC}$ pulse width	$PW_{\overline{PC}}$		560			ns
Data setup time	t_{SETUP}		10			ns
Data hold time	t_{HOLD}		10			ns
Clock-strobe time	$t_{\overline{CLK}\text{-}\overline{STB}}$	$\overline{CLK}$ ↓ → $\overline{STB}$ ↑	50			ns

SWITCHING CHARACTERISTIC WAVEFORMS

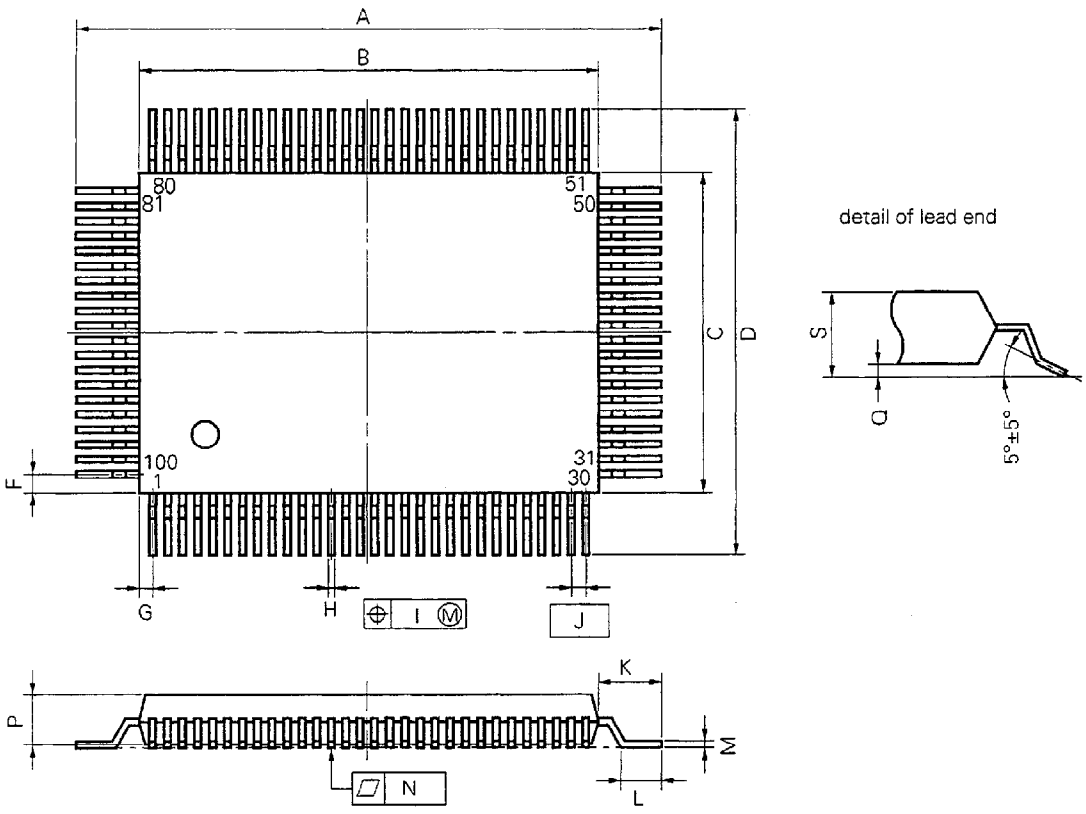



PWBLK
BLK
50 %
50 %
VDD1
VSS1
tPHL4
tPLH4
VOH2
90 %
On
10 %
VOL2
PWPC
PC
50 %
50 %
VDD1
VSS1
tPHL5
tPLH5
VOH2
90 %
On
10 %
VOL2

PACKAGE DRAWING

μPD16306AGF-3BA (Iron lead frame)

100 PIN PLASTIC QFP (14x20)



P100GF-65-3BA-2

NOTE

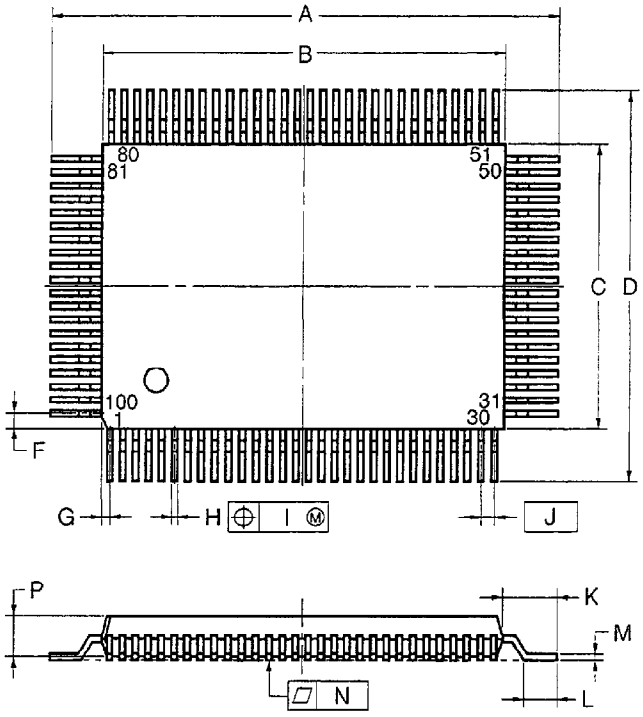
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

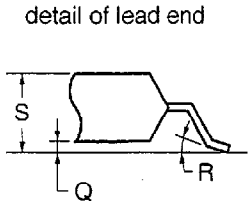
ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

PACKAGE DRAWING

μPD16306AGF-3RA (Copper lead frame)

100 PIN PLASTIC QFP (14×20)





NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.2	$0.913^{+0.009}_{-0.008}$
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.2	0.677±0.008
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S100GF-65-3BA-3

RECOMMENDED SOLDERING CONDITIONS

Please perform the soldered mounting of this product under the following recommended conditions.

For soldering methods and conditions other than those recommended here, please contact your NEC sales representative.

Surface Mount Type

For details on recommended soldering conditions, please refer to the **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

μPD16306AGF-3BA

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared Reflow	Package peak temperature: 235 °C, time: up to 30 sec. (no less than 210 °C), count: once, restricted number of days: none Note	IR-35-00-1
VPS	Package peak temperature: 215 °C, time: up to 40 sec. (no less than 200 °C), count: once, restricted number of days: none Note	VP15-00-1
Pin Part Heating	Pin part temperature: no more than 300 °C, time: up to 10 sec., restricted number of days: none Note	

Note This refers to the restricted number of days for storage after decapsulating the dry pack. The storage conditions are no more than 25 °C and 65 % RH.

Caution Please avoid mixing use of soldering methods (except for pin part heating methods).

References

NEC Semiconductor Device Reliability/Quality Control System (IEI-1212)
Quality Grades of NEC Semiconductor Devices (IEI-1209)
Semiconductor Device Mounting Technology Manual (C10535E)

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