

PRELIMINARY DATA SHEET



MOS INTEGRATED CIRCUIT
μPD16306

HIGH VOLTAGE CMOS DRIVER FOR PDP,EL,VFD

DESCRIPTION

μPD16306 is high voltage driver for PDP, EL or VFD graphic panel structured by CMOS process. Logic power supply is 5 V connecting direct to control logic. Maximum output voltage is 80 V and maximum current is 50 mA.

FEATURES

- 80 V Output Voltage Swing Capability
- 50 mA Output Sink and Source Current Capability
- 64 bit Shift-register and Latch
- High Speed Serial DATA Transferring (f_{max} - 20 MHz min.)
- Low Standby Current 100 μA

ORDERING INFORMATION

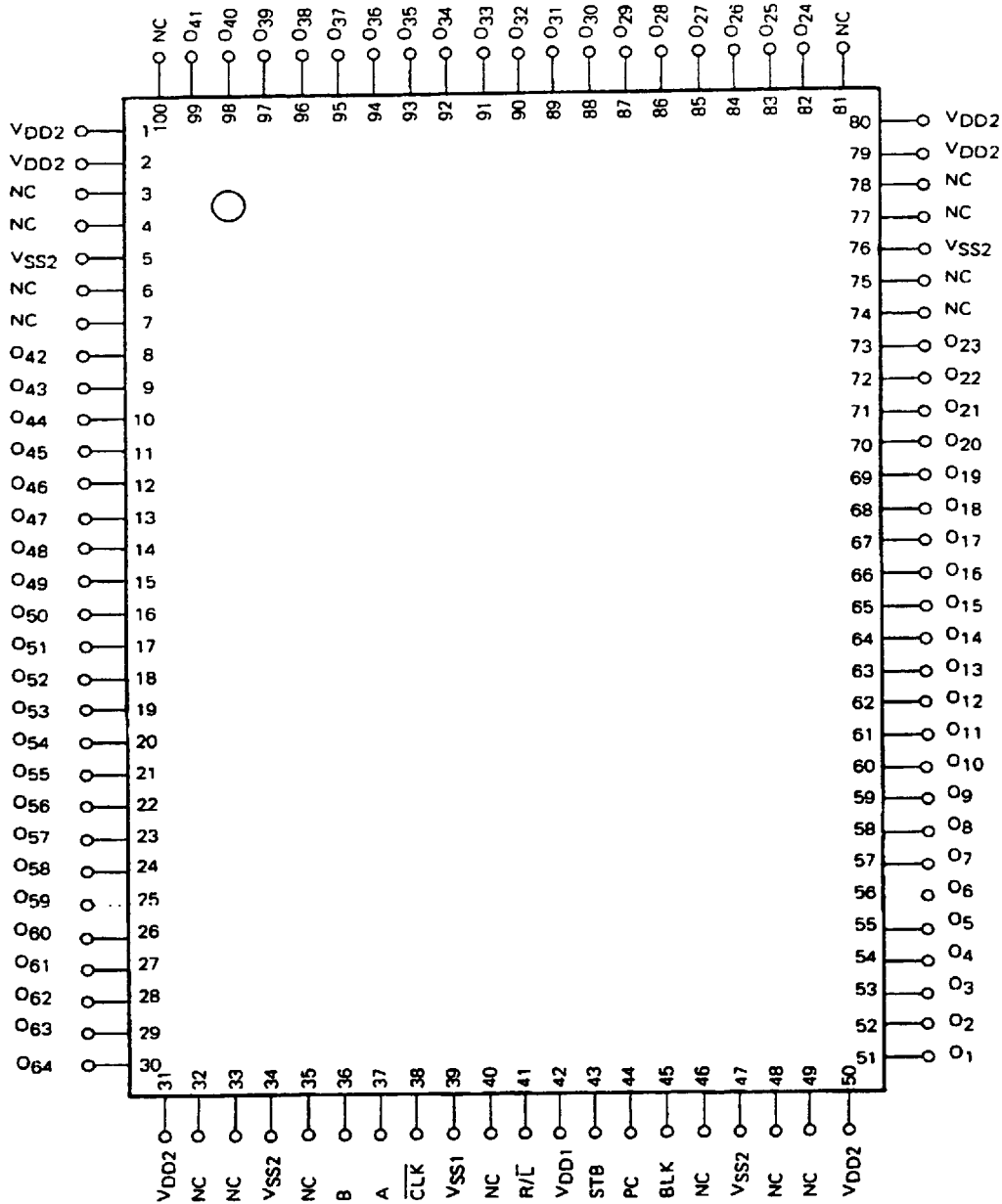
PART No.	Package
μPD16306GF-3BA	100 pin Plastic QFP (14 x 20)

The information in this document is subject to change without notice.

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PIN CONNECTION DIAGRAM (Top View)



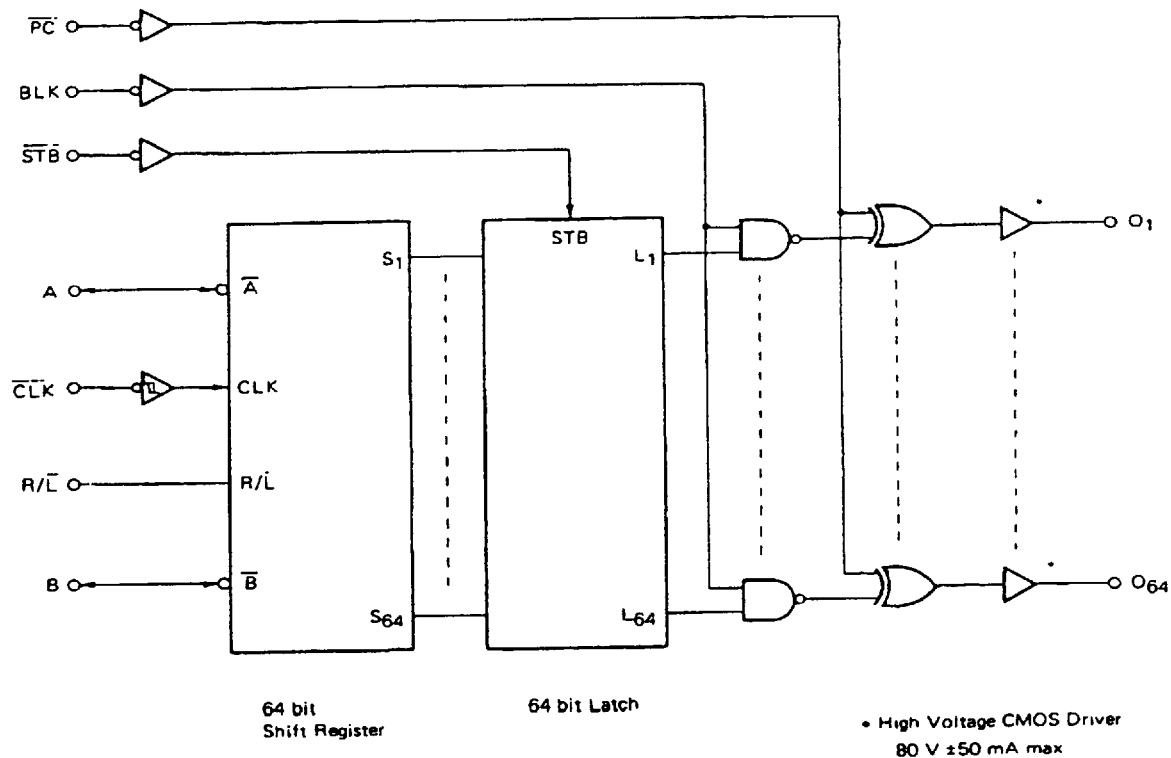
Note:
 The 40 pin (NC) should be open.
 All the power supply terminals should be used.
 VSS1 and VSS2 should be respectively connected with themselves outside.

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BLOCK DIAGRAM



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PIN CONFIGURATION

SYMBOL	PIN NAME	PIN No.	FUNCTION
\overline{PC}	Polarity Change input	44	All driver outputs' level are inverted while PC is L.
BLK	Plank input	45	All driver outputs are H while BLK is H and PC is H.
\overline{STB}	Latch Strobe input	43	Latch's status is data through while STB is L.
A	Right Data input/output	37	R/L = H : A = IN, B = OUT R/L = L : A = OUT, B = IN
B	Left Data input/output	36	
CLK	Clock input	38	Data of shift-register is shifted while CLK is going H to L. (Negative edge is active.)
R/L	Shift Direction Control input	41	H : Right Shift Mode A → O ₁ ...O ₆₄ → B L : Left Shift Mode B → O ₆₄ ...O ₁ → A
O ₁ -O ₆₄	Driver Outputs	8-30, 51-73 82-99	High voltage output 80 V, 50 mA
V _{DD1}	Logic Power Supply	42	5 V ± 10 %
V _{DD2}	Driver Power Supply	1, 2, 31, 50, 79, 80	10 - 70 V
V _{SS1}	Ground (for Logic)	39	
V _{SS2}	Ground (for Driver)	5, 34, 47, 76	
NC	No Connect	3, 4, 6, 7, 32, 33, 35, 40, 46, 48, 49, 74, 75, 77, 78, 81, 100	No. 40 pin should be open.

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TRUTH TABLE 1 (Shift-Register part)

INPUT		IN/OUT		SHIFT-REGISTER
R/L	CLK	A	B	
H	↓	IN	OUT	DATA is shifted.
H	H or L	IN	OUT	No Change
L	↓	OUT	IN	DATA is shifted.
L	H or L	OUT	IN	No Change

TRUTH TABLE 2 (Latch, Driver part)

DATA	STB	BLK	PC	DRIVER OUTPUT
X	X	H	H	ALL H
X	X	H	L	ALL L
H	L	L	H	H
H	L	L	L	L
L	L	L	H	L
L	L	L	L	H
X	H	L	H	Latch's data output
X	H	L	L	Latch's data output (inverting)

DATA are contents of shift register. (S₁-S₆₄)

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ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C, V_{SS} = 0 V)

Logic Power Supply	V _{DD1}	-0.5 to +7.0	V
Input Voltage	V _I	-0.5 to V _{DD1} +0.5	V
Logic Output Voltage	V _{O1}	-0.5 to V _{DD1} +0.5	V
Driver Power Supply	V _{DD2}	-0.5 to 80	V
Driver Output Voltage	V _{O2}	-0.5 to V _{DD2} +0.5	V
Driver Maximum Current	I _{O2}	±50	mA
Power Dissipation/Package	P _D	1000	mW
Operating Temperature	T _{OP1}	-40 to +85	°C
Storage Temperature	T _{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 25 °C, V_{SS} = 0 V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Logic Power Supply	V _{DD1}	4.5	5	5.5	V
High Level Input Voltage	V _{IH}	0.7 · V _{DD1}		V _{DD1}	V
Low Level Input Voltage	V _{IL}	0		0.2 · V _{DD1}	V
Driver Power Supply	V _{DD2}	10		70	V
Driver Output Current	I _{OL2}			+40	mA
	I _{OH2}			-40	mA

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DC CHARACTERISTICS

($T_a = 25^\circ\text{C}$, $V_{DD1} = 4.5\text{ V to } 5.5\text{ V}$, $V_{DD2} = 70\text{ V}$, $V_{SS} = 0\text{ V}$)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
High Level Output Voltage	V_{OH1}	$0.9 \cdot V_{DD1}$			V	Logic, $I_{OH1} = -1\text{ mA}$
Low Level Output Voltage	V_{OL1}			$0.1 \cdot V_{DD1}$	V	Logic, $I_{OL1} = 1\text{ mA}$
High Level Output Voltage	V_{OH21}	69			V	O_1-O_{64} , $I_{OH2} = -1\text{ mA}$
	V_{OH22}	65			V	O_1-O_{64} , $I_{OH2} = -10\text{ mA}$
Low Level Output Voltage	V_{OL21}			1	V	O_1-O_{64} , $I_{OL2} = 5\text{ mA}$
	V_{OL22}			10	V	O_1-O_{64} , $I_{OL2} = 40\text{ mA}$
High Level Input Current	I_{IH}			1	μA	$V_I = V_{DD1}$
Low Level Input Current	I_{IL}			-1	μA	$V_I = 0\text{ V}$
High Level Input Voltage	V_{IH}	$0.7 \cdot V_{DD1}$			V	
Low Level Input Voltage	V_{IL}			$0.2 \cdot V_{DD1}$	V	
Stand by Current	I_{DD1}			1.0	mA	for V_{DD1} , $T_a = -40\text{ to } +85^\circ\text{C}$
	I_{DD1}			10	μA	for V_{DD1} , $T_a = 25^\circ\text{C}$
	I_{DD2}			1.0	mA	for V_{DD2} , $T_a = -40\text{ to } +85^\circ\text{C}$
	I_{DD2}			100	μA	for V_{DD2} , $T_a = 25^\circ\text{C}$

AC CHARACTERISTICS

($T_a = 25^\circ\text{C}$, $V_{DD1} = 5\text{ V}$, $V_{DD2} = 70\text{ V}$, Logic $C_L = 15\text{ pF}$)

Driver $C_L = 50\text{ pF}$)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Delay Time	t_{PHL1}			50	ns	CLK → A/B
	t_{PLH1}			50	ns	
	t_{PHL2}			160	ns	CLK → O_1-O_{64}
	t_{PLH2}			160	ns	
	t_{PHL3}			150	ns	STB → O_1-O_{64}
	t_{PLH3}			150	ns	
	t_{PHL4}			145	ns	BLK → O_1-O_{64}
	t_{PLH4}			145	ns	
	t_{PHL5}			140	ns	PC → O_1-O_{64}
	t_{PLH5}			140	ns	
Rise Time	t_{TLH}			70	ns	O_1-O_{64}
Fall Time	t_{THL}			70	ns	O_1-O_{64}
Maximum Frequency	f_{max}	20	30		MHz	Duty=50%, for CLK
Input Capacitance	C_i		10	15	pF	

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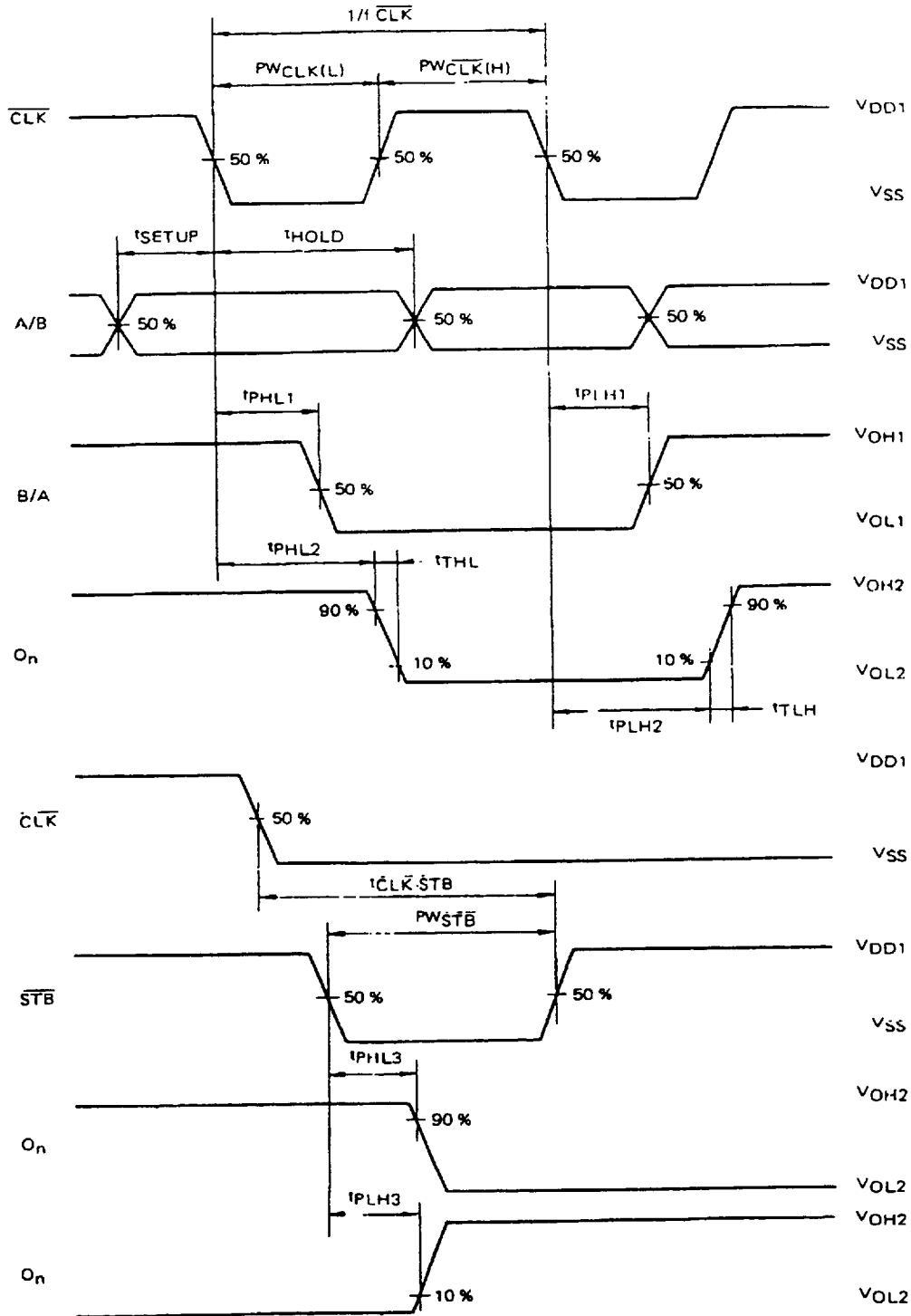
AC TIMING REQUIREMENT ($T_a = -40$ to 80 °C, $V_{DD1} = 4.5$ to 5.5 V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Clock Pulse Width	PW \overline{CLK}	20			ns	
Strobe Pulse Width	PW \overline{STB}	20			ns	
Blank Pulse Width	PW \overline{BLK}	200			ns	
Polarity Change Pulse Width	PW \overline{PC}	200			ns	
Data Setup Time	t \overline{SETUP}	10			ns	
Data Hold Time	t \overline{HOLD}	10			ns	
Setup Time	t $\overline{CLK-STB}$	50			ns	for CLK ↓ to STB ↓

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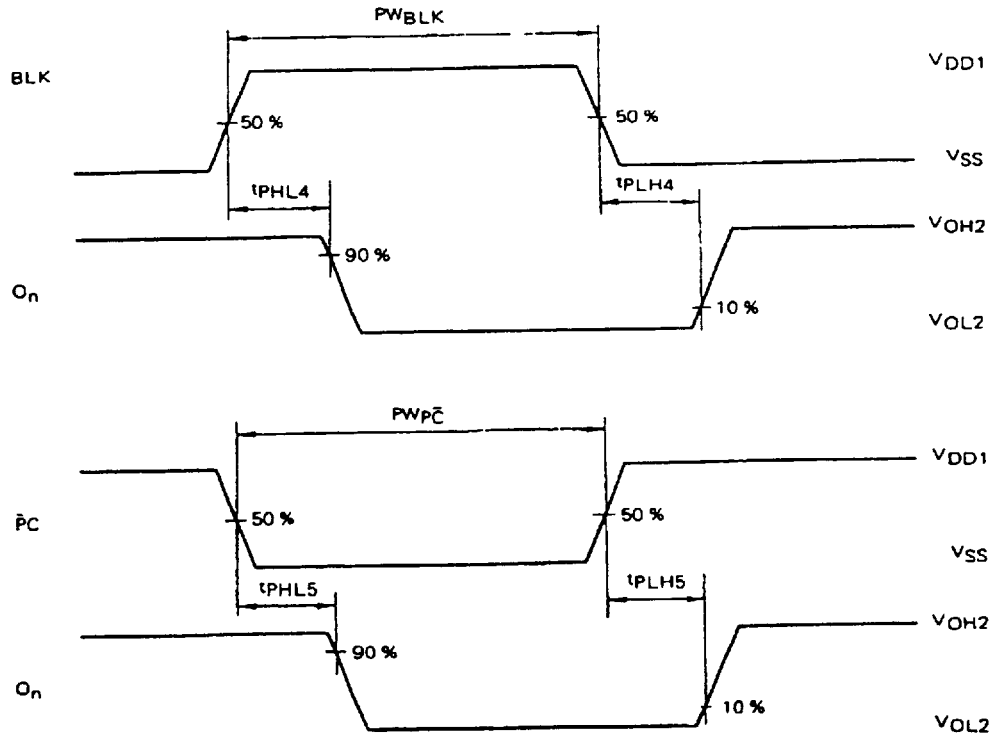
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AC CHARACTERISTICS WAVEFORM



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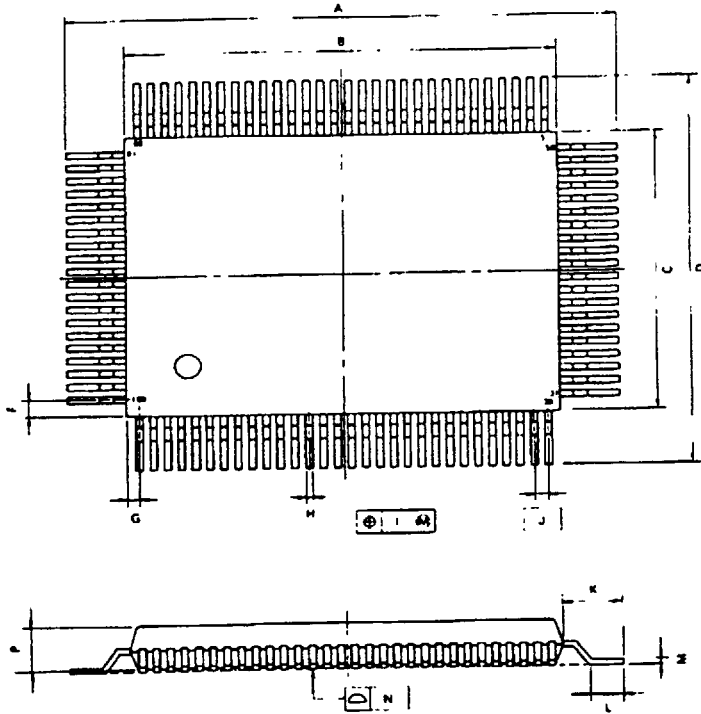


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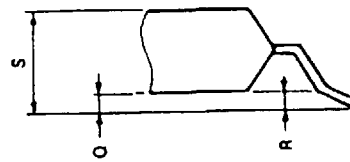
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PACKAGE DIMENSIONS

100 Pin Plastic QFP (14 x 20) (unit: mm)



detail of lead end



P100GF-65-3BA-1

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6 ^{+0.4}	0.929 ^{+0.016}
B	20.0 ^{+0.2}	0.795 ^{+0.008}
C	14.0 ^{+0.2}	0.551 ^{+0.008}
D	17.6 ^{+0.4}	0.693 ^{+0.016}
F	0.8	0.031
G	0.6	0.024
H	0.30 ^{+0.10}	0.012 ^{+0.004}
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8 ^{+0.2}	0.071 ^{+0.008}
L	0.8 ^{+0.2}	0.031 ^{+0.008}
M	0.15 ^{+0.05}	0.006 ^{+0.002}
N	0.15	0.006
P	2.7	0.106
Q	0.1 ^{+0.1}	0.004 ^{+0.004}
R	0.1 ^{+0.1}	0.004 ^{+0.004}
S	3.0 MAX.	0.119 MAX.