

1/4- to 1/12-DUTY FIP™(VFD) CONTROLLER/DRIVER

DESCRIPTION

The μ PD16315 is a FIP (Fluorescent Indicator Panel, or Vacuum Fluorescent Display) controller/driver that is driven on a 1/4- to 1/12- duty factor. It consists of 16 segment output lines, 4 grid output lines, 8 segment/grid output drive lines, a display memory, a control circuit, and a key scan circuit. Serial data is input to the μ PD16315 through a three-line serial interface. This FIP controller/driver is ideal as a peripheral device for a single-chip microcomputer.

FEATURES

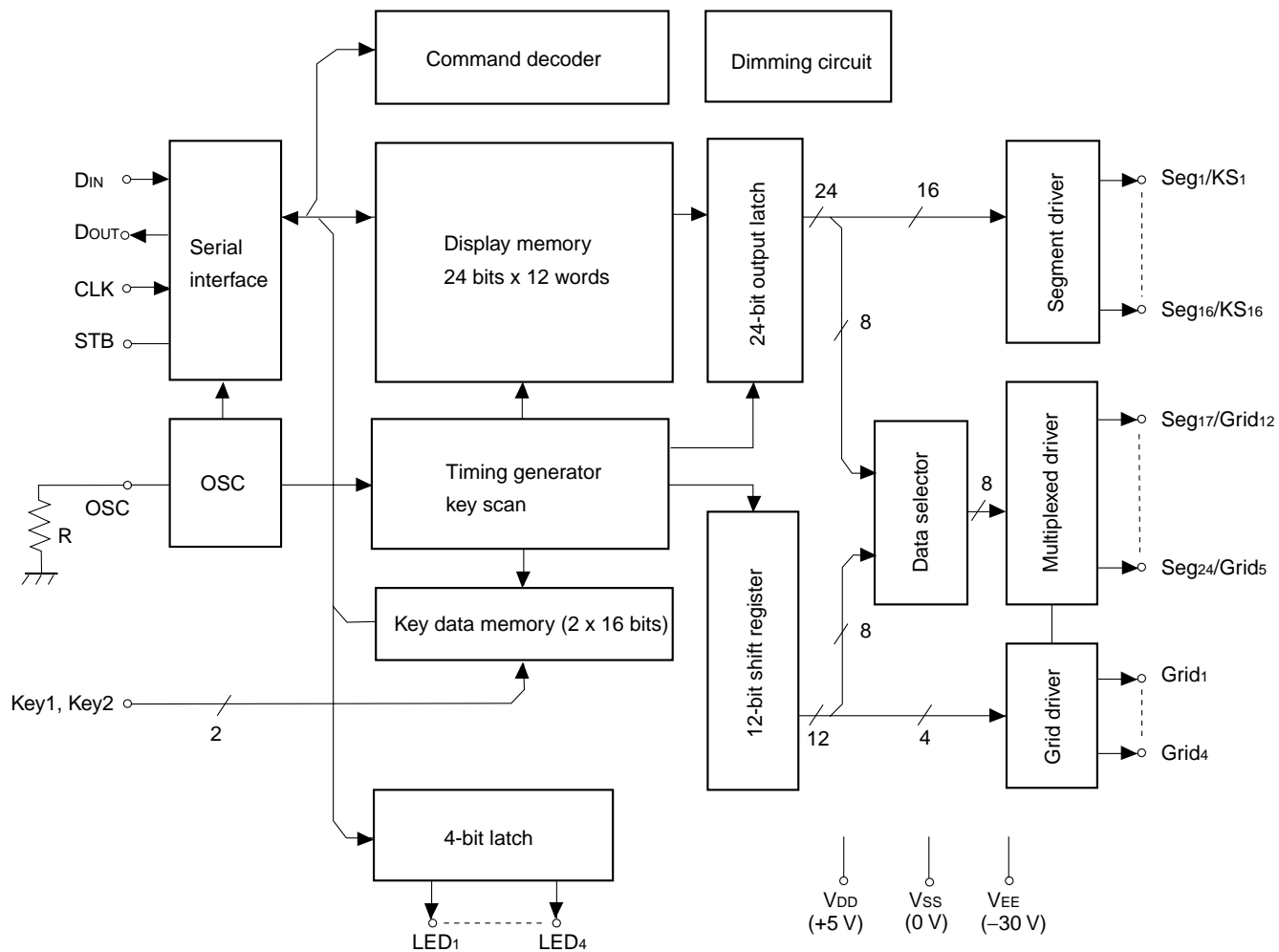
- Multiple display modes: 16-segment & 12-digit to 24-segment & 4-digit
- Key scanning: 16 x 2 matrix
- Dimming circuit: 8 steps
- High-withstanding-voltage output: $V_{DD} - 35$ V MAX.
- LED ports: 4 chs., 20 mA MAX.
- No external resistors necessary for driver outputs: P-ch open-drain + pull-down resistor output
- Serial interface: CLK, STB, DIN, DOUT

ORDERING INFORMATION

Part Number	Package
μ PD16315GB-3BS	44-pin Plastic QFP (10 x 10)

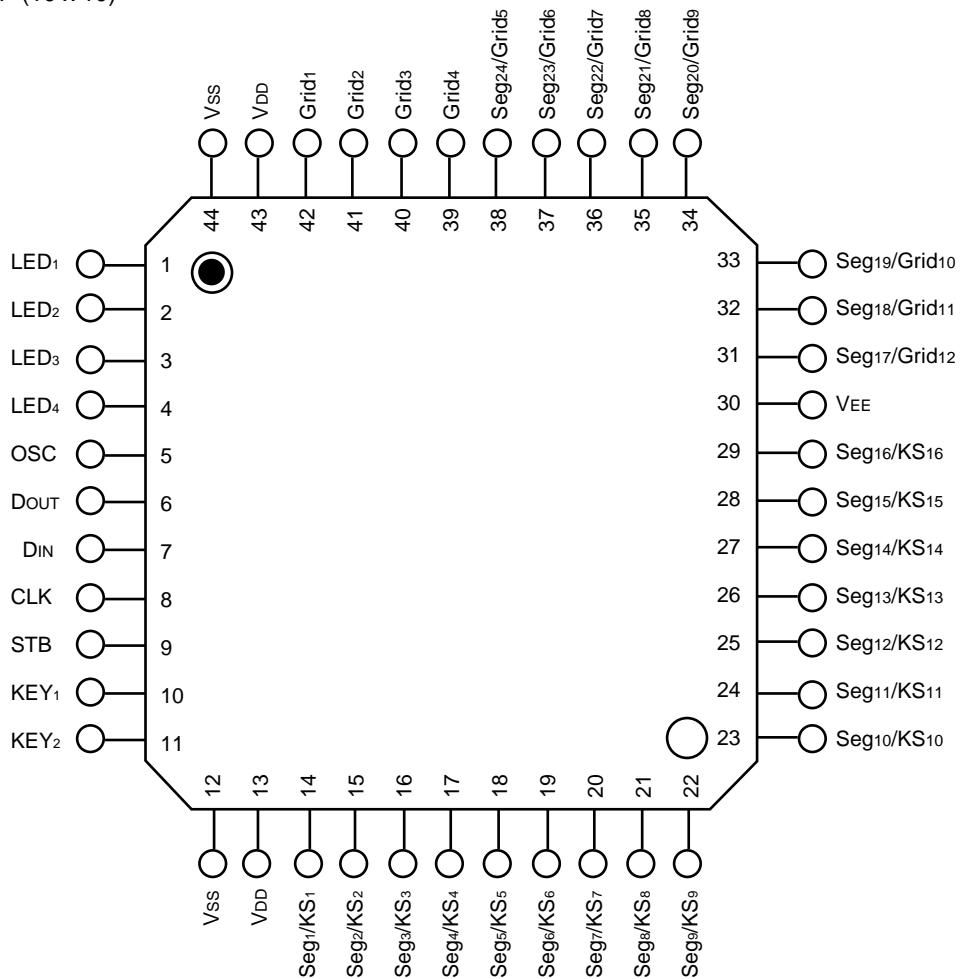
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1. BLOCK DIAGRAM



2. PIN CONFIGURATION (Top View)

44-pin Plastic QFP (10 x 10)



Caution Use all of the power supply pins.

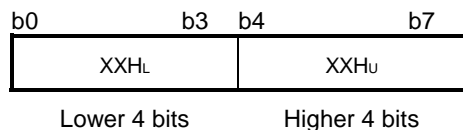
3. PIN FUNCTION

Symbol	Pin Name	Pin No.	I/O	Description
D _{IN}	Data input	7	Input	Input serial data at rising edge of shift clock, starting from the low order bit.
D _{OUT}	Data output	6	Output	Output serial data at the falling edge of the shift clock, starting from low order bit. This is N-ch open-drain output pin.
STB	Strobe	9	–	Initializes serial interface at the rising or falling edge of the μPD16315. It then waits for reception of a command. Data input after STB has fallen is processed as a command. While command data is processed, current processing is stopped, and the serial interface is initialized. While STB is high, CLK is ignored.
CLK	Clock input	8	Input	Reads serial data at the rising edge, and outputs data at the falling edge.
OSC	Oscillator pin	5	–	Connect resistor to this pin to determine the oscillation frequency to this pin. Connect resistor between this pin and GND (V _{SS}).
Seg ₁ /KS ₁ to Seg ₁₆ /KS ₁₆	High-withstanding-voltage output (Segment)	14 to 29	Output	Segment output pins (Dual function as key source)
Grid ₁ to Grid ₄	High-withstanding-voltage output (grid)	39 to 42	Output	Grid output pins
Seg ₁₇ /Grid ₁₂ to Seg ₂₄ /Grid ₅	High-withstanding-voltage output (segment/grid)	31 to 38	Output	These pins are selectable for segment or grid driving.
LED ₁ to LED ₄	LED output	1 to 4	Output	CMOS output, +20 mA MAX.
KEY ₁ , KEY ₂	Key data input	10, 11	Input	Data input to these pins is latched at the end of the display cycle.
V _{DD}	Logic power	13, 43	–	5 V ± 10%
V _{SS}	Logic ground	12, 44	–	Connect this pin to system GND.
V _{EE}	Pull-down level	30	–	V _{DD} – 35 V MAX.

4. DISPLAY RAM ADDRESS AND DISPLAY MODE

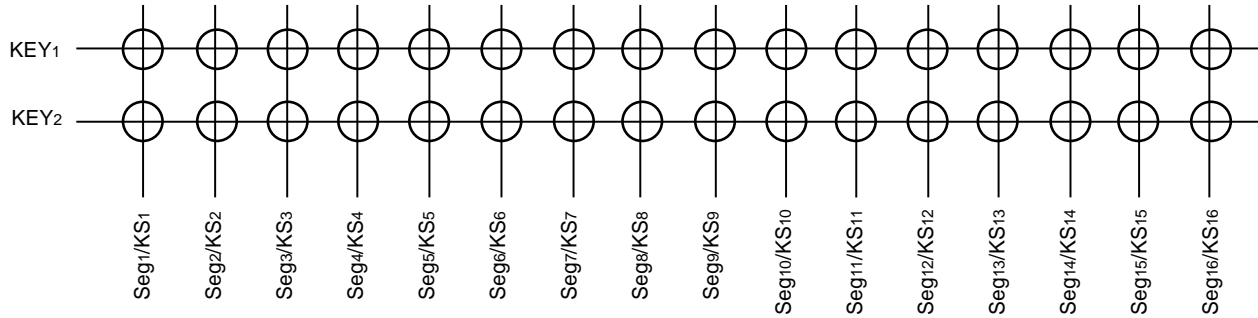
The display RAM stores the data transmitted to the μPD16315 through the serial communication. The addresses are allocated in 8-bit units.

Seg ₁	Seg ₄	Seg ₈	Seg ₁₂	Seg ₁₆	Seg ₂₀	Seg ₂₄	
00H _L	00H _U	01H _L	01H _U	02H _L	02H _U		DIG ₁
03H _L	03H _U	04H _L	04H _U	05H _L	05H _U		DIG ₂
06H _L	06H _U	07H _L	07H _U	08H _L	08H _U		DIG ₃
09H _L	09H _U	0AH _L	0AH _U	0BH _L	0BH _U		DIG ₄
0CH _L	0CH _U	0DH _L	0DH _U	0EH _L	0EH _U		DIG ₅
0FH _L	0FH _U	10H _L	10H _U	11H _L	11H _U		DIG ₆
12H _L	12H _U	13H _L	13H _U	14H _L	14H _U		DIG ₇
15H _L	15H _U	16H _L	16H _U	17H _L	17H _U		DIG ₈
18H _L	18H _U	19H _L	19H _U	1AH _L	1AH _U		DIG ₉
1BH _L	1BH _U	1CH _L	1CH _U	1DH _L	1DH _U		DIG ₁₀
1EH _L	1EH _U	1FH _L	1FH _U	20H _L	20H _U		DIG ₁₁
21H _L	21H _U	22H _L	22H _U	23H _L	23H _U		DIG ₁₂

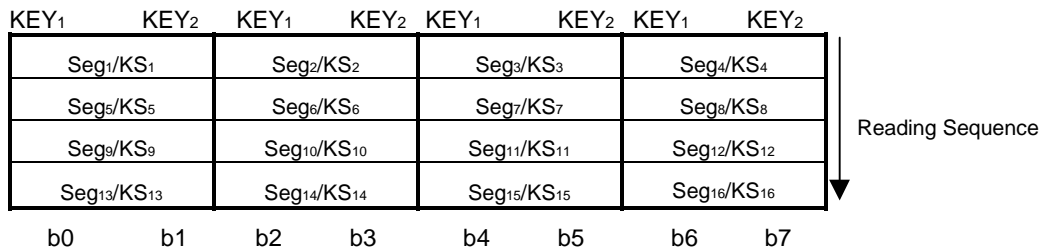


5. KEY MATRIX AND KEY-INPUT DATA STORAGE RAM

The key matrix is made up of a 16 x 2 matrix, as shown below.

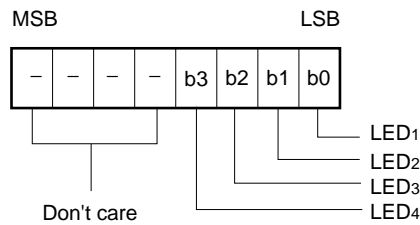


The data of each key is stored as follows, and is read with the read command starting from the least significant bit.



5.1 LED Port

Data is written to the LED port with the write command, starting from the least significant bit. “L” output when the bit of this port is 0, and “H” output when the bit is 1. The data of bits after the 5th bit are ignored.



Remark Power ON application, all the LED ports are “L” output.

6. COMMANDS

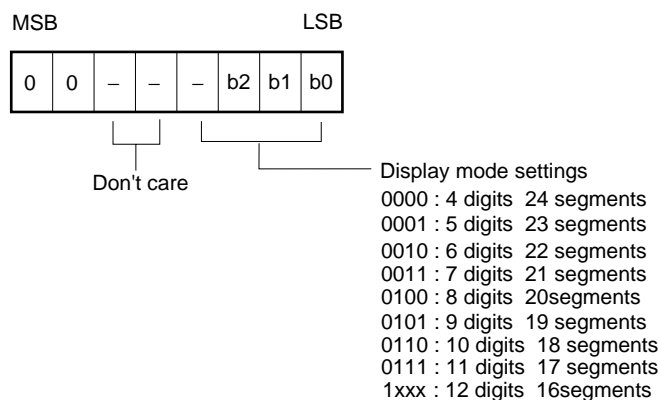
Commands set the display mode and status of the FIP™ (VFD) driver.

The first 1 byte input to the μPD16315 through the DIN pin after the STB pin has fallen is regarded as a command. If STB is set high while commands/data are transmitted, serial communication is initialized, and the commands/data being transmitted are invalid (however, the commands/data previously transmitted remain valid).

(1) Display mode setting commands

These commands initialize the μPD16315 and select the number of segments and the number of grids (1/4- to 1/12-duty, 16 segments to 24 segments).

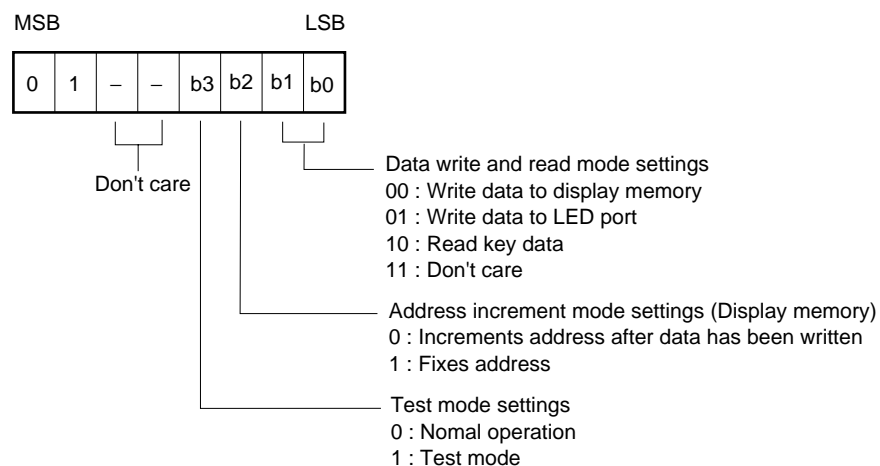
When these commands are executed, the display is forcibly turned OFF, and key scanning is also stopped. To resume display, the display command “ON” must be executed. If the same mode is selected, however, nothing happens.



Remark Power ON application, the 12-digit, 16-segment mode is selected.

(2) Data setting commands

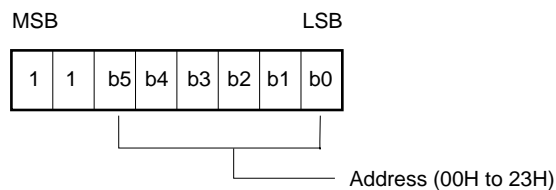
These commands set data write and data read modes.



Remark Power ON application, the normal operation and address increment modes are set.

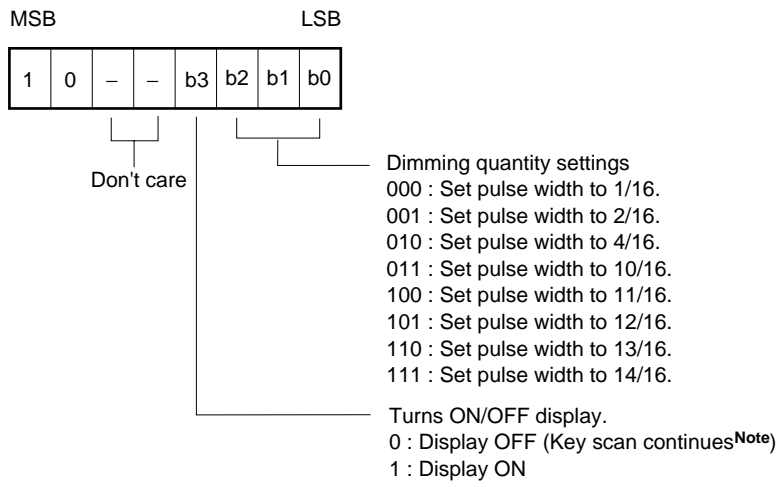
(3) Address setting commands

These commands set an address of the display memory.



- Remarks**
1. If address 24H or higher is set, data is ignored, until a valid address is set.
 2. Power ON application, the address is set to 00H.

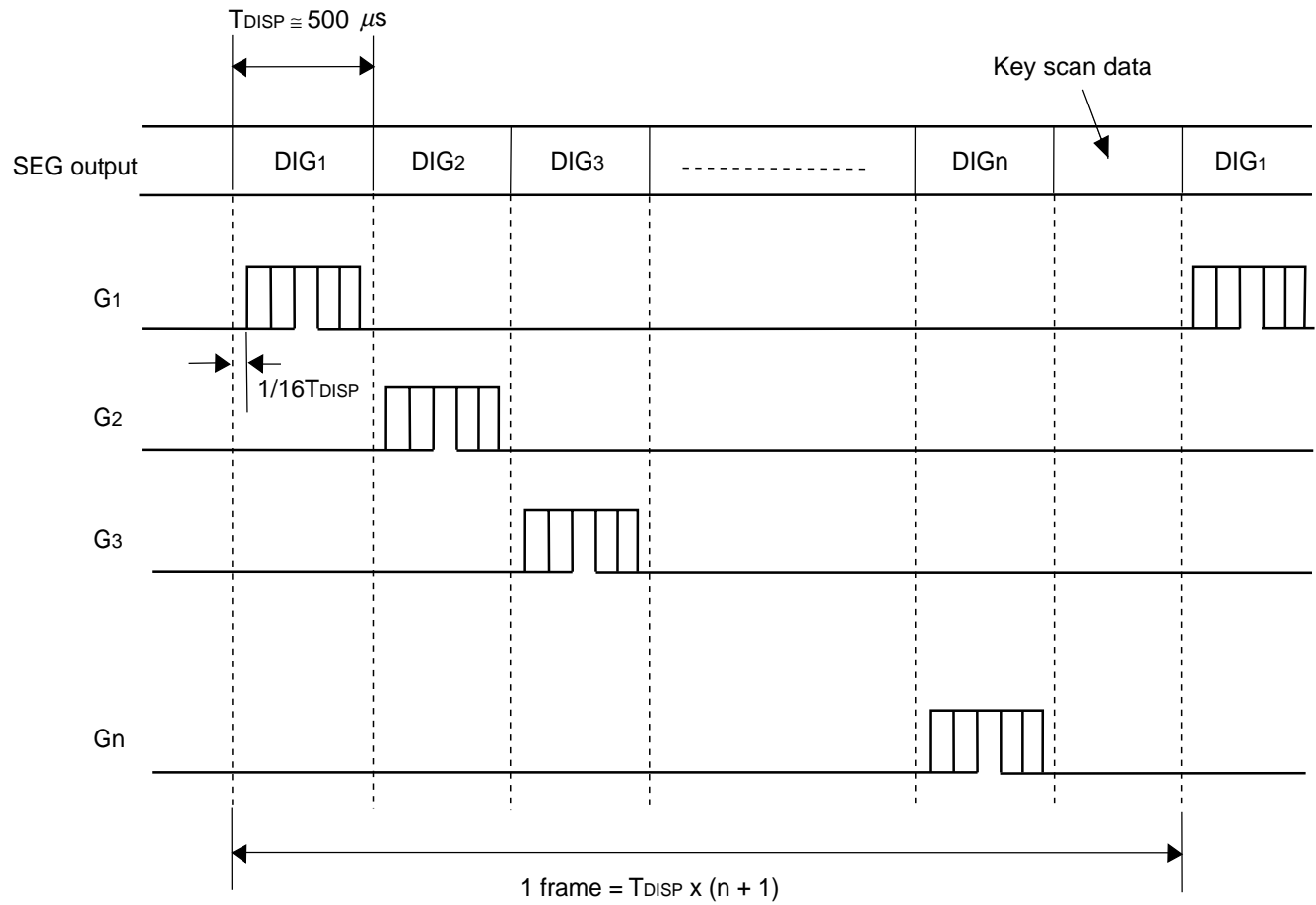
(4) Display control commands



Note Power ON application, key scanning is stopped.

Remark Power ON application, the 1/16 pulse width is set and the display is turned OFF.

7. KEY SCANNING AND DISPLAY TIMING



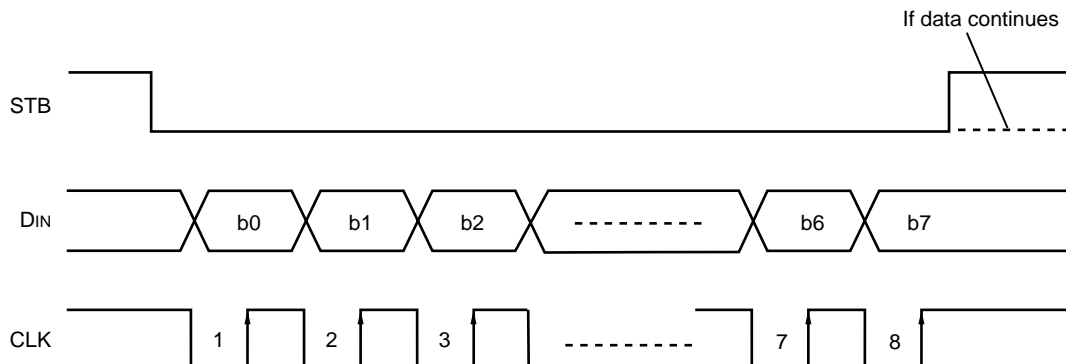
Remark One cycle of key scanning consists of two frame, and data in a 16 x 2 matrix is stored in RAM.

Key Scan Expansion

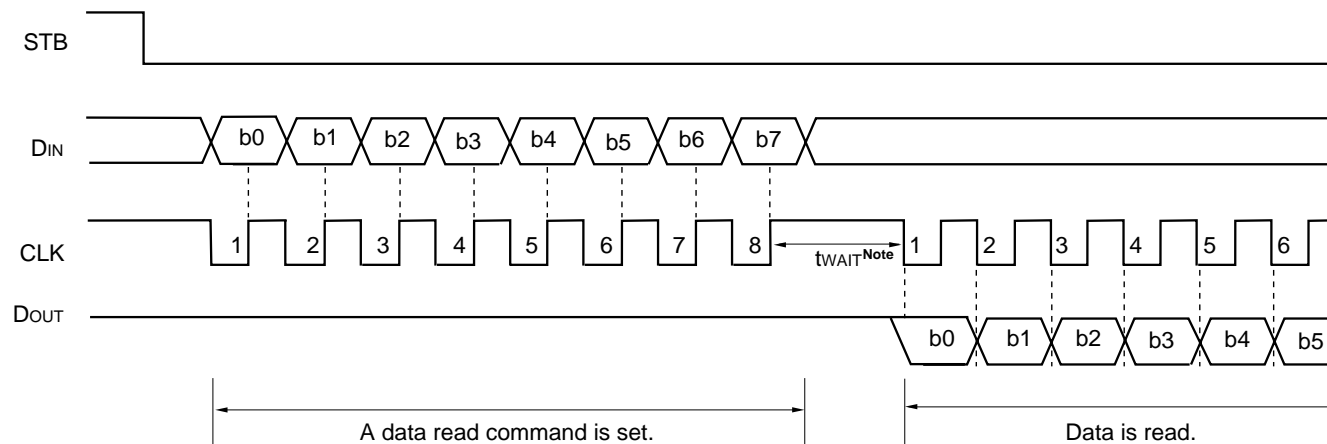
1st frame	DIGn	1	2	3	4	5	6	7	8	DIG1
2nd frame		9	10	11	12	13	14	15	16	

8. SERIAL COMMUNICATION FORMAT

Reception (command/data write)



Transmission (data read)



Note When data is read, a wait time t_{WAIT} of 1 μs is necessary since the rising of the eighth clock that has set the command, until the falling of the first clock that has read the data.

Remark Because the D_{OUT} pin is an N-ch, open-drain output pin, be sure to connect an external pull-up resistor (1 to 10 kΩ) to this pin.

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic Supply Voltage	V _{DD}	-0.5 to +6.0	V
Driver Supply Voltage	V _{EE}	V _{DD} + 0.5 to V _{DD} - 40	V
Logic Input Voltage	V _{I1}	-0.5 to V _{DD} + 0.5	V
FIP Driver Output Voltage	V _{O2}	V _{EE} - 0.5 to V _{DD} + 0.5	V
LED Driver Output Current	I _{O1}	±20	mA
FIP Driver Output Current	I _{O2}	-40 (grid) -15 (segment)	mA
Power Dissipation	P _D	800 ^{Note}	mW
Operating Ambient Temperature	T _A	-40 to +85	°C
Storage Temperature	T _{stg}	-65 to +150	°C

Note Derate at -6.4 mW/°C at T_A = 25°C or higher.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = -20 to 70°C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Supply Voltage	V _{DD}	4.5	5	5.5	V
High-Level Input Voltage	V _{IH}	0.7 V _{DD}		V _{DD}	V
Low-Level Input Voltage	V _{IL}	0		0.3 V _{DD}	V
Driver Supply Voltage	V _{EE}	0		V _{DD} - 35	V

Remark Maximum power consumption P_{MAX.} = FIP driver dissipation + R_L dissipation + LED driver dissipation + dynamic power consumption

Where segment current = 3 mA, grid current = 15 mA, and LED current = 20 mA,

FIP driver dissipation = number of segments x 6 + number of grids/(number of grids + 1) x 30 (mW)

R_L dissipation ≅ (V_{DD} - V_{EE})²/50 x (number of segments + 1) (mW)

LED driver dissipation = number of LEDs x 20 (mW)

Dynamic power consumption = V_{DD} x 5 (mW)

Electrical Characteristics (T_A = -20 to +70°C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, V_{EE} = V_{DD} - 35 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
High-Level Output Voltage	V _{OH1}	LED ₁ - LED ₄ , I _{OH1} = -15 mA	V _{DD} - 1			V
Low-Level Output Voltage	V _{OL1}	LED ₁ - LED ₄ , I _{OL1} = +15 mA			1	V
Low-Level Output Voltage	V _{OL2}	D _{OUT} , I _{OL2} = 4 mA			0.4	V
High-Level Output Current	I _{OH21}	V _O = V _{DD} - 2 V, Seg ₁ /KS ₁ to Seg ₁₆ /KS ₁₆	-3			mA
High-Level Output Current	I _{OH22}	V _O = V _{DD} - 2 V, Grid ₁ to Grid ₄ Seg ₁₇ /Grid ₁₂ to Seg ₂₄ /Grid ₅	-15			mA
Driver Leakage Current	I _{OLEAK}	V _O = V _{DD} - 35 V, driver OFF			-10	μA
Output Pull-Down Resistor	R _L	Driver output	40	65	120	kΩ
Input Current	I _I	V _I = V _{DD} or V _{SS}			±1	μA
High-Level Input Voltage	V _{IH}		0.7 V _{DD}			V
Low-Level Input Voltage	V _{IL}				0.3 V _{DD}	V
Hysteresis Voltage	V _H	CLK, D _{IN} , STB		0.35		V
Dynamic Current Consumption	I _{DDdyn}	Under no load, display OFF			5	mA

Switching Characteristics (T_A = -20 to +70°C, V_{DD} = 4.5 to 5.5 V, V_{EE} = -30 V)

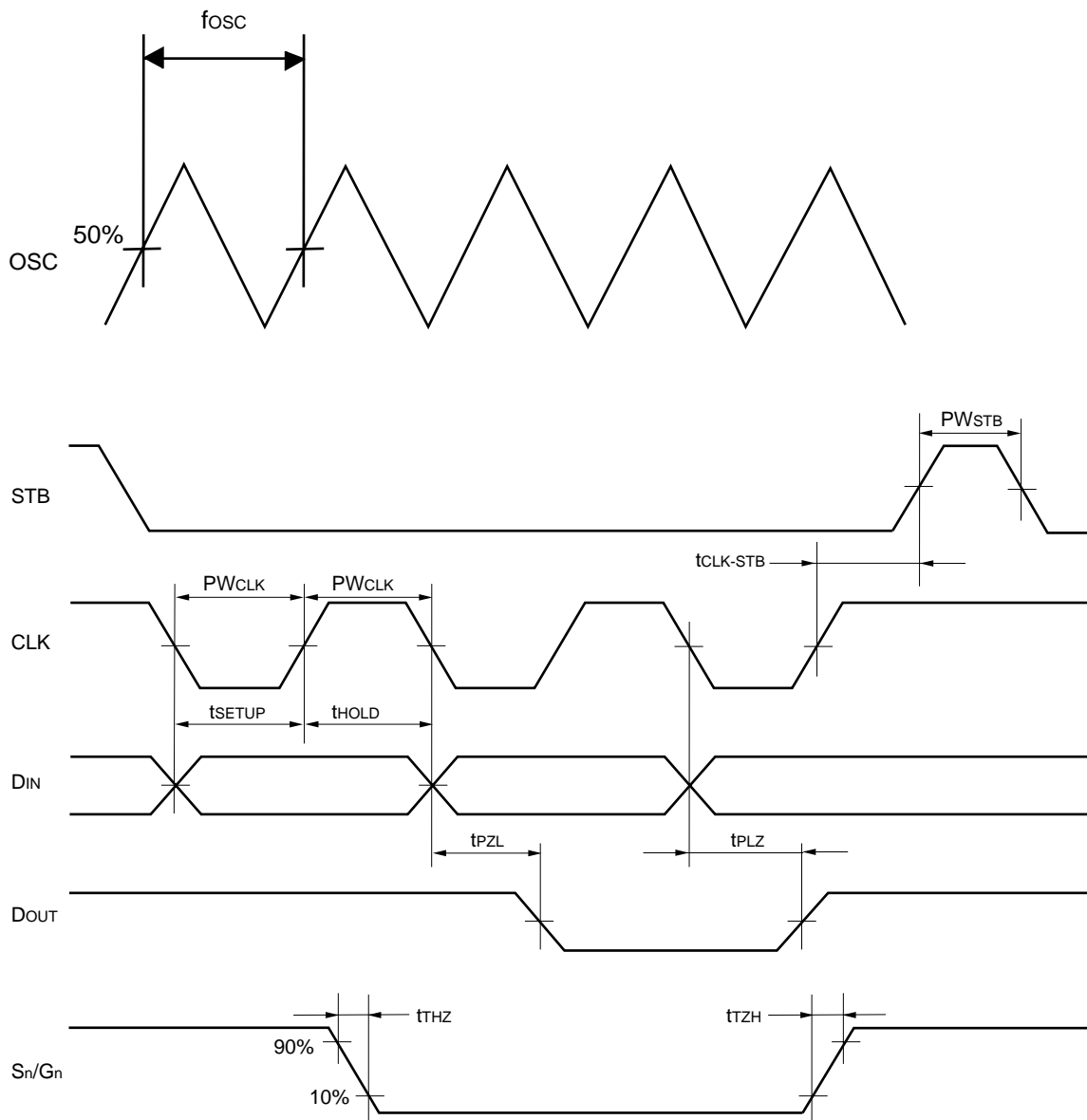
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Oscillation Frequency	f _{OSC}	R = 82 kΩ	350	500	650	kHz
Propagation Delay Time	t _{PLZ}	CLK → D _{OUT}			300	ns
	t _{PZL}	C _L = 15 pF, R _L = 10 kΩ			100	ns
Rise Time	t _{TZH1}	C _L = 300 pF Seg ₁ /KS ₁ to Seg ₁₆ /KS ₁₆			2	μs
	t _{TZH2}		Grid ₁ to Grid ₄ , Seg ₁₇ /Grid ₁₂ to Seg ₂₄ /Grid ₅			0.5
Fall Time	t _{THZ}	C _L = 300 pF, Seg _n , Grid _n			160	μs
Maximum Clock Frequency	f _{MAX}	Duty = 50%	1			MHz
Input Capacitance	C _I				15	pF

Timing Conditions (T_A = -20 to 70°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW _{CLK}		400			ns
Strobe Pulse Width	PW _{STB}		1			μs
Data Setup Time	t _{SETUP}		100			ns
Data Hold Time	t _{HOLD}		100			ns
Clock-Strobe Time	t _{CLK-STB}	CLK ↑ → STB ↑	1			μs
Wait Time	t _{WAIT}	CLK ↑ → CLK ↓ ^{Note}	1			μs

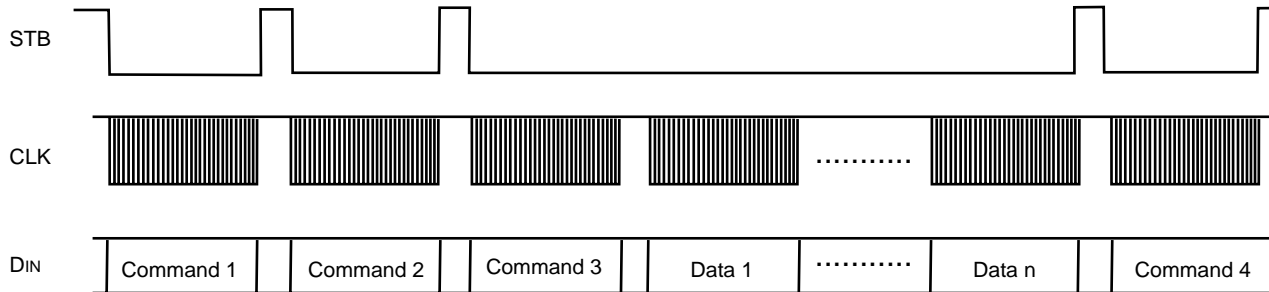
Note Refer to the **SERIAL COMMUNICATION FORMAT**.

Switching Characteristic Waveforms



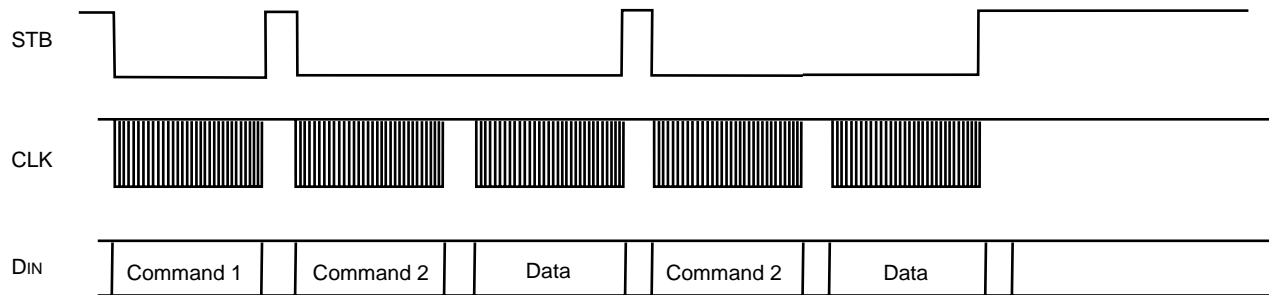
10. APPLICATIONS

Updating display memory by incrementing address



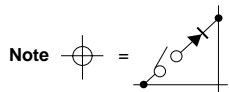
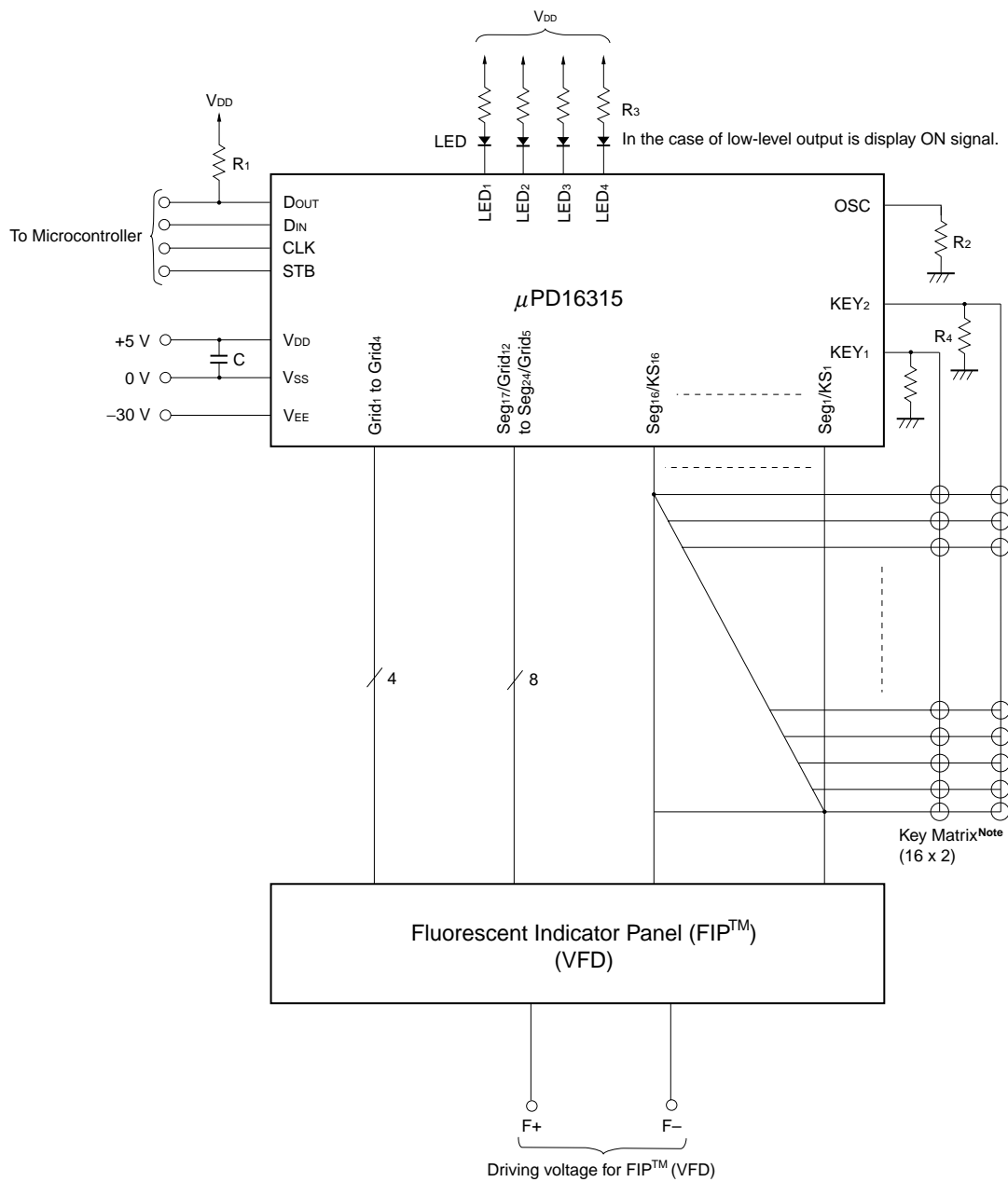
- Command 1 : sets display mode
- Command 2 : sets data
- Command 3 : sets address
- Data 1 to n : transfers display data (36 bytes MAX.)
- Command 4 : controls display

Updating specific address



- Command 1 : sets data
- Command 2 : sets address
- Data : display data

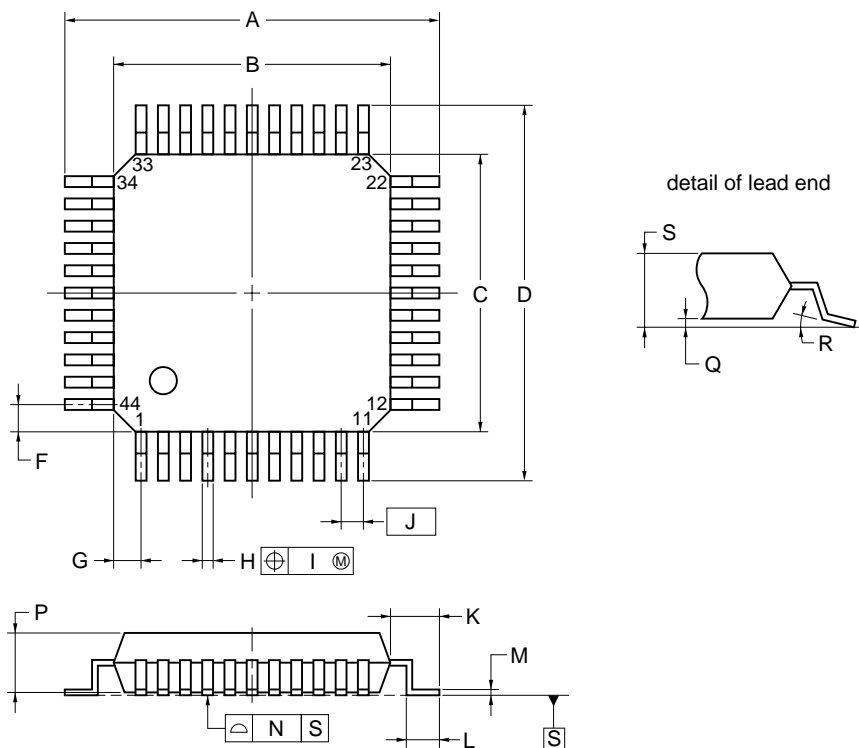
11. CIRCUIT EXAMPLE FOR APPLICATION



Remark R₁, R₄ = 1 k to 10 kΩ
 R₂ = 82 kΩ
 R₃ = 330 to 1 kΩ
 C = 0.1 μ to 1.0 μF

12. PACKAGE DRAWING

44-PIN PLASTIC QFP (10x10)



NOTE

Each lead centerline is located within 0.16 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	13.2±0.2
B	10.0±0.2
C	10.0±0.2
D	13.2±0.2
F	1.0
G	1.0
H	0.37 ^{+0.08} _{-0.07}
I	0.16
J	0.8 (T.P.)
K	1.6±0.2
L	0.8±0.2
M	0.17 ^{+0.06} _{-0.05}
N	0.10
P	2.7±0.1
Q	0.125±0.075
R	3° ^{+7°} _{-3°}
S	3.0 MAX.
S44GB-80-3BS-2	

13. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the μ PD16315.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Type of Surface Mount Device

μ PD16315GB-3BS : 44-pin plastic QFP (10 x 10)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235°C or below, Reflow time: 30 seconds or below (210°C or higher), Number of reflow process: MAX.3	IR35-00-3
VPS	Peak package's temperature: 215°C or below, Reflow time: 25 to 40 seconds (200°C or higher), Number of reflow process: MAX.3	VP15-00-3
Wave Soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or below Temperature of pre-heat: 120°C or below (Plastic surface temperature) Number of flow process: 1	WS60-00-1
Partial heating method	Terminal temperature: 300°C or below, Time 3 seconds or below (per side of pin position)	-

Caution Do not apply more than a single process at once, except for partial heating method.

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents**NEC Semiconductor Device Reliability/Quality Control System (C10983E)****Quality Grades On NEC Semiconductor Devices (C11531E)****FIP™ is a trademark of NEC Corporation**

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