NEC

MOS INTEGRATED CIRCUIT
μPD16488A

1/92 DUTY LCD CONTROLLER/DRIVER WITH FOUR-LEVEL GRAY SCALE, ON-CHIP RAM

DESCRIPTION

The μPD16488A is a controller/driver which includes display RAM for full-dot LCDs that can provide a four-level gray scale display. This IC is able to drive full-dot LCDs that contain up to 128 x 92 dots.

FEATURES

- LCD controller/driver with on-chip display RAM
- Full dot outputs: 128 segment outputs and 92 common outputs
- Can operate using single power supply (logic system) in range from 1.7 to 3.6 V.
- Selection of four levels of gray scales from among 33 possible levels (four-frame rate control + 8 pulse width modulation)
- Serial data input and 8-bit parallel data input (i80 series interface and M68 series interface)
- Dot display RAM: 128 x 128 x 2 bits
- On-chip booster: Switchable from x2 to x9 modes
- Selectable bias levels: 1/12 to 1/7 bias (normal display), 1/6 or 1/5 bias (partial display)
- Duty settings: 1/92 to 1/1 duty
- On-chip voltage divider resistor
- On-chip oscillator

ORDERING INFORMATION

Part Number	Package
μPD16488AP	Chip
μPD16488AW	Wafer

Remark Purchasing the chip/wafer entails the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representative.

Document No. S15745EJ2V0DS00 (2nd Edition)
Date Published December 2001 NS CP(K)

The mark ★ shows major revised points.

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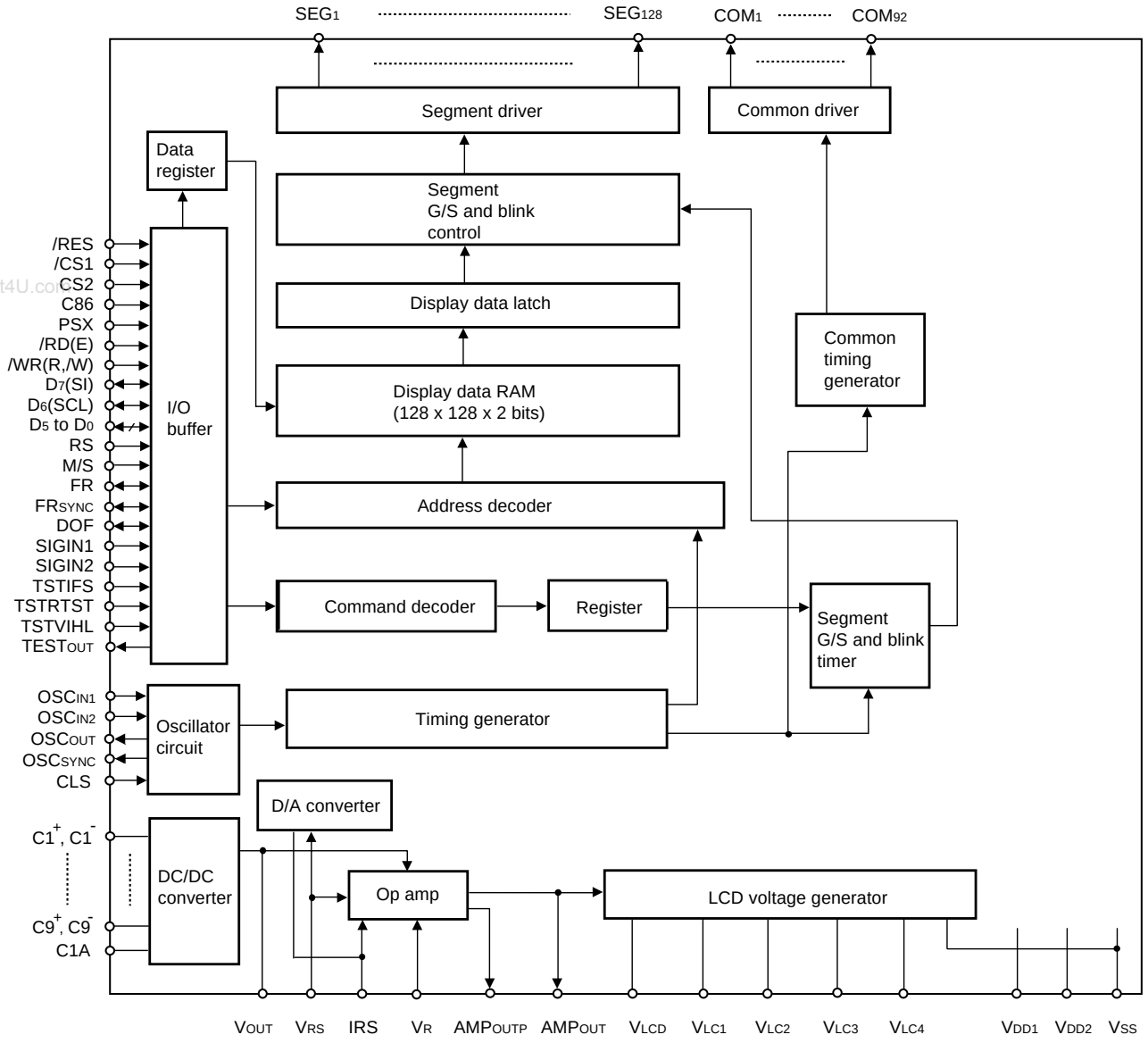
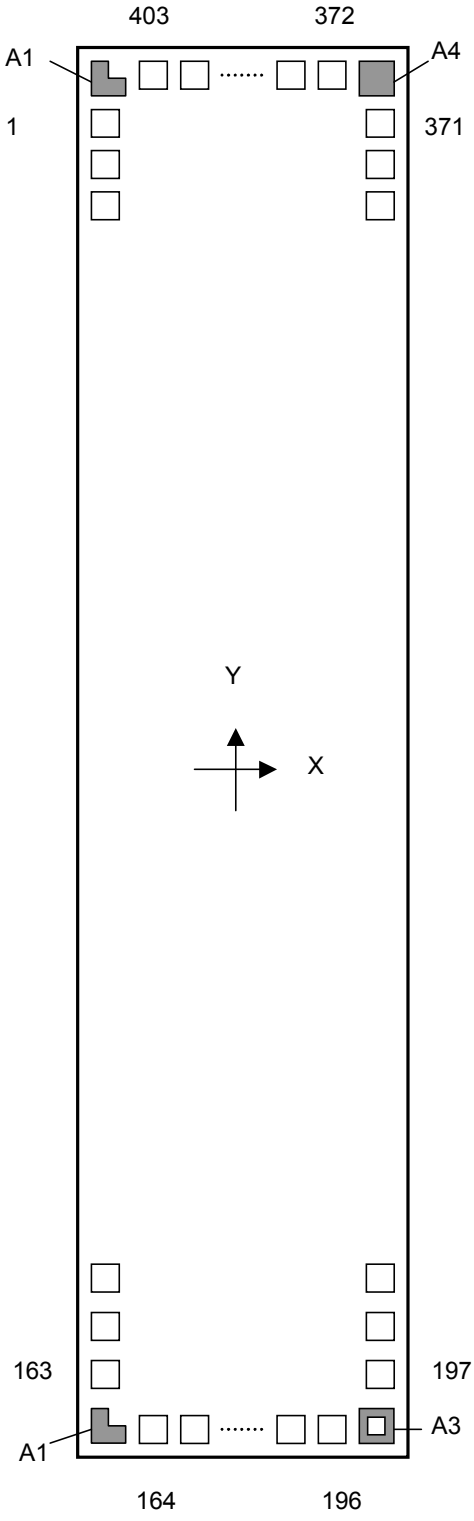
★ 1. BLOCK DIAGRAM



Remark /xxx indicates active low signals.

★ 2. PIN CONFIGURATION (PAD LAYOUT)

Chip size : 3.0 x 11.4 mm²
Chip : 485 μm TYP.



Pad type A : Pad size (Al) : 53 x 73 μm²
Bump size : 45 x 60 μm²
Bump height : 17 μm TYP.

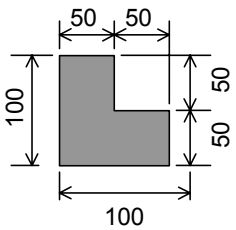
Pad type B : Pad size (Al) : 118 x 73 μm²
Bump size : 110 x 60 μm²
Bump height : 17 μm TYP.

Alignment Mark Coordinate

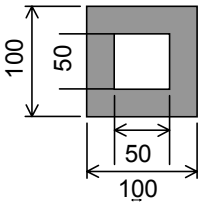
	Mark Center Coordinate	
	X [μm]	Y [μm]
M1	–1200.00	5300.00
M2	–1200.00	–5300.00
M3	1275.00	–5475.00
M4	1275.00	5475.00

Shape of Alignment Mark (unit: μm)

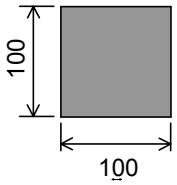
A1,A2



A3



A4



- **μPD16488A Pad Layout (1/2)**

Pad No.	Pin Name	Pad Type	Pad Coordinate X [μm]	Pad Coordinate Y [μm]
1	DUMMY	B	-1383.50	5284.00
2	DUMMY	B	-1383.50	5154.00
3	DUMMY	B	-1383.50	5024.00
4	DUMMY	B	-1383.50	4894.00
5	DUMMY	A	-1383.50	4796.50
6	VSS	A	-1383.50	4590.00
7	VRS	A	-1383.50	4530.00
8	VRS	A	-1383.50	4470.00
9	AMPOUTP	A	-1383.50	4410.00
10	AMPOUTP	A	-1383.50	4350.00
11	AMPOUT	A	-1383.50	4290.00
12	AMPOUT	A	-1383.50	4230.00
13	VR	A	-1383.50	4170.00
14	VR	A	-1383.50	4110.00
15	VLC4	A	-1383.50	4050.00
16	VLC4	A	-1383.50	3990.00
17	VLC3	A	-1383.50	3930.00
18	VLC3	A	-1383.50	3870.00
19	VLC2	A	-1383.50	3810.00
20	VLC2	A	-1383.50	3750.00
21	VLC1	A	-1383.50	3690.00
22	VLC1	A	-1383.50	3630.00
23	VLCD	A	-1383.50	3570.00
24	VLCD	A	-1383.50	3510.00
25	VSS	A	-1383.50	3450.00
26	VOUT	A	-1383.50	3390.00
27	VOUT	A	-1383.50	3330.00
28	VSS	A	-1383.50	3270.00
29	C9-	A	-1383.50	3210.00
30	C9-	A	-1383.50	3150.00
31	C9+	A	-1383.50	3090.00
32	C9+	A	-1383.50	3030.00
33	C8-	A	-1383.50	2970.00
34	C8-	A	-1383.50	2910.00
35	C8+	A	-1383.50	2850.00
36	C8+	A	-1383.50	2790.00
37	C7-	A	-1383.50	2730.00
38	C7-	A	-1383.50	2670.00
39	C7+	A	-1383.50	2610.00
40	C7+	A	-1383.50	2550.00
41	C6-	A	-1383.50	2490.00
42	C6-	A	-1383.50	2430.00
43	C6+	A	-1383.50	2370.00
44	C6+	A	-1383.50	2310.00
45	C5-	A	-1383.50	2250.00
46	C5-	A	-1383.50	2190.00
47	C5+	A	-1383.50	2130.00
48	C5+	A	-1383.50	2070.00
49	C4-	A	-1383.50	2010.00
50	C4-	A	-1383.50	1950.00
51	C4+	A	-1383.50	1890.00
52	C4+	A	-1383.50	1830.00
53	C3-	A	-1383.50	1770.00
54	C3-	A	-1383.50	1710.00
55	C3+	A	-1383.50	1650.00
56	C3+	A	-1383.50	1590.00
57	C2-	A	-1383.50	1530.00
58	C2-	A	-1383.50	1470.00
59	C2+	A	-1383.50	1410.00
60	C2+	A	-1383.50	1350.00
61	C1-	A	-1383.50	1290.00
62	C1-	A	-1383.50	1230.00
63	C1+	A	-1383.50	1170.00
64	C1+	A	-1383.50	1110.00
65	C1A	A	-1383.50	1050.00
66	C1A	A	-1383.50	990.00
67	VDD2	A	-1383.50	930.00
68	VDD2	A	-1383.50	870.00
69	VDD2	A	-1383.50	810.00
70	VDD1	A	-1383.50	750.00
71	VDD1	A	-1383.50	690.00
72	VDD1	A	-1383.50	630.00
73	VSS	A	-1383.50	570.00
74	VSS	A	-1383.50	510.00
75	VSS	A	-1383.50	450.00
76	CLS	A	-1383.50	390.00
77	CLS	A	-1383.50	330.00
78	VDD1	A	-1383.50	270.00
79	M/S	A	-1383.50	210.00
80	M/S	A	-1383.50	150.00
81	VSS	A	-1383.50	90.00
82	C86	A	-1383.50	30.00
83	C86	A	-1383.50	-30.00
84	PSX	A	-1383.50	-90.00
85	PSX	A	-1383.50	-150.00
86	VDD1	A	-1383.50	-210.00
87	IRS	A	-1383.50	-270.00
88	IRS	A	-1383.50	-330.00
89	VSS	A	-1383.50	-390.00
90	/CS1	A	-1383.50	-450.00
91	/CS1	A	-1383.50	-510.00
92	CS2	A	-1383.50	-570.00
93	CS2	A	-1383.50	-630.00
94	VDD1	A	-1383.50	-690.00
95	/RES	A	-1383.50	-750.00
96	/RES	A	-1383.50	-810.00
97	RS	A	-1383.50	-870.00
98	RS	A	-1383.50	-930.00
99	VSS	A	-1383.50	-990.00
100	/WR (R,/W)	A	-1383.50	-1050.00
101	/WR (R,/W)	A	-1383.50	-1110.00
102	/RD (E)	A	-1383.50	-1170.00
103	/RD (E)	A	-1383.50	-1230.00
104	VDD1	A	-1383.50	-1290.00
105	D7	A	-1383.50	-1350.00
106	D7	A	-1383.50	-1410.00
107	D6	A	-1383.50	-1470.00
108	D6	A	-1383.50	-1530.00
109	DUMMY	A	-1383.50	-1590.00
110	D5	A	-1383.50	-1650.00
111	D5	A	-1383.50	-1710.00
112	D4	A	-1383.50	-1770.00
113	D4	A	-1383.50	-1830.00
114	DUMMY	A	-1383.50	-1890.00
115	D3	A	-1383.50	-1950.00
116	D3	A	-1383.50	-2010.00
117	D2	A	-1383.50	-2070.00
118	D2	A	-1383.50	-2130.00
119	DUMMY	A	-1383.50	-2190.00
120	D1	A	-1383.50	-2250.00
121	D1	A	-1383.50	-2310.00
122	D0	A	-1383.50	-2370.00
123	D0	A	-1383.50	-2430.00
124	DUMMY	A	-1383.50	-2490.00
125	FRSYNC	A	-1383.50	-2550.00
126	FRSYNC	A	-1383.50	-2610.00
127	FR	A	-1383.50	-2670.00
128	FR	A	-1383.50	-2730.00
129	DUMMY	A	-1383.50	-2790.00
130	DOF	A	-1383.50	-2850.00
131	DOF	A	-1383.50	-2910.00
132	OSCIN1	A	-1383.50	-2970.00
133	OSCIN1	A	-1383.50	-3030.00
134	OSCIN2	A	-1383.50	-3090.00
135	OSCIN2	A	-1383.50	-3150.00
136	OSCOUT	A	-1383.50	-3210.00
137	OSCOUT	A	-1383.50	-3270.00
138	DUMMY	A	-1383.50	-3330.00
139	OSCSYNC	A	-1383.50	-3390.00
140	OSCSYNC	A	-1383.50	-3450.00
141	DUMMY	A	-1383.50	-3510.00
142	DUMMY	A	-1383.50	-3570.00
143	VSS	A	-1383.50	-3630.00
144	SIGIN1	A	-1383.50	-3690.00
145	SIGIN1	A	-1383.50	-3750.00
146	VDD1	A	-1383.50	-3810.00
147	SIGIN2	A	-1383.50	-3870.00
148	SIGIN2	A	-1383.50	-3930.00
149	VSS	A	-1383.50	-3990.00
150	TESTOUT	A	-1383.50	-4050.00
151	TESTOUT	A	-1383.50	-4110.00
152	TSTIFS	A	-1383.50	-4170.00
153	TSTIFS	A	-1383.50	-4230.00
154	TSTRTST	A	-1383.50	-4290.00
155	TSTRTST	A	-1383.50	-4350.00
156	TSTVIHL	A	-1383.50	-4410.00
157	TSTVIHL	A	-1383.50	-4470.00
158	VSS	A	-1383.50	-4530.00
159	DUMMY	A	-1383.50	-4796.50
160	DUMMY	B	-1383.50	-4894.00
161	DUMMY	B	-1383.50	-5024.00
162	DUMMY	B	-1383.50	-5154.00
163	DUMMY	B	-1383.50	-5284.00
164	DUMMY	B	-1172.50	-5474.76
165	DUMMY	A	-1075.00	-5474.76
166	COM47	A	-965.00	-5474.76
167	COM48	A	-905.00	-5474.76
168	COM49	A	-845.00	-5474.76
169	COM50	A	-785.00	-5474.76
170	COM51	A	-725.00	-5474.76
171	COM52	A	-665.00	-5474.76
172	COM53	A	-605.00	-5474.76
173	COM54	A	-545.00	-5474.76
174	COM55	A	-485.00	-5474.76
175	COM56	A	-425.00	-5474.76
176	COM57	A	-365.00	-5474.76
177	COM58	A	-305.00	-5474.76
178	COM59	A	-245.00	-5474.76
179	COM60	A	-185.00	-5474.76
180	COM61	A	-125.00	-5474.76
181	COM62	A	-65.00	-5474.76
182	COM63	A	-5.00	-5474.76
183	COM64	A	55.00	-5474.76
184	COM65	A	115.00	-5474.76
185	COM66	A	175.00	-5474.76
186	COM67	A	235.00	-5474.76
187	COM68	A	295.00	-5474.76
188	COM69	A	355.00	-5474.76
189	COM70	A	415.00	-5474.76
190	COM71	A	475.00	-5474.76
191	COM72	A	535.00	-5474.76
192	COM73	A	595.00	-5474.76
193	DUMMY	A	655.00	-5474.76
194	DUMMY	B	771.00	-5474.76
195	DUMMY	B	906.00	-5474.76
196	DUMMY	B	1041.00	-5474.76
197	DUMMY	B	1274.76	-5257.50
198	DUMMY	A	1274.76	-5160.00
199	DUMMY	A	1274.76	-5100.00
200	COM74	A	1274.76	-5040.00
201	COM75	A	1274.76	-4980.00
202	COM76	A	1274.76	-4920.00
203	COM77	A	1274.76	-4860.00
204	COM78	A	1274.76	-4800.00
205	COM79	A	1274.76	-4740.00
206	COM80	A	1274.76	-4680.00
207	COM81	A	1274.76	-4620.00
208	COM82	A	1274.76	-4560.00
209	COM83	A	1274.76	-4500.00
210	COM84	A	1274.76	-4440.00

- **μPD16488A Pad Layout (2/2)**

Pad No.	Pin Name	Pad Type	Pad Coordinate X [μm]	Pad Coordinate Y [μm]
211	COM85	A	1274.76	-4380.00
212	COM86	A	1274.76	-4320.00
213	COM87	A	1274.76	-4260.00
214	COM88	A	1274.76	-4200.00
215	COM89	A	1274.76	-4140.00
216	COM90	A	1274.76	-4080.00
217	COM91	A	1274.76	-4020.00
218	COM92	A	1274.76	-3960.00
219	DUMMY	A	1274.76	-3900.00
220	SEG128	A	1274.76	-3840.00
221	SEG127	A	1274.76	-3780.00
222	SEG126	A	1274.76	-3720.00
223	SEG125	A	1274.76	-3660.00
224	SEG124	A	1274.76	-3600.00
225	SEG123	A	1274.76	-3540.00
226	SEG122	A	1274.76	-3480.00
227	SEG121	A	1274.76	-3420.00
228	SEG120	A	1274.76	-3360.00
229	SEG119	A	1274.76	-3300.00
230	SEG118	A	1274.76	-3240.00
231	SEG117	A	1274.76	-3180.00
232	SEG116	A	1274.76	-3120.00
233	SEG115	A	1274.76	-3060.00
234	SEG114	A	1274.76	-3000.00
235	SEG113	A	1274.76	-2940.00
236	SEG112	A	1274.76	-2880.00
237	SEG111	A	1274.76	-2820.00
238	SEG110	A	1274.76	-2760.00
239	SEG109	A	1274.76	-2700.00
240	SEG108	A	1274.76	-2640.00
241	SEG107	A	1274.76	-2580.00
242	SEG106	A	1274.76	-2520.00
243	SEG105	A	1274.76	-2460.00
244	SEG104	A	1274.76	-2400.00
245	SEG103	A	1274.76	-2340.00
246	SEG102	A	1274.76	-2280.00
247	SEG101	A	1274.76	-2220.00
248	SEG100	A	1274.76	-2160.00
249	SEG99	A	1274.76	-2100.00
250	SEG98	A	1274.76	-2040.00
251	SEG97	A	1274.76	-1980.00
252	SEG96	A	1274.76	-1920.00
253	SEG95	A	1274.76	-1860.00
254	SEG94	A	1274.76	-1800.00
255	SEG93	A	1274.76	-1740.00
256	SEG92	A	1274.76	-1680.00
257	SEG91	A	1274.76	-1620.00
258	SEG90	A	1274.76	-1560.00
259	SEG89	A	1274.76	-1500.00
260	SEG88	A	1274.76	-1440.00
261	SEG87	A	1274.76	-1380.00
262	SEG86	A	1274.76	-1320.00
263	SEG85	A	1274.76	-1260.00
264	SEG84	A	1274.76	-1200.00
265	SEG83	A	1274.76	-1140.00
266	SEG82	A	1274.76	-1080.00
267	SEG81	A	1274.76	-1020.00
268	SEG80	A	1274.76	-960.00
269	SEG79	A	1274.76	-900.00
270	SEG78	A	1274.76	-840.00
271	SEG77	A	1274.76	-780.00
272	SEG76	A	1274.76	-720.00
273	SEG75	A	1274.76	-660.00
274	SEG74	A	1274.76	-600.00
275	SEG73	A	1274.76	-540.00
276	SEG72	A	1274.76	-480.00
277	SEG71	A	1274.76	-420.00
278	SEG70	A	1274.76	-360.00
279	SEG69	A	1274.76	-300.00
280	SEG68	A	1274.76	-240.00
281	SEG67	A	1274.76	-180.00
282	SEG66	A	1274.76	-120.00
283	SEG65	A	1274.76	-60.00
284	SEG64	A	1274.76	0.00
285	SEG63	A	1274.76	60.00
286	SEG62	A	1274.76	120.00
287	SEG61	A	1274.76	180.00
288	SEG60	A	1274.76	240.00
289	SEG59	A	1274.76	300.00
290	SEG58	A	1274.76	360.00
291	SEG57	A	1274.76	420.00
292	SEG56	A	1274.76	480.00
293	SEG55	A	1274.76	540.00
294	SEG54	A	1274.76	600.00
295	SEG53	A	1274.76	660.00
296	SEG52	A	1274.76	720.00
297	SEG51	A	1274.76	780.00
298	SEG50	A	1274.76	840.00
299	SEG49	A	1274.76	900.00
300	SEG48	A	1274.76	960.00
301	SEG47	A	1274.76	1020.00
302	SEG46	A	1274.76	1080.00
303	SEG45	A	1274.76	1140.00
304	SEG44	A	1274.76	1200.00
305	SEG43	A	1274.76	1260.00
306	SEG42	A	1274.76	1320.00
307	SEG41	A	1274.76	1380.00
308	SEG40	A	1274.76	1440.00
309	SEG39	A	1274.76	1500.00
310	SEG38	A	1274.76	1560.00
311	SEG37	A	1274.76	1620.00
312	SEG36	A	1274.76	1680.00
313	SEG35	A	1274.76	1740.00
314	SEG34	A	1274.76	1800.00
315	SEG33	A	1274.76	1860.00
316	SEG32	A	1274.76	1920.00
317	SEG31	A	1274.76	1980.00
318	SEG30	A	1274.76	2040.00
319	SEG29	A	1274.76	2100.00
320	SEG28	A	1274.76	2160.00
321	SEG27	A	1274.76	2220.00
322	SEG26	A	1274.76	2280.00
323	SEG25	A	1274.76	2340.00
324	SEG24	A	1274.76	2400.00
325	SEG23	A	1274.76	2460.00
326	SEG22	A	1274.76	2520.00
327	SEG21	A	1274.76	2580.00
328	SEG20	A	1274.76	2640.00
329	SEG19	A	1274.76	2700.00
330	SEG18	A	1274.76	2760.00
331	SEG17	A	1274.76	2820.00
332	SEG16	A	1274.76	2880.00
333	SEG15	A	1274.76	2940.00
334	SEG14	A	1274.76	3000.00
335	SEG13	A	1274.76	3060.00
336	SEG12	A	1274.76	3120.00
337	SEG11	A	1274.76	3180.00
338	SEG10	A	1274.76	3240.00
339	SEG9	A	1274.76	3300.00
340	SEG8	A	1274.76	3360.00
341	SEG7	A	1274.76	3420.00
342	SEG6	A	1274.76	3480.00
343	SEG5	A	1274.76	3540.00
344	SEG4	A	1274.76	3600.00
345	SEG3	A	1274.76	3660.00
346	SEG2	A	1274.76	3720.00
347	SEG1	A	1274.76	3780.00
348	DUMMY	A	1274.76	3840.00
349	DUMMY	A	1274.76	3900.00
350	COM46	A	1274.76	3960.00
351	COM45	A	1274.76	4020.00
352	COM44	A	1274.76	4080.00
353	COM43	A	1274.76	4140.00
354	COM42	A	1274.76	4200.00
355	COM41	A	1274.76	4260.00
356	COM40	A	1274.76	4320.00
357	COM39	A	1274.76	4380.00
358	COM38	A	1274.76	4440.00
359	COM37	A	1274.76	4500.00
360	COM36	A	1274.76	4560.00
361	COM35	A	1274.76	4620.00
362	COM34	A	1274.76	4680.00
363	COM33	A	1274.76	4740.00
364	COM32	A	1274.76	4800.00
365	COM31	A	1274.76	4860.00
366	COM30	A	1274.76	4920.00
367	COM29	A	1274.76	4980.00
368	COM28	A	1274.76	5040.00
369	DUMMY	A	1274.76	5100.00
370	DUMMY	A	1274.76	5160.00
371	DUMMY	B	1274.76	5257.50
372	DUMMY	B	1041.00	5474.76
373	DUMMY	B	906.00	5474.76
374	DUMMY	B	771.00	5474.76
375	COM27	A	595.00	5474.76
376	COM26	A	535.00	5474.76
377	COM25	A	475.00	5474.76
378	COM24	A	415.00	5474.76
379	COM23	A	355.00	5474.76
380	COM22	A	295.00	5474.76
381	COM21	A	235.00	5474.76
382	COM20	A	175.00	5474.76
383	COM19	A	115.00	5474.76
384	COM18	A	55.00	5474.76
385	COM17	A	-5.00	5474.76
386	COM16	A	-65.00	5474.76
387	COM15	A	-125.00	5474.76
388	COM14	A	-185.00	5474.76
389	COM13	A	-245.00	5474.76
390	COM12	A	-305.00	5474.76
391	COM11	A	-365.00	5474.76
392	COM10	A	-425.00	5474.76
393	COM9	A	-485.00	5474.76
394	COM8	A	-545.00	5474.76
395	COM7	A	-605.00	5474.76
396	COM6	A	-665.00	5474.76
397	COM5	A	-725.00	5474.76
398	COM4	A	-785.00	5474.76
399	COM3	A	-845.00	5474.76
400	COM2	A	-905.00	5474.76
401	COM1	A	-965.00	5474.76
402	DUMMY	A	-1075.00	5474.76
403	DUMMY	B	-1172.50	5474.76

3. PIN FUNCTIONS

3.1 Power Supply System Pins

Symbol	Name	Pad No.	I/O	Description
V_{DD1}	Logic power supply pin	70-72, 78, 86, 94, 104, 146	–	Power supply pin for logic circuit
V_{DD2}	Boost circuit power supply pin	67-69	–	Power supply pin for booster
V_{SS}	Logic and driver ground pin	6, 25, 28, 73 to 75, 81, 89, 99, 143, 149, 158	–	Ground pin for logic and driver circuits
V_{OUT}	Driver power supply pin	26, 27	–	Power supply pin for driver. Output pin for on-chip booster. Connect a 1 μF boost capacitor between this pin and the GND pin. If not using the on-chip booster, a direct driver power supply can be input.
V_{LCD}, V_{LC1} to V_{LC4}	Reference power supply pins for driver	24, 23, 22 to 15	–	These are reference power supply pins for the LCD driver. Connect a capacitor between these pins and the GND pin if an internal bias has been selected.
$C1^+$, $C1^-$ $C2^+$, $C2^-$ $C3^+$, $C3^-$ $C4^+$, $C4^-$ $C5^+$, $C5^-$ $C6^+$, $C6^-$ $C7^+$, $C7^-$ $C8^+$, $C8^-$ $C9^+$, $C9^-$	Boost capacitor connection pins (1)	64, 63, 62, 61 60, 59, 58, 57 56, 55, 54, 53 52, 51, 50, 49 48, 47, 46, 45 44, 43, 42, 41 40, 39, 38, 37 36, 35, 34, 33 32, 31, 30, 29	–	These are capacitor connection pins for the booster. When using the on-chip booster, connect a 1 μF capacitor between positive (+) and negative (-) pins.
C1A	Boost capacitor connection pin (2)	65, 66	–	This is a capacitor connection pin for boost adjustment. When using the on-chip booster, connect a 1 μF capacitor between this pin and the GND pin.

3.2 Logic System Pins

(1/3)

Symbol	Name	Pad No.	I/O	Description
PSX	Data transfer selection	84, 85	Input	This pin is used to select between parallel data input and serial data input. PSX = H: Parallel data input PSX = L: Serial data input
/CS1, CS2	Chip select	90, 91, 92, 93	Input	These pins are used for chip select signals. When /CS1 = L (CS2 = H), the chip is active and can perform data input/output operations including command and data I/O.
/RD (E)	Read (enable)	102, 103	Input	When i80 series parallel data transfer (/RD) has been selected, the signal at this pin is used to enable read operations. Data is output to the data bus only when this pin is L. When M68 series parallel data transfer (E) has been selected, the signal at this pin is used to enable write operations. Data is written at the falling edge of this signal.
/WR (R,/W)	Write (read/write)	100, 101	Input	When i80 series parallel data transfer (/WR) has been selected, the signal at this pin is used to enable write operations. Data is written at the rising edge of this signal. When 68 series parallel data transfer (R,/W) has been selected, this pin is used to determine the direction of data transfer. L: Write H: Read
C86	Interface selection	82, 83	Input	This pin is used to switch between interface modes (i80 series CPU or M68 series CPU). L: Selects i80 series CPU mode H: Selects M68 series CPU mode
D_0 to D_5, D_6 (SCL) D_7 (SI)	Data bus (serial clock) (serial input)	105 to 108, 110 to 113, 115 to 118, 120 to 123	I/O	These pins comprise an 8-bit bidirectional data bus that connects to an 8-bit or 16-bit standard CPU bus. When the serial interface has been selected (PSX = L), D_6 functions as a serial clock input pin (SCL) and D_7 functions as a serial data input pin (SI). In either case, pins D_0 to D_5 are in high impedance mode. When the chip is not selected, D_0 to D_7 are in high impedance mode.
RS	Index register/data, command selection	97, 98	Input	Usually, this pin is connected to the LSB of the standard CPU address bus and is used to distinguish between data from index registers and data/commands. RS = H: Indicates that data from D_0 to D_7 is data/command RS = L : Indicates that data from D_0 to D_7 is index register contents
/RES	Reset	95, 96	Input	When /RES is low, an internal reset is performed. The reset operation is executed at the /RES signal level.

(2/3)

Symbol	Name	Pad No.	I/O	Description
CLS	Select clock division	76, 77	Input	This pin is used to select whether or not to use the divider within the display clock oscillator. CLS = H: Use divider CLS = L: Do not use divider When using an external clock, the CLS = L setting is input via the OSC_{IN1} and OSC_{IN2} pins as normal and partial clocks respectively. When CLS = H, clock input is via the OSC_{IN1} pin only.
FR	Frame signal	127, 128	I/O	This pin is used as I/O pin for the LCD's AC conversion signal. M/S = H: Output M/S = L: Input When using the μPD16488A in master/slave mode, both FR pins must be connected.
FR_{SYNC}	Frame synchronization signal	125, 126	I/O	This pin is used as I/O pin for the LCD's AC conversion synchronization signal. M/S = H: Output M/S = L: Input When the μPD16488A is used in master/slave mode, both FR_{SYNC} pins must be connected.
DOF	Display blink	130, 131	I/O	This pin is used to control the LCD's display blink function. M/S = H: Output M/S = L: Input When the μPD16488A is used in master/slave mode, both DOF pins must be connected.
M/S	Master/slave	79, 80	Input	This pin is used to select between master and slave operation modes. In master operation mode, it outputs the timing signal required by the LCD driver and in slave operation mode it inputs this timing signal from an external source for use in LCD display synchronization. M/S = H: Master operation mode M/S = L: Slave operation mode Settings dependent on the M/S mode are listed in the following chart.
IRS	V_{LCD} regulation	87, 88	Input	This pin is used to select the resistor that is used for V_{LCD} voltage regulation. IRS = H: Uses internal resistor IRS = L: Does not use internal resistor. The V_{LCD} voltage level is regulated using the external voltage division resistor that is connected to the V_R pin. This pin is valid only in master operation mode. In slave operation mode, this pin is fixed high or low level.
SIGIN1, SIGIN2	Signature setting pins	144, 145, 147, 148	Input	These pins can be used to set a unique signature for the IC. The signal set via these pins can subsequently be read from the signature read register (R45).

M/S	Power supply circuit	FR	FR_{SYNC}	DOF
H	Valid	Output	Output	Output
L	Invalid	Input	Input	Input

(3/3)

Symbol	Name	Pad No.	I/O	Description
OSC_{IN1}	Oscillation signal pins	132, 133	Input	A resistor can be inserted between OSC_{IN1}-OSC_{OUT}, and OSC_{IN2}-OSC_{OUT}. When using an external oscillator, a clock signal is input via the OSC_{IN} pins according to the CLS pin's status and the OSC_{OUT} pin is left unconnected. The wiring between OSC_{IN1}-OSC_{OUT} and OSC_{IN2}-OSC_{OUT} must be as short as possible, and use after proper evaluation.
OSC_{IN2}		134, 135	Input	
OSC_{OUT}		136, 137	Output	
OSC_{SYNC}	Display clock output	139, 140	Output	Display clock output pin. See **5. 4 Oscillator** concerning use or this pin when the μPD16488A is in master or slave operation mode.

3.3 Driver-Related Pins

Symbol	Name	Pad No.	I/O	Description
SEG_1 to SEG_{128}	Segment	347-220	Output	Segment output pins
COM_1 to COM_{92}	Common	166 to 192, 200 to 218, 350 to 368, 375 to 401	Output	Common output pins
V_{RS}	Op amp input pin for regulating the driving voltage of the LCD	7, 8	Input	V_{RS} is an op amp input pin for regulating the driving voltage of the LCD. This is a reference voltage input for the LCD voltage regulation amplifier. When using the internal drive circuit (i.e., when OP1 = 1), we recommend inserting a 0.1 to 1 μF capacitor between this pin and GND.
V_R	Input pin for the op amp's feedback connection	13, 14	Input	V_R is an input for the op amp's feedback connection. Insert this pin between GND and AMP_{OUT} when using the feedback resistor for this input. This pin is valid only when not using an internal resistor for V_{LCD} voltage regulation (i.e., when IRS = L). This pin cannot be used when using the internal resistor for V_{LCD} voltage regulation (i.e., when IRS = H).
AMP_{OUT}	Op amp output	9, 10	Output	These are op amp output pins for regulating the driving voltage of the LCD. When not using an internal resistor for V_{LCD} voltage regulation (i.e., when IRS = L), these outputs are connected to the LCD drive voltage regulation resistor (see **5.6.2 Voltage regulator**). We recommend inserting a 0.01 to 0.1 μF capacitor between these pins in order to stabilize the internal op amp's output.
AMP_{OUTP}		11, 12		
DUMMY	Dummy pin	1 to 5, 109, 114, 119, 124, 129, 138, 141, 142, 159 to 165, 193 to 199, 219, 348, 349, 369 to 374, 402, 403	–	Dummy pin. These pins are not connected inside IC. Usually, leave these pins open.

3.4 Test Pins

Symbol	Name	Pad No.	I/O	Description
TSTIFS TSTRTST TSTVIHL	Test input	152, 153, 154, 155, 156, 157	Input	These pins are used to set a test mode for the IC. Normally, connect these pins to V_{SS}.
$TEST_{OUT}$	Test output	150, 151	Output	These pins are used when the IC is in test mode. Usually, leave them open.

4. PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The I/O circuit type of each pin and recommended connection of unused pins are described below.

Pin Name	Input Type	Input/output	Recommended Connection of Unused Pins	Notes
PSX	Schmitt trigger	Input	Mode setting pin.	**Note 1**
/CS1	Filter	Input	Connect to V_{SS}.	–
CS2	Filter	Input	Connect to V_{DD1}.	–
/RD(E)	Filter	Input	Connect to V_{DD1} (i80 series interface), connect to V_{DD1} or V_{SS} (serial interface).	–
/WR(R,/W)	Filter	Input	Connect to V_{DD1} or V_{SS} (serial interface).	–
C86	Schmitt trigger	Input	Mode setting pin.	**Note 1**
D_0 to D_5	Filter	Input/output	Leave open	–
D_6(SCL)	Filter	Input/output	–	–
D_7(SI)	Filter	Input/output	–	–
RS	Filter	Input	Register setting pin.	**Note 2**
/RES	Schmitt trigger	Input	Connect to V_{DD1}.	–
CLS	Schmitt trigger	Input	Mode setting pin	**Note 1**
FR	CMOS	Input/output	Leave open (using master mode, M/S = H).	–
FR_{SYNC}	CMOS	Input/output	Leave open (using master mode, M/S = H).	–
DOF	CMOS	Input/output	Leave open (using master mode, M/S = H).	–
M/S	Schmitt trigger	Input	Mode setting pin.	**Note 1**
IRS	Schmitt trigger	Input	Mode setting pin.	**Note 1**
SIGIN1	Schmitt trigger	Input	Connect to V_{DD1} or V_{SS}.	–
SIGIN2	Schmitt trigger	Input	Connect to V_{DD1} or V_{SS}.	–
OSC_{IN1}	Schmitt trigger	Input	–	–
OSC_{IN2}	Schmitt trigger	Input	Connect to V_{DD1} or V_{SS} (CLS = H)	–
OSC_{OUT}	–	Output	Leave open (when using external clock)	–
OSC_{SYNC}	–	Output	Leave open	–
TSTIFS	Schmitt trigger	Input	Connect to V_{SS} (during normal use)	–
TSTRTST	Schmitt trigger	Input	Connect to V_{SS} (during normal use)	–
TSTVIHL	Schmitt trigger	Input	Connect to V_{SS} (during normal use)	–
$TEST_{OUT}$	–	Output	Leave open	

Notes 1. Connect to either V_{DD1} or V_{SS}, depending on the mode setting.

2. Input either V_{DD1} or V_{SS} output from CPU, depending on the mode setting.

5. DESCRIPTION OF FUNCTIONS

5.1 CPU Interface

5.1.1 Selection of interface type

The μPD16488A chip transfers data using an 8-bit bidirectional data bus (D_7 to D_0) or a serial data input (SI). Setting the polarity of the PSX pin as either H (high) or L (low) selects between 8-bit parallel or serial data input, as shown in the following table.

PSX	CS	RS	/RD	/WR	C86	D_7	D_6	D_5 to D0
H: Parallel input	CS	RS	/RD	/WR	C86	D_7	D_6	D_5 to D0
L: Serial input	CS	RS	**Note1**	**Note1**	**Note1**	SI	SCL	Hi-Z **Note2**

Notes 1. Fixed as either High or Low.

2. Hi-Z: High impedance

5.1.2 Parallel interface

When the parallel interface has been selected (PSX = H), setting the C86 pin as either H or L enables a direct connection to an i80 series or M68 series CPU (see table below).

C86	/CS1	CS2	RS	/RD	/WR	D_7 to D_0
H: M68 series CPU	/CS1	CS2	RS	E	R,/W	D_7 to D_0
L: i80 series CPU	/CS1	CS2	RS	/RD	/WR	D_7 to D_0

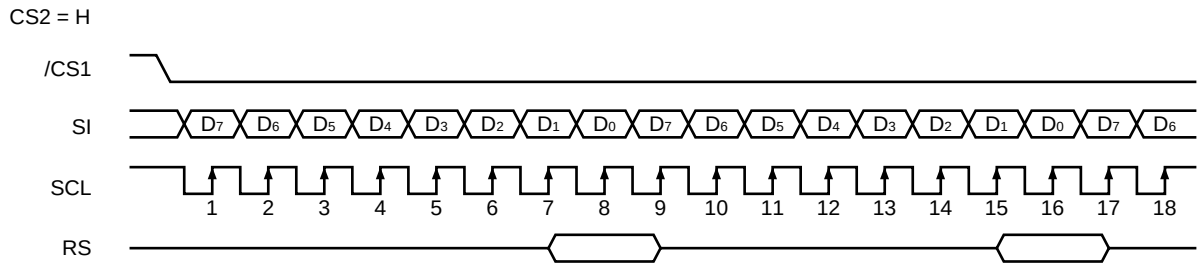
The data bus signal is identified according to the combination of the RS, /RD(E), and /WR(R,/W) signals, as shown in the following table.

Common	M68	i80		Function
RS	R,/W	/RD	/WR	
1	1	0	1	Reads display data and registers
1	0	1	0	Writes display data and registers
0	1	0	1	Prohibited
★ 0	0	1	0	Writes to index register

5.1.3 Serial interface

When the serial interface has been selected (PSX = L), if the chip is active (/CS1 = L, CS2 = H), serial data input (SI) and serial clock input (SCL) can be received. Serial data is read from D_7 and then from D_6 to D_0 on the rising edge of the serial clock, via the serial input pin. This data is synchronized on the eighth serial clock's rising edge and is then converted to parallel data for processing. RS input is used to judge serial input data as display data or command data: when RS = H the data is display/command data and when RS = L the data is index data. When the chip enters active mode, RS input is read at the rising edge after every eighth serial clock and is then used to judge the serial input data. The serial interface signal chart is shown below.

Figure 5-1. Serial Interface Signal Chart



Remarks 1. If the chip is not active, the shift register and counter are reset to their initial settings.

2. The data read function is disabled during serial interface mode.

3. When using SCL wiring, take care concerning the possible effects of terminating reflection and noise from external sources. We recommend checking operation with the actual device.

5.1.4 Chip select

The μPD16488A has two chip select pins (/CS1 and CS2). The CPU parallel interface or serial interface can be used only when /CS1 = L and CS2 = H. When chip select is inactive, P_0 to P_7 are set to high impedance (invalid) and input of RS, /RD, or /WR is not active. If serial interface mode has been set, the shift register and counter are both reset.

5.1.5 Display data RAM and on-chip register access

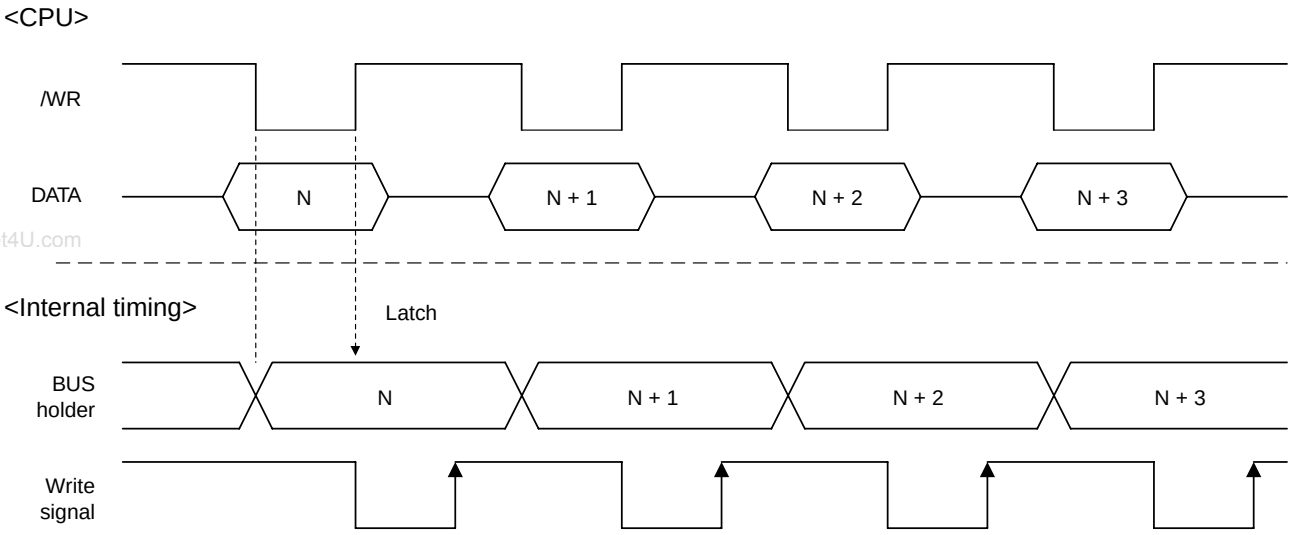
Because only the required cycle time (t_{cyc}) is satisfied when accessing the μPD16488A from the CPU, high-speed data transfer is possible. There is no need to consider any wait time. No dummy data is needed when writing data. Even when data is read, there is no need for dummy data except in the display memory access register (R11).

In other words, dummy data is required only when reading data from the display memory access register (R11).

Figure 5-2 illustrates this relationship.

Figure 5-2. Write and Read (1/2)

Write



Read (display memory access register (R11))

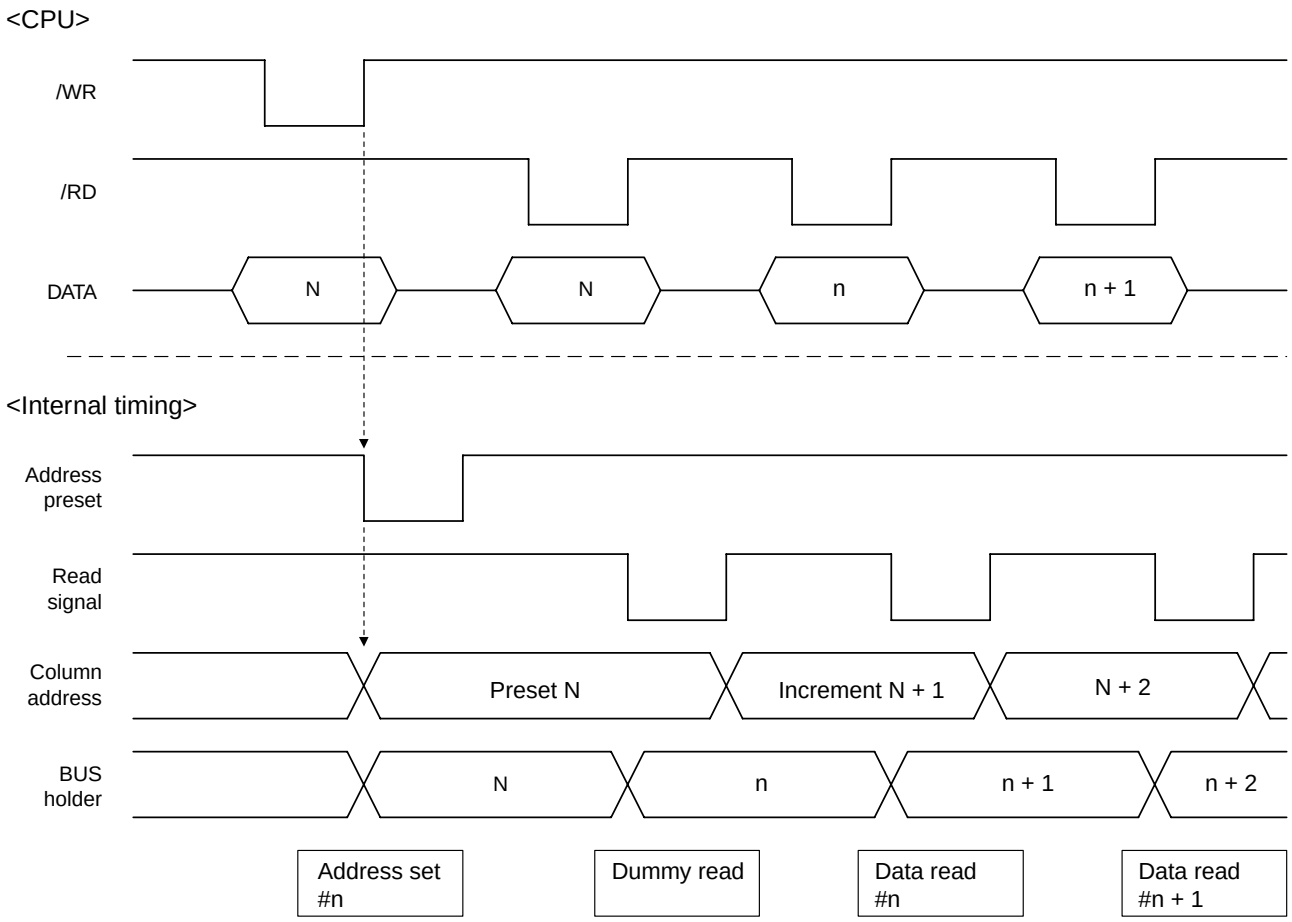
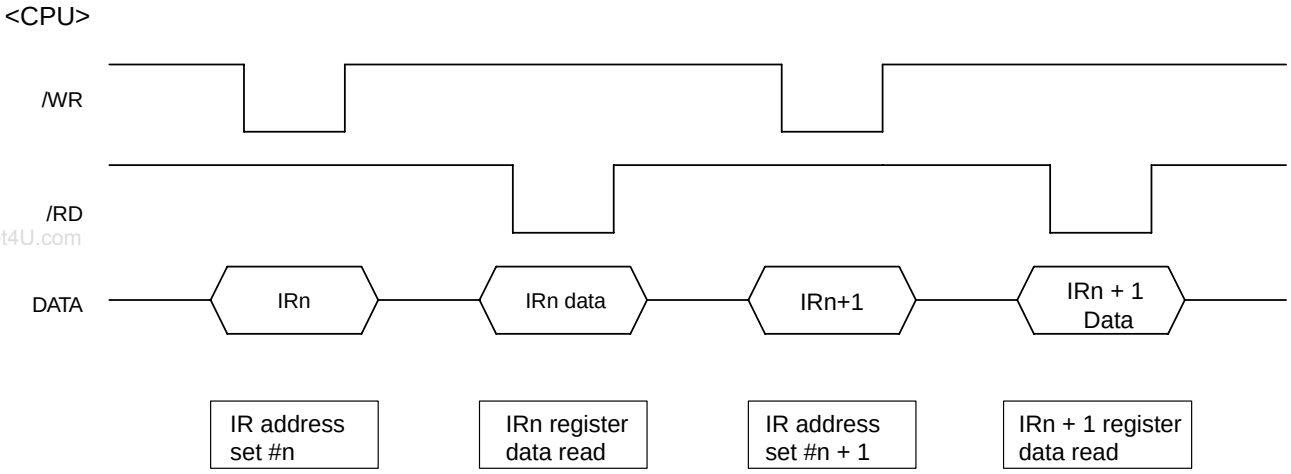


Figure 5-2. Write and Read (2/2)

Read (other than display memory access register)



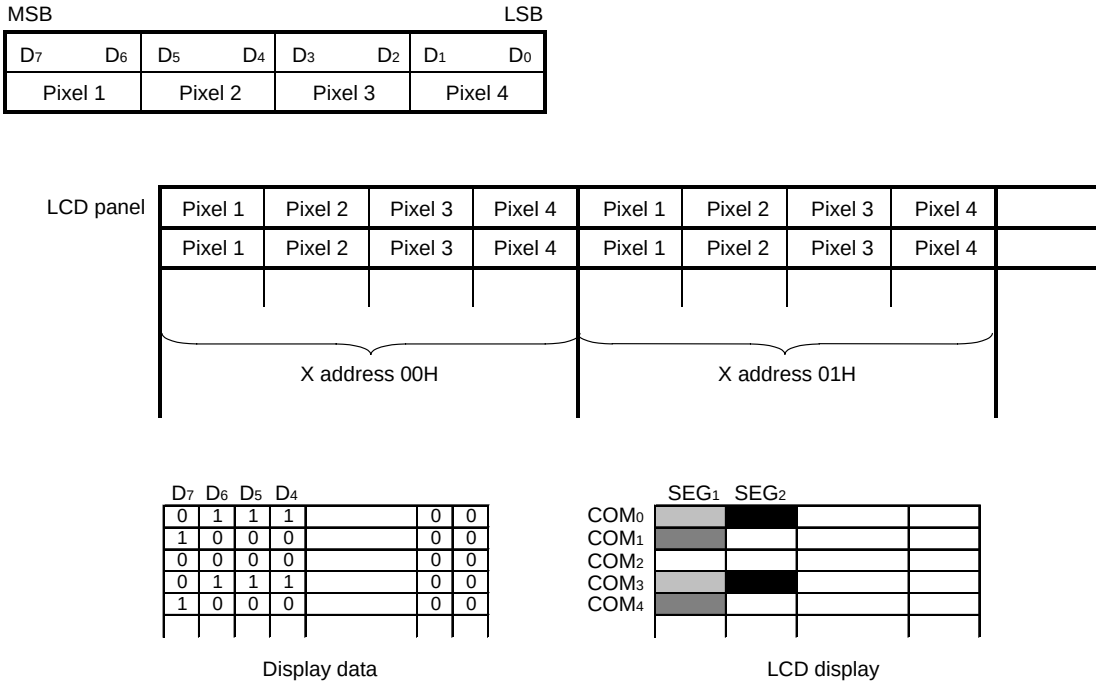
5.2 Display Data RAM

5.2.1 Display data RAM

This is the RAM that is used to store the display's dot data. The RAM configuration is 256 bits (32 x 8 bits) x 128 bits. Any specified bit can be accessed by selecting the corresponding X address and Y address. D_0 to D_7 are the display data sent from the CPU, and correspond to SEGx on the LCD display (see Figure 5-3).

The CPU writes data to and reads data from the display RAM via the I/O buffer, and these read/write operations are independent of the signal read operations for the LCD driver. Accordingly, there are no adverse effects (such as flicker) in the LCD display when display data RAM is accessed asynchronously.

Figure 5-3. Display Data RAM

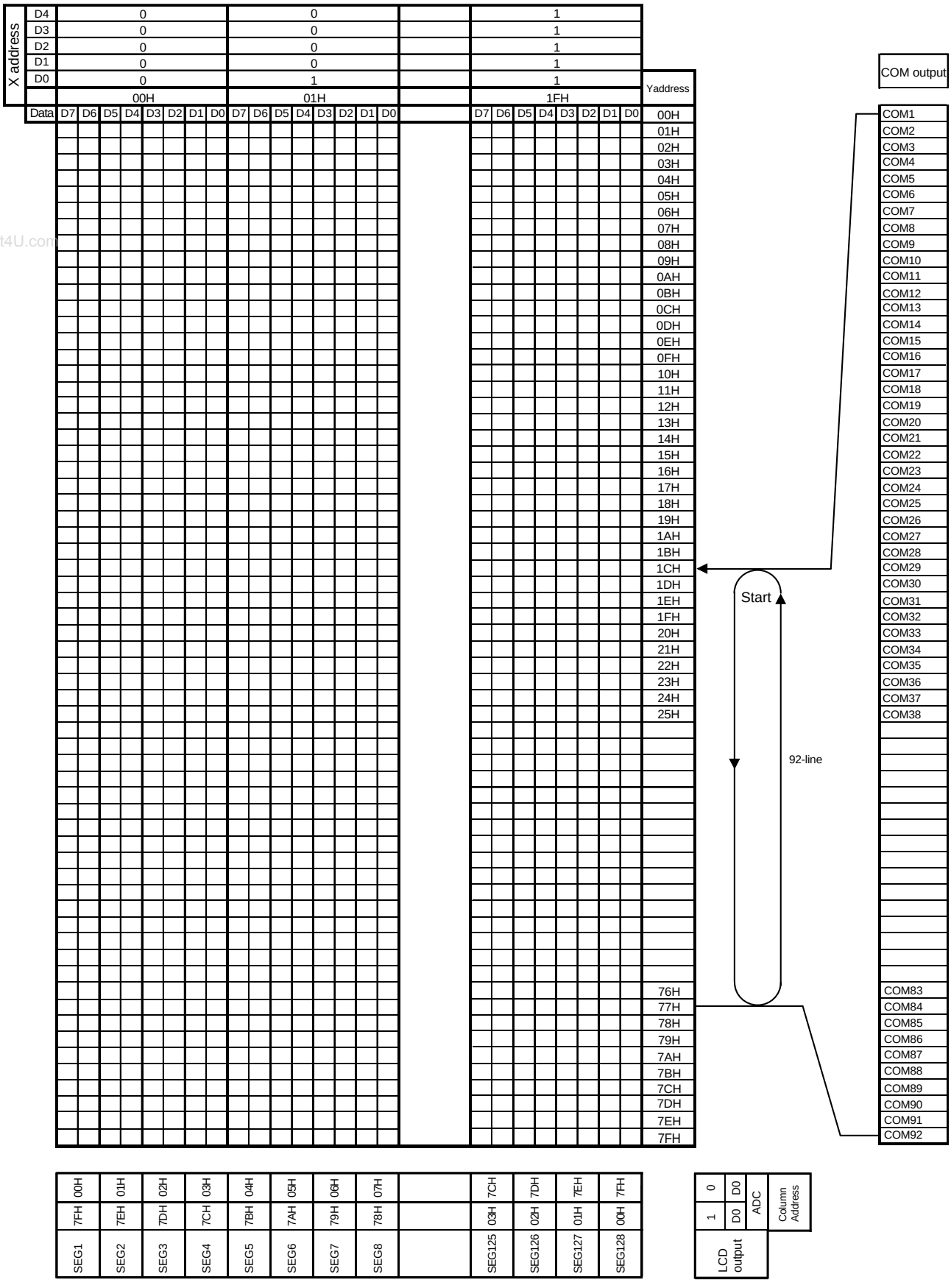


5.2.2 X address circuit

As shown in Figure 5-4, the display data RAM's X address is specified via the X address register (R3). When using X address increment mode (INC = 0: control register 2 (R1)), the specified X address is incremented (by 1) each time a display data read or write operation is executed. The CPU is able to continuously access the display data. The X address is incremented to 1FH, after which the Y address is incremented after each read or write operation and the X address is set back to 00H.

For monochrome (black-and-white) display, the X address is incremented to 0FH, after which the Y address is incremented after each read or write operation and the X address is set back to 00H.

Figure 5-4. Configuration of X Address Register



5.2.3 Column address circuit

When displaying the contents of the display data RAM, the column address corresponds to the SEG output, as shown in Figure 5-4.

As is shown in Table 5-1, the correspondence between the display RAM's column address and segment output can be inverted using the ADC flag in control register 1 (R0) (segment driver direction selection flag). This reduces the constraints on chip layout when assembling the LCD module.

Table 5-1. Relationship between Column Address and SEG Output

SEG Output		SEG_1				SEG_{128}
ADC (D_1)	0	00H	→	Column address	→	7FH
	1	7FH	←	Column address	←	00H

5.2.4 Y address circuit

As is shown in Figure 5-4, the Y address register (R4) is used to specify the display data RAM's Y address. When using Y address increment mode (INC = 1: control register 2 (R1)), the specified Y address is incremented (by 1) each time a display data read or write operation is executed. The CPU is able to continuously access the display data. The Y address is incremented to 7FH, after which the X address is incremented after each read or write operation and the Y address is set back to 00H.

5.2.5 Common scan circuit

The common scan circuit sets the scan lines for common signals. The scan direction is set using the COMR flag in control register 1 (R0), as shown in Table 5-2.

For example, when using 1/80 duty, when COMR = L the scan direction is $COM_1 \rightarrow COM_{80}$ and when COMR = H, the scan direction is $COM_{80} \rightarrow COM_1$ using the COM_{80} to COM_1 pins.

★ **Table 5-2. Relationship between Common Scan Circuit and Scan Direction**

COMR	0	COM_1	→	COM_{92}
(D_0)	1	COM_{92}	→	COM_1

5.2.6 Display start line set

As is shown in Figure 5-4, display start line set specifies the Y address that corresponds to the COM_1 output for displaying the contents of display data RAM. The display start line setting register (R12) is used to specify the top line in the display. The screen can be scrolled, overwritten, etc. A 7-bit display start address is set to the display start line setting register.

5.2.7 Display data latch circuit

The display data latch circuit is used for temporary storage of data that is output to the LCD driver from the display data RAM.

The display scan command that sets normal or reverse display mode and the display ON/OFF command control latched data so that there is no effect on the data in the display data RAM.

5.3 Blink/Reverse Display Circuit

The μPD16488A enables blinking display and reverse display in designated parts of the full dot display. A blinking display is achieved by cycling ON/OFF (level 0 when four-level gray scale mode has been selected) at approximately 1 Hz and reverse display is achieved by inverting the display level value.

The area designated for blinking is specified via the blink start/end line address registers (R14 and R15), the blink X address register (R13), and the blink data memory access register (R16).

First, the blinking display's start and end line addresses are selected via the blink start/end line address registers. Next, the blink X address register (R13) and the blink data memory (R16) are used to select the column for the blinking display.

The inversion start/end line address registers (R18 and R19), the inverted X address register (R17), and the inverted data memory access register (R20) are used to select the reverse display area.

First, the inversion start/end line address registers (R18 and R19) are set to select the line addresses where the reverse display will start and end. Next, the inverted X address register (R17) and the inverted data memory access register (R20) are used to select the column for the reverse display. The specified blink/inverted X address is incremented (by 1) with each input of blink/reverse display data.

The blink RAM and inversion RAM, which have a 128 bit (16 x 8 bit) configuration, are used to store data for blinking display and reverse display respectively. To access the desired bit, simply specify the corresponding X address. The blink/reverse data (data bits D_0 to D_7 sent from the CPU) correspond to SEGx on the LCD display, as shown in Figure 5-5.

After the area and data settings are complete, the BLD bit and IVD bit in the control register 1 (R0) are set to H, at which point the blinking and/or reverse display of data begins. Figure 5-6 illustrates the relationship between the start line address, end line address, blink/reverse data, and LCD display.

Table 5-3. Inversion Manipulation and Display

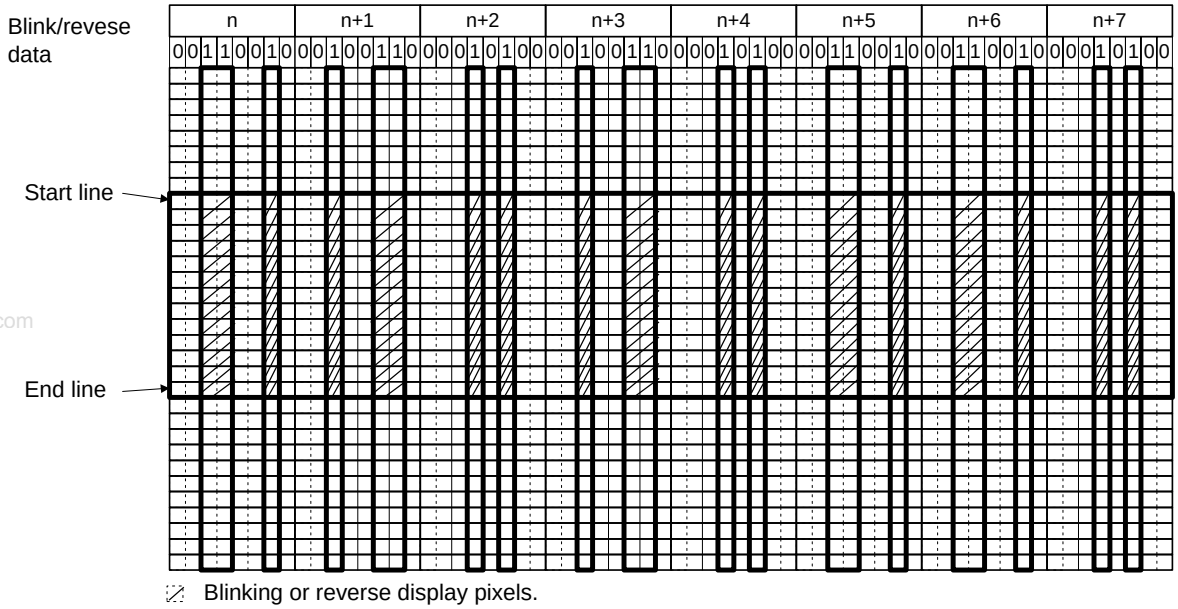
Original Level	After Inversion
Four-level gray scale display mode	
0, 0	1, 1
0, 1	1, 0
1, 0	0, 1
1, 1	0, 0
B/W display mode	
1	0
0	1

Figure 5-5. Correspondence Between Blink/Reverse Data and Segments

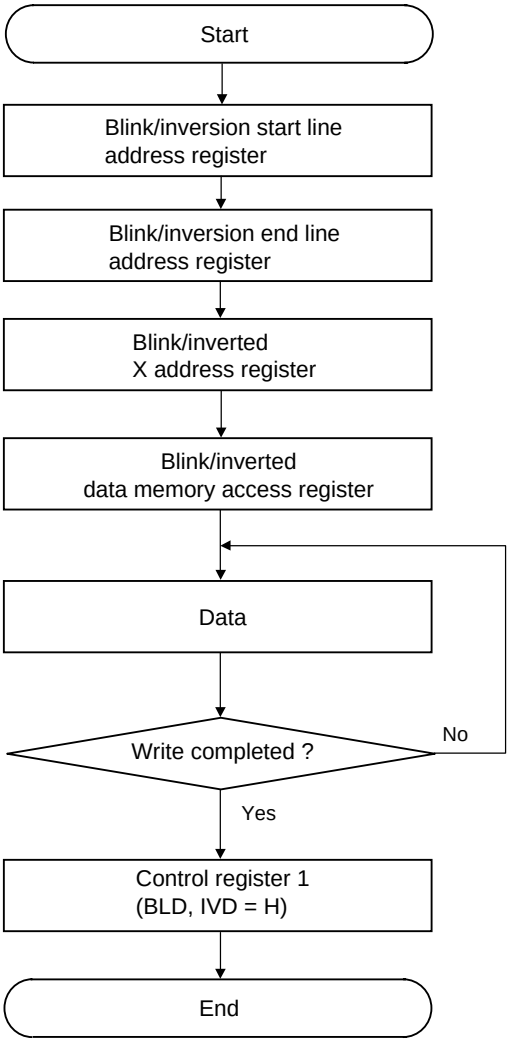
X address																															
	D3	0								0										1											
	D2	0								0										1											
	D1	0								0										1											
	D0	0								1										1											
		00H								01H										0FH											
	Data	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0			D7	D6	D5	D4	D3	D2	D1	D0				
		7FH	7EH	7DH	7CH	7BH	7AH	79H	78H	77H	76H	75H	74H	73H	72H	71H	70H			07H	08H	05H	04H	03H	02H	01H	00H				
		00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH			78H	79H	7AH	7BH	7CH	7DH	7EH	7FH				
		SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16			SEG121	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127	SEG128				

0	D0	ADC	Column address
1	D0		
LCD output			

Figure 5-6. Setting Image of Blink/Reverse Display Area



Example of sequence for setting blink/reverse display



5.4 Oscillator

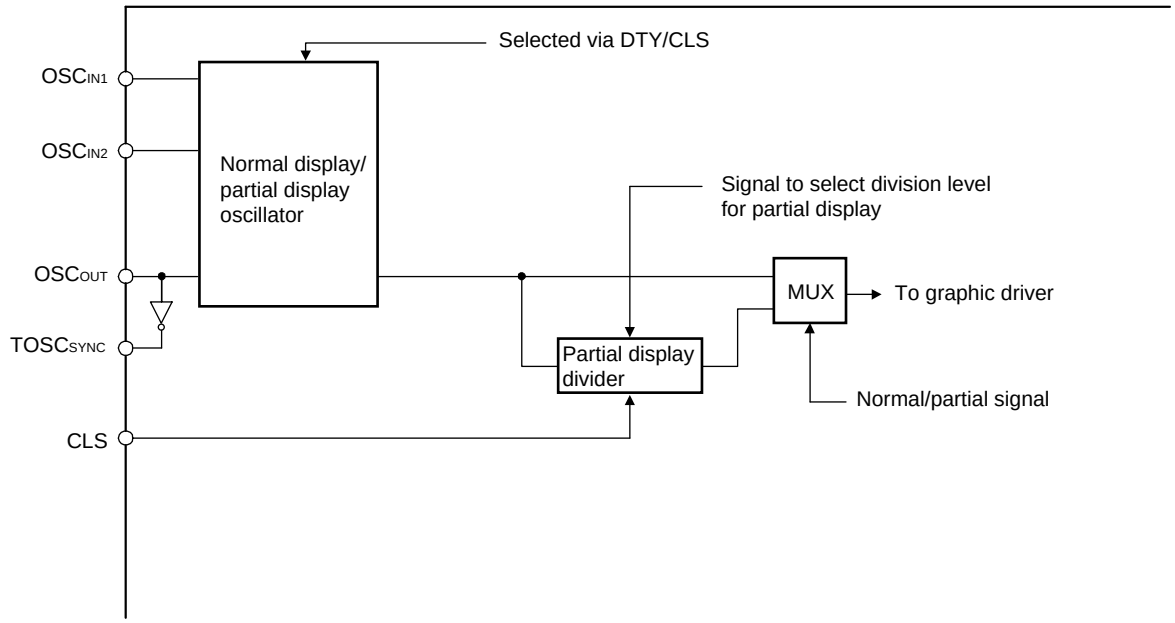
The μPD16488A include a CR-type oscillator (R external) for normal and partial display, which generates the display clocks.

The clocks from this oscillator are controlled via the CLS pin and the DTY flag in the control register 2 (R1). The clock configuration for the display can be set to suit the target system.

The functions of this circuit are described below.

- The oscillator for normal and partial display is enabled only when resistors RN and RP have been connected. The DTY flag in the control register 2 (R1) and the CLS pin status are used to switch between the oscillation clocks for normal display and partial display modes.
- The divider divides the external clock that has been input for the normal oscillator and the normal display into a clock for partial display. The external clock that is input for the partial oscillator and partial display is also divided for the partial display.
- The division level is automatically set for the divider based on the relationship between the ON/OFF status of the divider setting pin (CLS pin) and the duty of the specified partial display, as shown in Table 5-4.

Figure 5-7. Oscillator Block



The relationship between the frame frequency (f_{FRAME}), oscillation frequency (f_{OSCIN1}), and setting duty (in normal display mode) is described below.

$f_{FRAME} = f_{OSCIN1} \div 8 \div N$ (in four-level gray scale display mode)

$f_{FRAME} = f_{OSCIN1} \div 4 \div N$ (in B/W display mode)

N = 1/N duty (setting duty)

Table 5-4. Setting of Division Level for Partial Display and Static Icon Display

In four-level gray scale display mode (GRAY = L, control register 2 (R1))

Display Mode	Normal Display Duty Ratio	Partial Display Duty Ratio	Division Source OSC_{IN1} /OSC_{IN2}	Divider ON/OFF CLS	Normal/Partial Select DTY	Partial Division Ratio	Comments
Four-level gray scale GRAY = L	1/1 to 1/80	1/38	OSC_{IN1}	L(OFF)	L (Normal)	–	
		1/25					
		1/12					
		1/38		H(ON)			
		1/25					
		1/12					
		1/38	OSC_{IN2}	L(OFF)	H (Partial)	1/1	Partial frame frequency: f_{OSCIN2} /8 /38
		1/25				1/1	Partial frame frequency: f_{OSCIN2} /8 /25
		1/12				1/2	Partial frame frequency: f_{OSCIN2} /2(division ratio) /8 /12
		1/38	OSC_{IN1}	H(ON)		1/2	Partial frame frequency: f_{OSCIN1} /2(division ratio) /8 /38
		1/25				1/2	Partial frame frequency: f_{OSCIN1} /2(division ratio) /8 /25
		1/12				1/4	Partial frame frequency: f_{OSCIN1} /4(division ratio) /8 /12
	1/81 to 1/92	1/38	OSC_{IN1}	L(OFF)	L (Normal)	–	
		1/25					
		1/12					
		1/38		H(ON)			
		1/25					
		1/12					
		1/38	OSC_{IN2}	L(OFF)	H (Partial)	1/1	Partial frame frequency: f_{OSCIN2} /8 /38
		1/25				1/1	Partial frame frequency: f_{OSCIN2} /8 /25
		1/12				1/2	Partial frame frequency: f_{OSCIN2} /2(division ratio) /8 /12
		1/38	OSC_{IN1}	H(ON)		1/2	Partial frame frequency: f_{OSCIN1} /2(division ratio) /8 /38
		1/25				1/4	Partial frame frequency: f_{OSCIN1} /4(division ratio) /8 /25
		1/12				1/8	Partial frame frequency: f_{OSCIN1} /8(division ratio) /8 /12

In black/white display mode (GRAY = H, control register 2 (R1))

Display Mode	Normal Display Duty Ratio	Partial Display Duty Ratio	Division Source OSC_{IN1} /OSC_{IN2}	Divider ON/OFF CLS	Normal/Partial Select DTY	Partial Division Ratio	Comments
B/W GRAY = H	1/1 to 1/80	1/38	OSC_{IN1}	L(OFF)	L (Normal)	–	
		1/25					
		1/12					
		1/38		H(ON)			
		1/25					
		1/12					
		1/38	OSC_{IN2}	L(OFF)	H (Partial)	1/1	Partial frame frequency: f_{OSCIN2} /4 /38
		1/25				1/1	Partial frame frequency: f_{OSCIN2} /4 /25
		1/12				1/2	Partial frame frequency: f_{OSCIN2} /2(division ratio) /4 /12
		1/38	OSC_{IN1}	H(ON)		1/2	Partial frame frequency: f_{OSCIN1} /2(division ratio) /4 /38
		1/25				1/2	Partial frame frequency: f_{OSCIN1} /2(division ratio) /4 /25
		1/12				1/4	Partial frame frequency: f_{OSCIN1} /4(division ratio) /4 /12
	1/81 to 1/92	1/38	OSC_{IN1}	L(OFF)	L (Normal)	–	
		1/25					
		1/12					
		1/38		H(ON)			
		1/25					
		1/12					
		1/38	OSC_{IN2}	L(OFF)	H (Partial)	1/1	Partial frame frequency: f_{OSCIN2} /4 /38
		1/25				1/1	Partial frame frequency: f_{OSCIN2} /4 /25
		1/12				1/2	Partial frame frequency: f_{OSCIN2} /2(division ratio) /4 /12
		1/38	OSC_{IN1}	H(ON)		1/2	Partial frame frequency: f_{OSCIN1} /2(division ratio) /4 /38
		1/25				1/4	Partial frame frequency: f_{OSCIN1} /4(division ratio) /4 /25
		1/12				1/8	Partial frame frequency: f_{OSCIN1} /8(division ratio) /4 /12

Table 5-5 shows the relationship between the CLS pin, resistors RN and RP, and the display clock circuit.

Table 5-5. Relationship between CLS Pin/Resistors and Display Clock Circuit

RN Connection	RP Connection	CLS	Clock for Normal Display	Clock for Partial Display	Use Example (Figure 5-8)
Connected	Connected	L	Internal oscillator	Internal oscillator	(A)
Connected	Not connected	H	Internal oscillator	Divided from oscillator clock	(B)
Not connected	Connected	L	External clock	Internal oscillator	(C)
Not connected	Not connected	L	External clock	External clock	(D)
Not connected	Not connected	H	External clock	Divided from external clock	(E)

Figure 5-8. Clock Use Examples

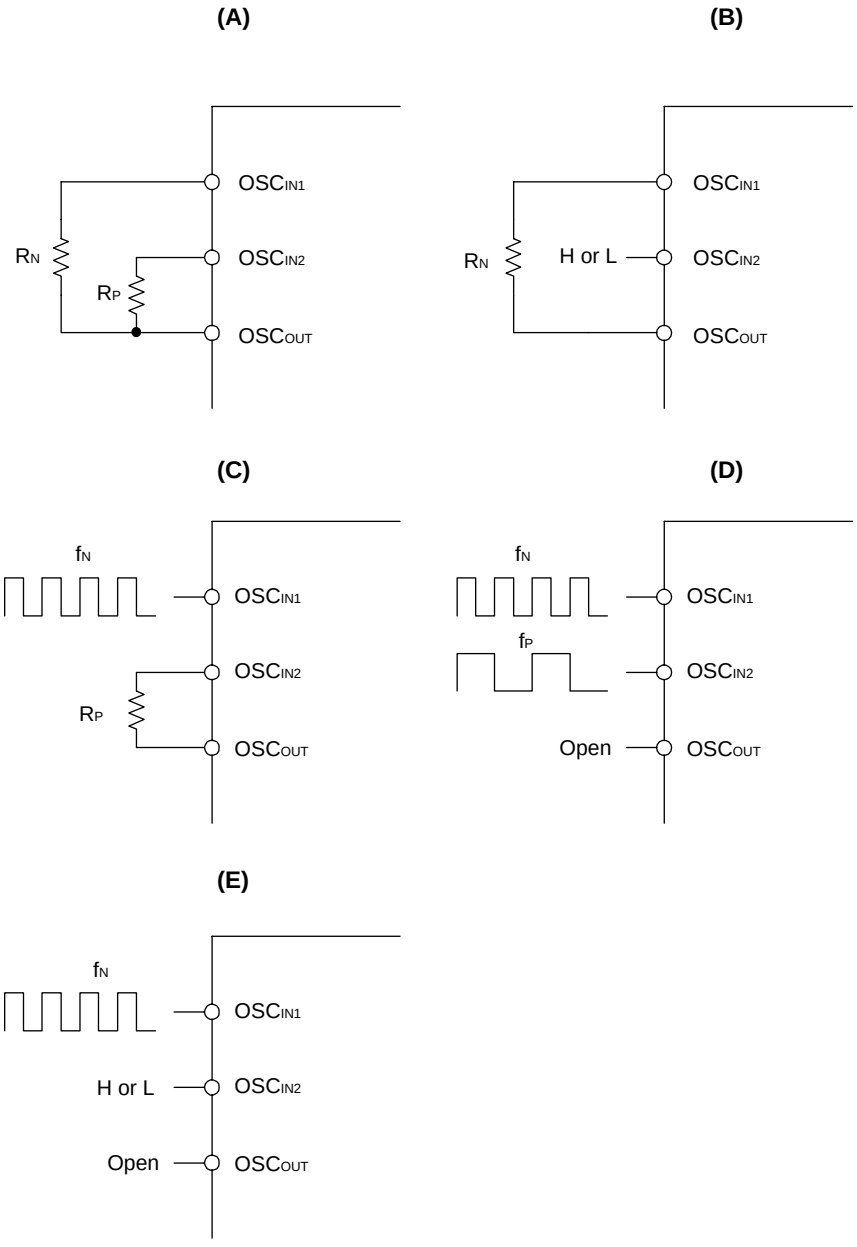
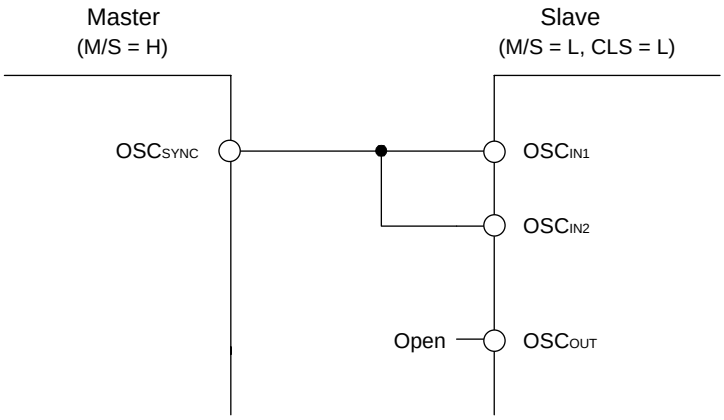
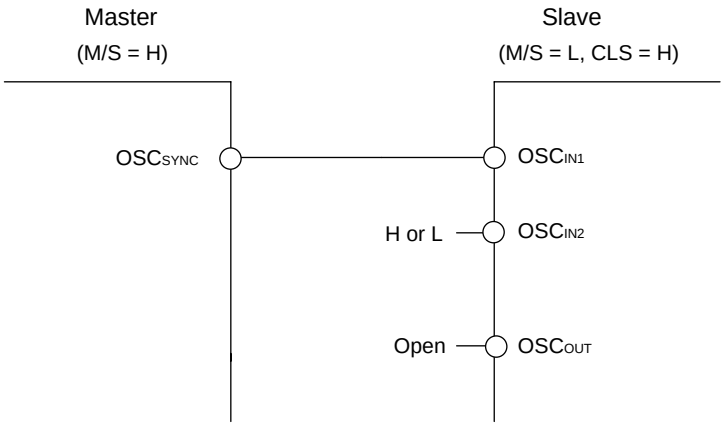


Figure 5-9. Master/Slave Connection Examples

(A)



(B)



5.5 Display Timing Generator

The display clock generates timing signals for the line address circuit and the display data latch circuit.

Display data is latched into the display data latch circuit in synch with the display clock and is output via segment driver output pins.

Reading of the display data is completely independent of the CPU's accessing of the display data RAM. Consequently, there are no adverse effects (such as flicker) on the LCD panel even when the display data RAM is accessed asynchronously in relation to the LCD contents.

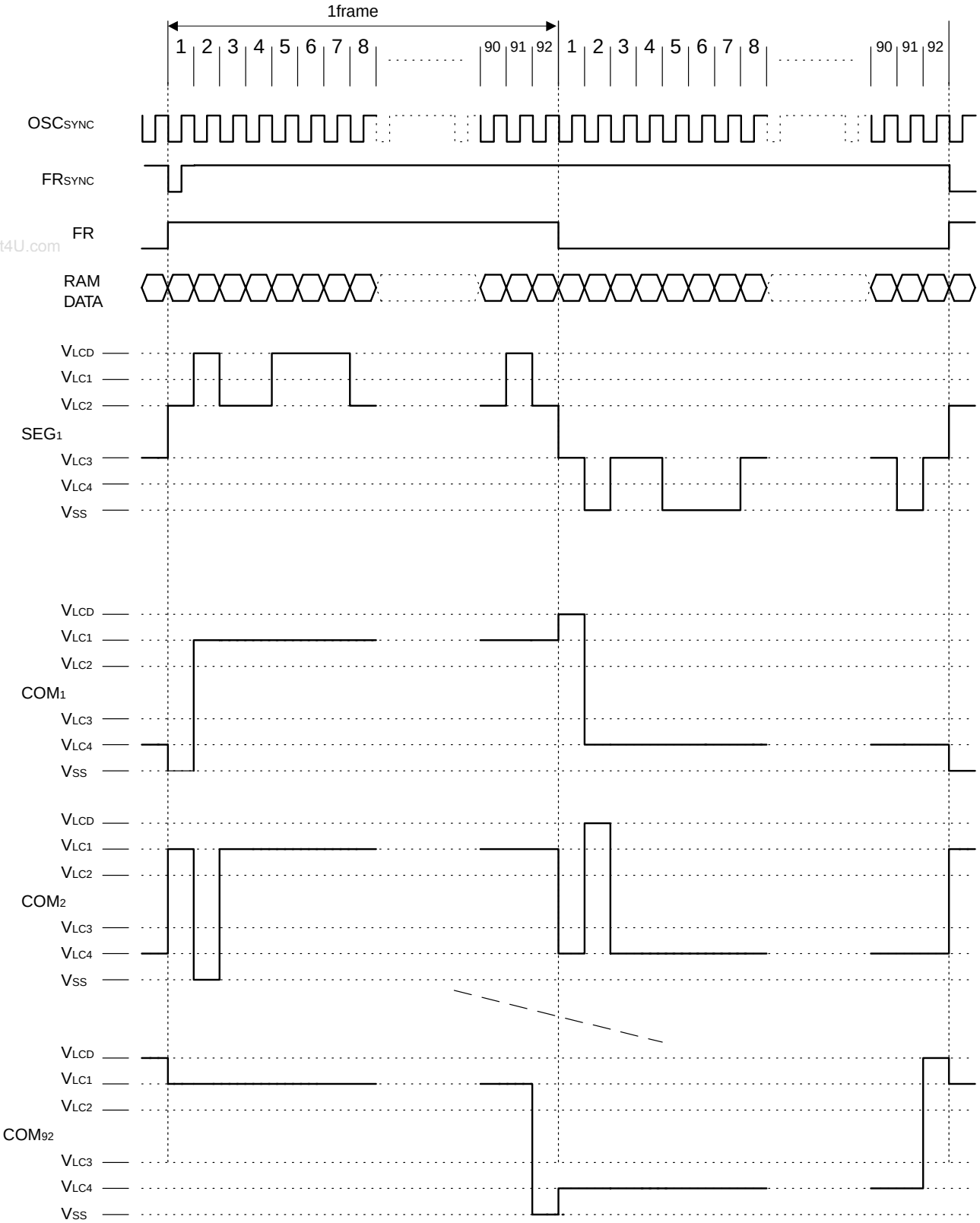
The internal common timing is generated from the display clock. As shown in Figure 5-10, a driver waveform based on the frame AC drive method is generated for the LCD driver.

If a multiple set of μPD16488A chips are used, the display timing signals (FR and FR_{SYNC}) for the slave side must be supplied from the master side.

Table 5-6. Relationship Between Operation Mode and FR, FR_{SYNC}

Operation Mode	FR	FR_{SYNC}
Master (M/S = H)	Output	Output
Slave (M/S = L)	Input	Input

Figure 5-10. Driver Waveform Based on Frame AC Drive Method



5.6 Power Supply Circuit

The power supply circuit supplies the voltage needed to drive the LCD. It includes a booster, voltage regulator, and voltage follower.

In the power supply circuit, the power system control register 1 (R32) is used to control the ON/OFF status of the power supply circuit's booster, voltage regulator (also called V regulator), and voltage follower (V/F). This makes it possible to jointly use an external power supply together with certain functions of the on-chip power supply. Table 5-7 shows the function that controls the 3-bit data in the power system control register 1 (R32) and Table 5-8 shows a reference chart of combinations.

Table 5-7. Control Values of Bits in Power System Control 1

Item		Status	
		1	0
OP2	Booster control bit	ON	OFF
OP1	Voltage regulator (V regulator) control bit	ON	OFF
OP0	Voltage follower (V/F) control bit	ON	OFF

Table 5-8. Reference Chart of Combinations

Use Status	OP2	OP1	OP0	Booster	V Regulator	V/F	External Power Supply Input	Boost-Related Note System Pins
<1> Use on-chip power supply	1	1	1	enable	enable	enable	V_{DD2}	Used
<2> Use V regulator and V/F only	0	1	1	disable	enable	enable	V_{OUT}	Not connected
<3> Use V/F only	0	0	1	disable	disable	enable	V_{OUT}, AMP_{OUT}	Not connected
<4> Use external power supply only	0	0	0	disable	disable	disable	V_{OUT}, V_{LCD} to V_{LC4}	Not connected

Note The boost-related system pins are indicated as pins $C1^+$, $C1^-$ to $C9^+$, $C9^-$, and C1A.

5.6.1 Booster

A booster that boosts the LCD driving voltage by 2 to 9 times is incorporated in the power supply circuit.

Since the booster uses signals from the on-chip oscillator, either the oscillator must be operating or a display clock must be input from an external source.

The booster uses pins $C1^+$, $C1^-$ to $C9^+$, $C9^-$ for normal boost and pins C1A and V_{DD2} for boost regulation. The wire impedance should be kept as low as possible. The number of boost levels is set using the FBS2, FBS1, and FBS0 flags in the power system control 3 (R34), as shown in Table 5-9.

Caution If a capacitor is connected to a boost-related system pin that is not for one of these set boost levels, current consumption may increase. Therefore, do not connect any capacitors beyond the number of set boost levels. This also applies for the CA1 pin, used to regulate the boost levels.

Figure 5-11 describes the connection method for boost levels and capacitors.

The partial booster is settings are made using the BST1 and BST0 flags in the power system control 3 (R34), as shown in Table 5-10.

Figure 5-11. Connection Method for Boost Levels and Capacitors

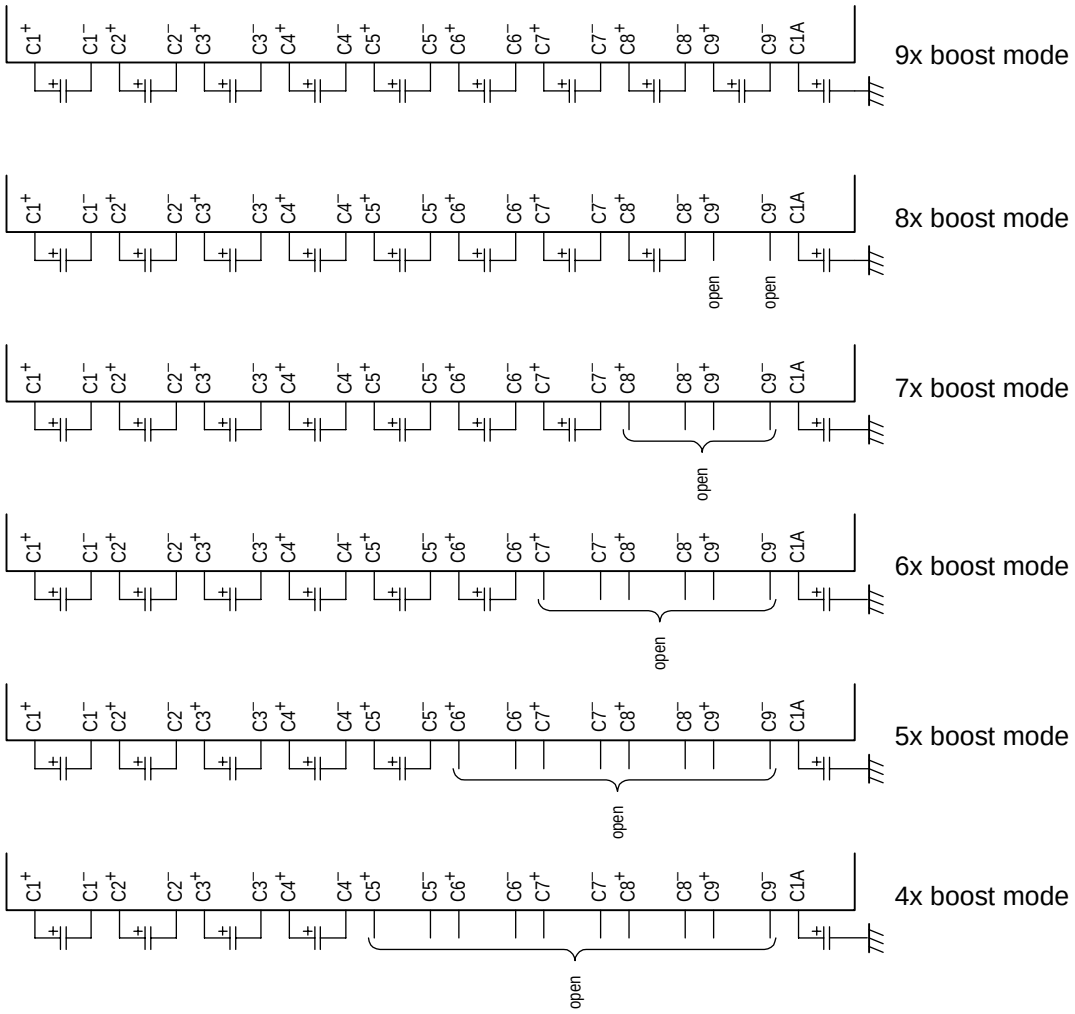


Table 5-9. Boost Level Settings for Normal Display's Booster

FBS2	FBS1	FBS0	Boost Level
0	0	0	4x
0	0	1	5x
0	1	0	6x
0	1	1	7x
1	0	0	8x
1	0	1	9x
1	1	0	Prohibited
1	1	1	Prohibited

Table 5-10. Boost Level Settings for Partial Display's Booster

BST1	BST0	Boost Level
0	0	2x
0	1	3x
1	0	4x
1	1	Prohibited

5.6.2 Voltage regulator

The boost voltage from V_{OUT} is supplied to the voltage regulator and output as the LCD drive voltage V_{LCD}.

Since the μPD16488A has a 256-step electronic volume function and an on-chip resistor for V_{LCD} voltage regulation, a small number of components can be used to configure a highly accurate voltage regulator.

(1) When using an on-chip resistor for V_{LCD} voltage regulation

The on-chip resistor for V_{LCD} voltage regulation and the electronic volume function can be used to regulate the contrast of the LCD contents by controlling the LCD drive voltage V_{LCD} using commands only. In such cases, no external resistor is needed.

If $V_{LCD} < V_{OUT}$, then the value for V_{LCD} can be determined from the following equation.

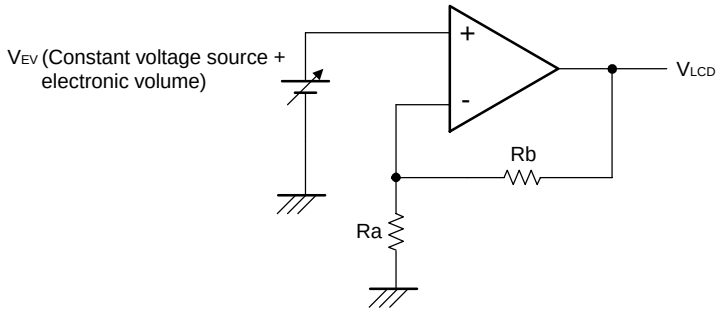
Example Equation $V_{LCD} < V_{OUT}$

$$V_{LCD} = (1 + \frac{Rb}{Ra}) V_{EV}$$

$$V_{LCD} = (1 + \frac{Rb}{Ra}) (1 - \frac{\alpha}{384}) V_{REG}$$

Remark $V_{EV} = (1 - \frac{\alpha}{384}) V_{REG}$

Figure 5-12. When Using On-Chip Resistor for V_{LCD} Voltage Regulation



V_{REG} is the IC's on-chip constant voltage source, for which three types of temperature characteristic curves are available. These temperature characteristic curves can be adjusted via settings in the power system control register 1 (R32) (TSC1, TCS0), as shown in Table 5-11.

Table 5-11 shows the V_{REG} voltage when T_A = 25°C.

Table 5-11. V_{REG} Voltage When T_A = 25°C

Status	TCS1	TCS0	Temperature Curve (%/°C)	V_{REG} (TYP.) (V)
Internal power supply	0	0	–0.06	1.04
	0	1	–0.08	0.98
	1	0	–0.09	0.93
	1	1	–0.12	0.85

α is the electronic volume register (R35) value. Any of 256 statuses can be set as the fetched status for α corresponding to the data set to the 8-bit electronic control register. α values based on settings in the electronic volume register (R35: normal display mode) and the partial electronic volume register (R36: partial display mode) are listed in Table 5-12.

Table 5-12. α Values Based on Settings in Electronic Volume Register

Register								α
EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
PEV7	PEV6	PEV5	PEV4	PEV3	PEV2	PEV1	PEV0	
0	0	0	0	0	0	0	0	384
0	0	0	0	0	0	0	1	254
0	0	0	0	0	0	1	0	253
0	0	0	0	0	0	1	1	252
				:				:
1	1	1	1	1	1	0	1	2
1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	0

Rb/Ra is an on-chip resistance factor used for the V_{LCD} voltage regulator. This factor can be controlled at eight levels based on settings in power control register 2 (R33) (VRR2, VRR1, VRR0: normal display mode and PVR2, PVR1, PVR0: partial display mode). Reference voltage values (1 + Rb/Ra) are determined based on 4-bit data set to V_{LCD}'s on-chip resistance factor register, as shown in Table 5-13.

Table 5-13. Determination of Reference Voltage Values Based on Settings of On-Chip Resistor for V_{LCD} Voltage Regulation

Register			1+Rb/Ra
VRR2	VRR1	VRR0	
PVR2	PVR1	PVR0	
0	0	0	5
0	0	1	8
0	1	0	12
0	1	1	13
1	0	0	16
1	0	1	19
1	1	0	21
1	1	1	24

(2) When using an external resistor (instead of using the on-chip resistor for V_{LCD} voltage regulation)

Instead of using only the on-chip resistor setting for V_{LCD} voltage regulation (IRS = L), resistors (Ra', Rb' and Rc') can be added between V_{SS} and V_R, between AMP_{OUTP} and AMP_{OUT}, and between V_R and AMP_{OUT} to set the LCD drive voltage V_{LCD}. In such cases, the electronic volume function can be used to control the LCD drive voltage V_{LCD} and to regulate the contrast of the LCD contents via commands.

In addition, the μPD16488A enable selection between two display values (for normal display and partial display). The value is set using an external division resistor and is automatically selected by the DTY flag in the control register 2 (R1).

The V_{LCD} value can be determined using **Example 1** (DTY = 0) and **Example 2** (DTY = 1) if it is within the range of $V_{LCD} < V_{OUT}$.

Example 1. DTY = 0, normal display mode

$$V_{LCD} = (1 + \frac{Rb'}{Ra'})\ V_{EV}$$

$$V_{LCD} = (1 + \frac{Rb'}{Ra'})\ (1 - \frac{\alpha}{384})\ V_{REG}$$

Remark $V_{EV}\ (1 - \frac{\alpha}{384})\ V_{REG}$

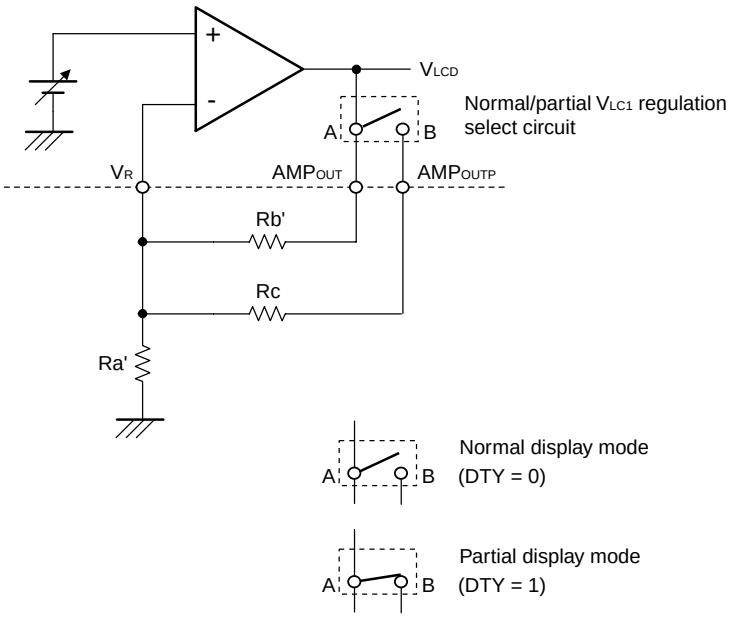
Example 2. DTY = 1, partial display mode

$$V_{LCD} = (1 + \frac{Rb' \times Rc}{Ra'(Rb' + Rc)})\ V_{EV}$$

$$V_{LCD} = (1 + \frac{Rb' \times Rc}{Ra'(Rb' + Rc)})\ (1 - \frac{\alpha}{384})\ V_{REG}$$

Remark $V_{EV} = (1 - \frac{\alpha}{384})\ V_{REG}$

Figure 5-13. When Using External Resistor



5.6.3 Use of op amp for level power supply control

Although the μPD16488A includes a circuit designed for low power consumption (HPM1, HPM0 = 0, 0), display quality problems may occur when a large-load LCD panel is used. In such cases, the display quality and power consumption level can be improved by setting. The HPM1 and HPM0 flags in the power system control register 1 (R32) to "0, 1" to "1, 1" to switch to the op amp driver capacity for mode settings shown in Table 5-14. Check the actual display quality before deciding which mode to set.

If setting high power mode still does not sufficiently improve the display quality, the LCD drive voltage must be provided from an external power source.

Table 5-14. Op Amp Mode Setting

HPM1	HPM0	Mode Setting
0	0	Normal mode
0	1	Low power mode
1	0	High power mode
1	1	For power ON mode

5.6.4 Application examples of power supply circuits

Figures 5-14 to 5-19 show application examples of power supply circuits.

Figure 5-14. IRS = H, [OP2, OP1, OP0] = [1, 1, 1]

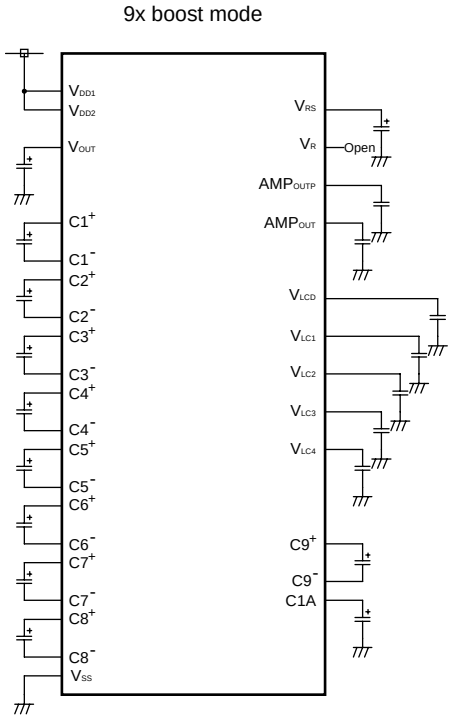


Figure 5-15. IRS = L, [OP2, OP1, OP0] = [1, 1, 1]

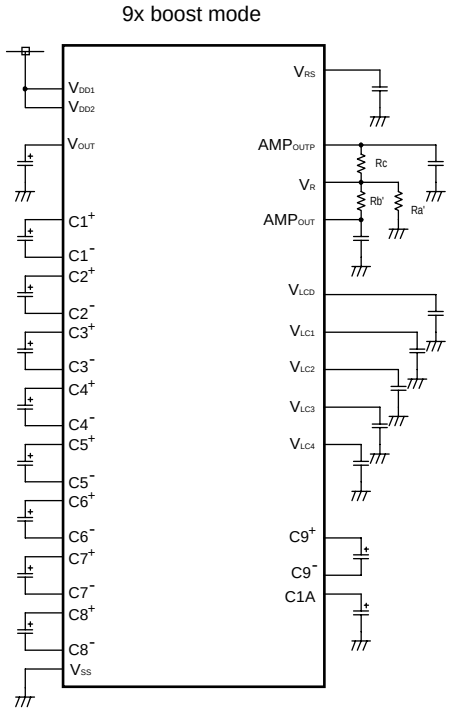


Figure 5-16. IRS = H, [OP2, OP1, OP0] = [0, 1, 1]

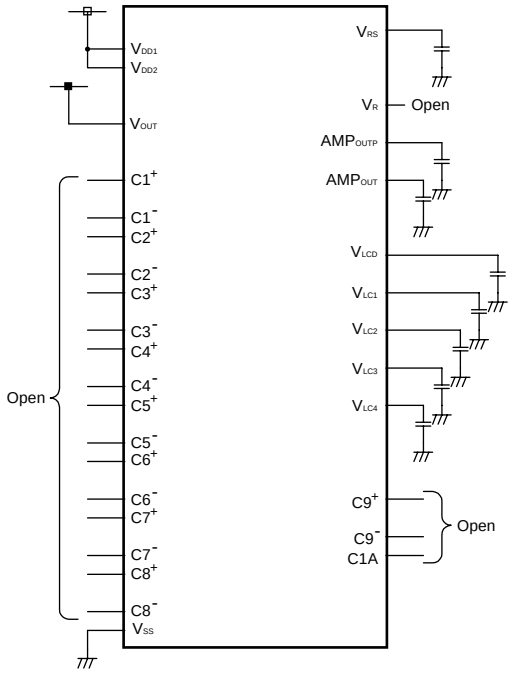


Figure 5-17. IRS = L, [OP2, OP1, OP0] = [0, 0, 1]

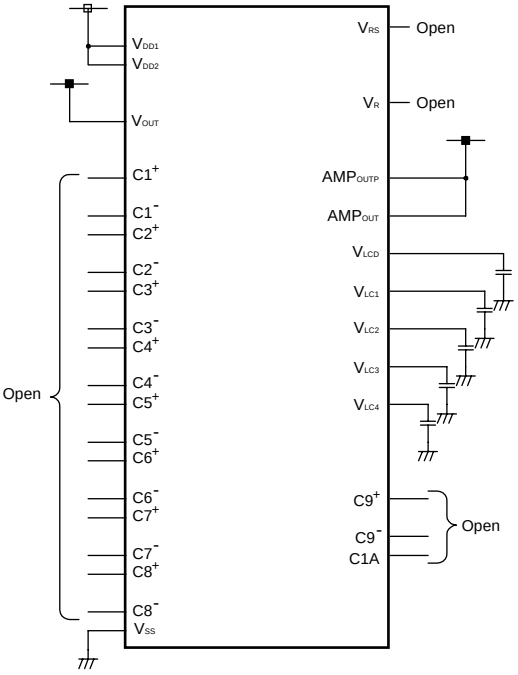


Figure 5-18. IRS = L, [OP2, OP1, OP0] = [0, 0, 0]

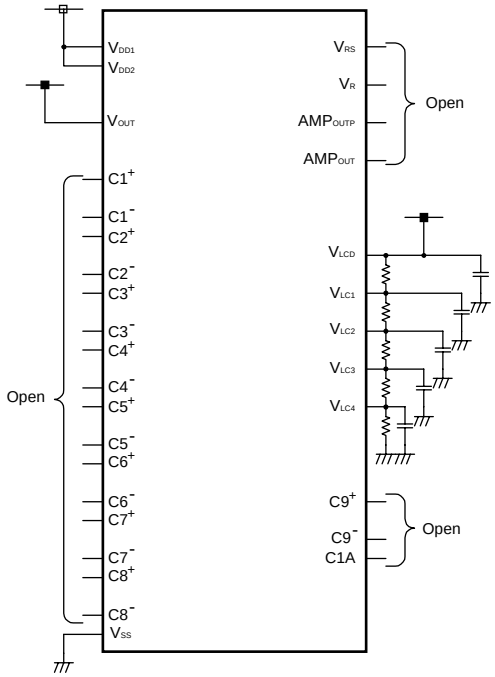
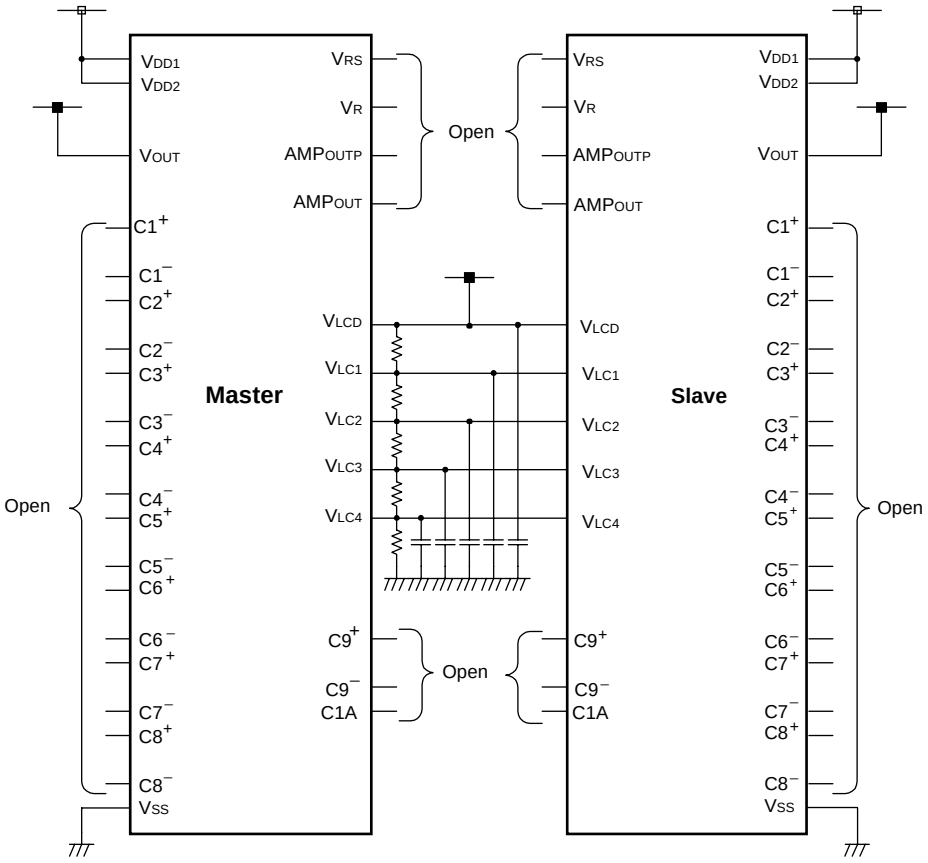


Figure 5-19. Master/Slave Connection Example



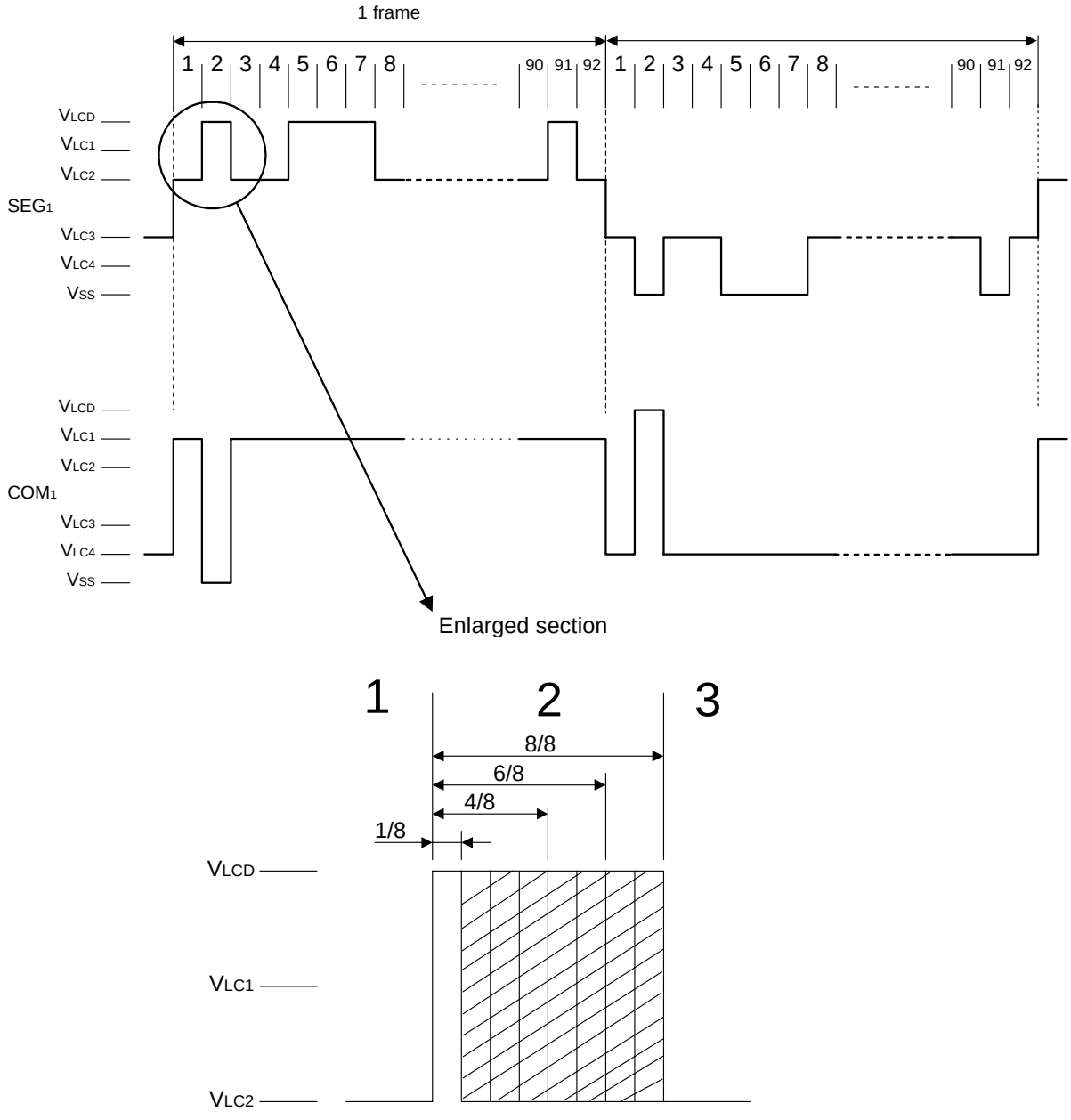
5.7 LCD Display Drivers

μPD16488A includes a full dot driver. The full dot driver has a 33-level gray-scale palette (eight levels of pulse width modulation plus four-frame rate control), from which four levels of gray scale can be selected and registered as the IC's output gray-scale palette (refer to **6.23 Gary scale registers 1 to 4 (R23 to R26)**).

5.7.1 Full-dot pulse width modulation

The μPD16488A's pulse width modulator divides the normal LCD display signal's segment pulse width by eight and outputs in synch with the dot output timing based on the ratio (1/8 to 8/8 pulses) for the gray-scale palette that has been selected via a command.

Figure 5-20. Full-Dot Pulse Width Modulation



Caution There is no pulse width modulation for common outputs.

The output pulses are output as odd-numbered lines/even-numbered lines or as even-numbered lines/odd-numbered lines, as shown in Figure 5-21. The pulse rising edge and falling edge combinations for each frame are listed in Table 5-15.

Figure 5-21. Example of Pulse Width Modulated Output

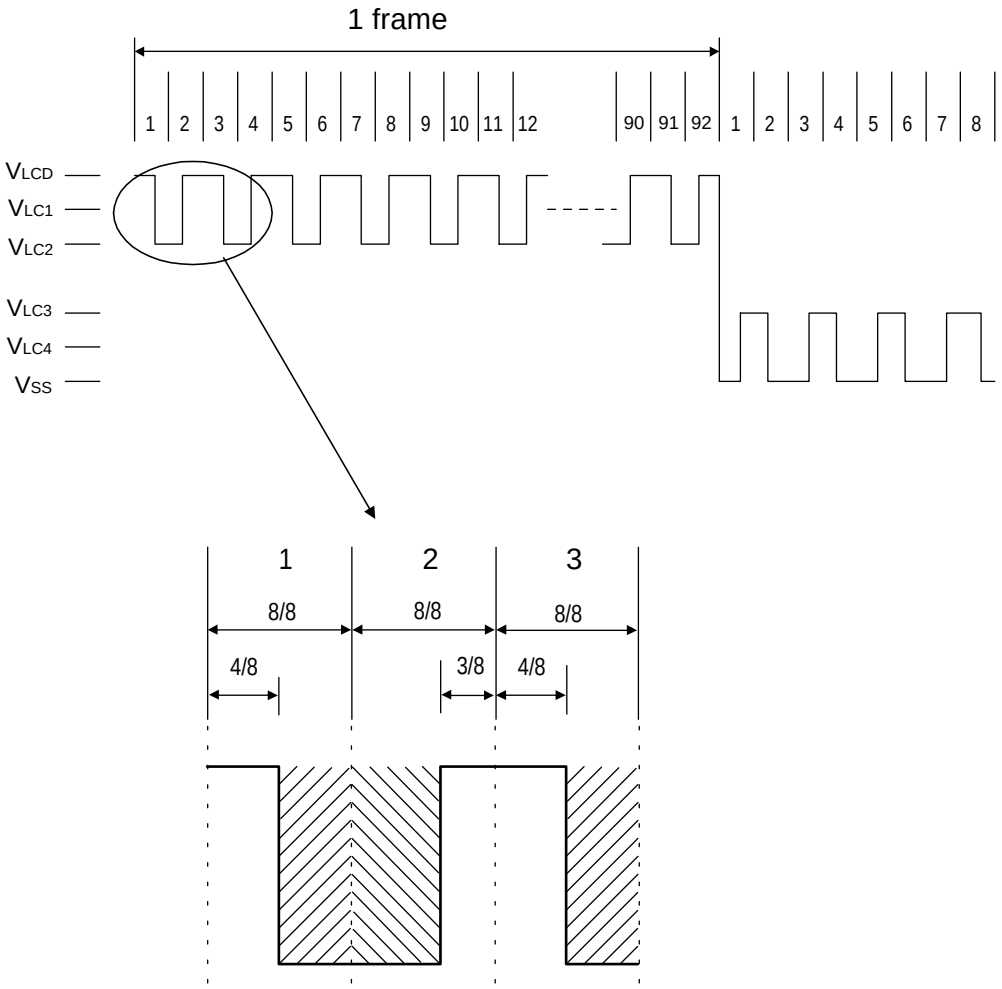


Table 5-15. Example of Pulse Width Modulated Output (1/3)

Gray-scale level	COM	1, 2 Frames		3, 4 Frames		5, 6 Frames		7, 8 Frames	
		SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered
0	4n+1	0	0	0	0	0	0	0	0
	4n+2	0	0	0	0	0	0	0	0
	4n+3	0	0	0	0	0	0	0	0
	4n+4	0	0	0	0	0	0	0	0
1	4n+1	↑1	↓1	0	0	0	0	0	0
	4n+2	0	0	0	0	↓1	↑1	0	0
	4n+3	0	0	0	0	0	0	↓1	↑1
	4n+4	0	0	↑1	↓1	0	0	0	0
2	4n+1	↑1	↓1	0	0	↑1	↓1	0	0
	4n+2	↓1	↑1	0	0	↓1	↑1	0	0
	4n+3	0	0	↓1	↑1	0	0	↓1	↑1
	4n+4	0	0	↑1	↓1	0	0	↑1	↓1
3	4n+1	↑1	↓1	↓1	↑1	↑1	↓1	0	0
	4n+2	↓1	↑1	0	0	↓1	↑1	↑1	↓1
	4n+3	↑1	↓1	↓1	↑1	0	0	↓1	↑1
	4n+4	0	0	↑1	↓1	↓1	↑1	↑1	↓1
4	4n+1	↑1	↓1	↓1	↑1	↑1	↓1	↓1	↑1
	4n+2	↓1	↑1	↑1	↓1	↓1	↑1	↑1	↓1
	4n+3	↑1	↓1	↓1	↑1	↑1	↓1	↓1	↑1
	4n+4	↓1	↑1	↑1	↓1	↓1	↑1	↑1	↓1
5	4n+1	↑2	↓2	↓1	↑1	↑1	↓1	↓1	↑1
	4n+2	↓1	↑1	↑1	↓1	↓2	↑2	↑1	↓1
	4n+3	↑1	↓1	↓1	↑1	↑1	↓1	↓2	↑2
	4n+4	↓1	↑1	↑2	↓2	↓1	↑1	↑1	↓1
6	4n+1	↑2	↓2	↓1	↑1	↑2	↓2	↓1	↑1
	4n+2	↓2	↑2	↑1	↓1	↓2	↑2	↑1	↓1
	4n+3	↑1	↓1	↓2	↑2	↑1	↓1	↓2	↑2
	4n+4	↓1	↑1	↑2	↓2	↓1	↑1	↑2	↓2
7	4n+1	↑2	↓2	↓2	↑2	↑2	↓2	↓1	↑1
	4n+2	↓2	↑2	↑1	↓1	↓2	↑2	↑2	↓2
	4n+3	↑2	↓2	↓2	↑2	↑1	↓1	↓2	↑2
	4n+4	↓1	↑1	↑2	↓2	↓2	↑2	↑2	↓2
8	4n+1	↑2	↓2	↓2	↑2	↑2	↓2	↓2	↑2
	4n+2	↓2	↑2	↑2	↓2	↓2	↑2	↑2	↓2
	4n+3	↑2	↓2	↓2	↑2	↑2	↓2	↓2	↑2
	4n+4	↓2	↑2	↑2	↓2	↓2	↑2	↑2	↓2
9	4n+1	↑3	↓3	↓2	↑2	↑2	↓2	↓2	↑2
	4n+2	↓2	↑2	↑2	↓2	↓3	↑3	↑2	↓2
	4n+3	↑2	↓2	↓2	↑2	↑2	↓2	↓3	↑3
	4n+4	↓2	↑2	↑3	↓3	↓2	↑2	↑2	↓2
10	4n+1	↑3	↓3	↓2	↑2	↑3	↓3	↓2	↑2
	4n+2	↓3	↑3	↑2	↓2	↓3	↑3	↑2	↓2
	4n+3	↑2	↓2	↓3	↑3	↑2	↓2	↓3	↑3
	4n+4	↓2	↑2	↑3	↓3	↓2	↑2	↑3	↓3

Remarks 1. n: Integer from 0 to 31.

2. ↑A: Rising edge of pulse during line A output.

3. ↓A: Rising edge of pulse at start of line A output.

4. A: PWM pulse width (A/8)

Table 5-15. Example of Pulse Width Modulated Output (2/3)

Gray-scale level	COM	1, 2 Frames		3, 4 Frames		5, 6 Frames		7, 8 Frames	
		SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered
11	4n+1	↑3	↓3	↓3	↑3	↑3	↓3	↓2	↑2
	4n+2	↓3	↑3	↑2	↓2	↓3	↑3	↑3	↓3
	4n+3	↑3	↓3	↓3	↑3	↑2	↓2	↓3	↑3
	4n+4	↓2	↑2	↑3	↓3	↓3	↑3	↑3	↓3
12	4n+1	↑3	↓3	↓3	↑3	↑3	↓3	↓3	↑3
	4n+2	↓3	↑3	↑3	↓3	↓3	↑3	↑3	↓3
	4n+3	↑3	↓3	↓3	↑3	↑3	↓3	↓3	↑3
	4n+4	↓3	↑3	↑3	↓3	↓3	↑3	↑3	↓3
13	4n+1	↑4	↓4	↓3	↑3	↑3	↓3	↓3	↑3
	4n+2	↓3	↑3	↑3	↓3	↓4	↑4	↑3	↓3
	4n+3	↑3	↓3	↓3	↑3	↑3	↓3	↓4	↑4
	4n+4	↓3	↑3	↑4	↓4	↓3	↑3	↑3	↓3
14	4n+1	↑4	↓4	↓3	↑3	↑4	↓4	↓3	↑3
	4n+2	↓4	↑4	↑3	↓3	↓4	↑4	↑3	↓3
	4n+3	↑3	↓3	↓4	↑4	↑3	↓3	↓4	↑4
	4n+4	↓3	↑3	↑4	↓4	↓3	↑3	↑4	↓4
15	4n+1	↑4	↓4	↓4	↑4	↑4	↓4	↓3	↑3
	4n+2	↓4	↑4	↑3	↓3	↓4	↑4	↑4	↓4
	4n+3	↑4	↓4	↓4	↑4	↑3	↓3	↓4	↑4
	4n+4	↓3	↑3	↑4	↓4	↓4	↑4	↑4	↓4
16	4n+1	↑4	↓4	↓4	↑4	↑4	↓4	↓4	↑4
	4n+2	↓4	↑4	↑4	↓4	↓4	↑4	↑4	↓4
	4n+3	↑4	↓4	↓4	↑4	↑4	↓4	↓4	↑4
	4n+4	↓4	↑4	↑4	↓4	↓4	↑4	↑4	↓4
17	4n+1	↑5	↓5	↓4	↑4	↑4	↓4	↓4	↑4
	4n+2	↓4	↑4	↑4	↓4	↓5	↑5	↑4	↓4
	4n+3	↑4	↓4	↓4	↑4	↑4	↓4	↓5	↑5
	4n+4	↓4	↑4	↑5	↓5	↓4	↑4	↑4	↓4
18	4n+1	↑5	↓5	↓4	↑4	↑5	↓5	↓4	↑4
	4n+2	↓5	↑5	↑4	↓4	↓5	↑5	↑4	↓4
	4n+3	↑4	↓4	↓5	↑5	↑4	↓4	↓5	↑5
	4n+4	↓4	↑4	↑5	↓5	↓4	↑4	↑5	↓5
19	4n+1	↑5	↓5	↓5	↑5	↑5	↓5	↓4	↑4
	4n+2	↓5	↑5	↑4	↓4	↓5	↑5	↑5	↓5
	4n+3	↑5	↓5	↓5	↑5	↑4	↓4	↓5	↑5
	4n+4	↓4	↑4	↑5	↓5	↓5	↑5	↑5	↓5
20	4n+1	↑5	↓5	↓5	↑5	↑5	↓5	↓5	↑5
	4n+2	↓5	↑5	↑5	↓5	↓5	↑5	↑5	↓5
	4n+3	↑5	↓5	↓5	↑5	↑5	↓5	↓5	↑5
	4n+4	↓5	↑5	↑5	↓5	↓5	↑5	↑5	↓5
21	4n+1	↑6	↓6	↓5	↑5	↑5	↓5	↓5	↑5
	4n+2	↓5	↑5	↑5	↓5	↓6	↑6	↑5	↓5
	4n+3	↑5	↓5	↓5	↑5	↑5	↓5	↓6	↑6
	4n+4	↓5	↑5	↑6	↓6	↓5	↑5	↑5	↓5

Remarks 1. n: Integer from 0 to 31.

2. ↑A: Rising edge of pulse during line A output.

3. ↓A: Rising edge of pulse at start of line A output.

4. A: PWM pulse width (A/8)

Table 5-15. Example of Pulse Width Modulated Output (3/3)

Gray-scale level	COM	1, 2 Frames		3, 4 Frames		5, 6 Frames		7, 8 Frames	
		SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered
22	4n+1	↑6	↓6	↓5	↑5	↑6	↓6	↓5	↑5
	4n+2	↓6	↑6	↑5	↓5	↓6	↑6	↑5	↓5
	4n+3	↑5	↓5	↓6	↑6	↑5	↓5	↓6	↑6
	4n+4	↓5	↑5	↑6	↓6	↓5	↑5	↑6	↓6
23	4n+1	↑6	↓6	↓6	↑6	↑6	↓6	↓5	↑5
	4n+2	↓6	↑6	↑5	↓5	↓6	↑6	↑6	↓6
	4n+3	↑6	↓6	↓6	↑6	↑5	↓5	↓6	↑6
	4n+4	↓5	↑5	↑6	↓6	↓6	↑6	↑6	↓6
24	4n+1	↑6	↓6	↓6	↑6	↑6	↓6	↓6	↑6
	4n+2	↓6	↑6	↑6	↓6	↓6	↑6	↑6	↓6
	4n+3	↑6	↓6	↓6	↑6	↑6	↓6	↓6	↑6
	4n+4	↓6	↑6	↑6	↓6	↓6	↑6	↑6	↓6
25	4n+1	↑7	↓7	↓6	↑6	↑6	↓6	↓6	↑6
	4n+2	↓6	↑6	↑6	↓6	↓7	↑7	↑6	↓6
	4n+3	↑6	↓6	↓6	↑6	↑6	↓6	↓7	↑7
	4n+4	↓6	↑6	↑7	↓7	↓6	↑6	↑6	↓6
26	4n+1	↑7	↓7	↓6	↑6	↑7	↓7	↓6	↑6
	4n+2	↓7	↑7	↑6	↓6	↓7	↑7	↑6	↓6
	4n+3	↑6	↓6	↓7	↑7	↑6	↓6	↓7	↑7
	4n+4	↓6	↑6	↑7	↓7	↓6	↑6	↑7	↓7
27	4n+1	↑7	↓7	↓7	↑7	↑7	↓7	↓6	↑6
	4n+2	↓7	↑7	↑6	↓6	↓7	↑7	↑7	↓7
	4n+3	↑7	↓7	↓7	↑7	↑6	↓6	↓7	↑7
	4n+4	↓6	↑6	↑7	↓7	↓7	↑7	↑7	↓7
28	4n+1	↑7	↓7	↓7	↑7	↑7	↓7	↓7	↑7
	4n+2	↓7	↑7	↑7	↓7	↓7	↑7	↑7	↓7
	4n+3	↑7	↓7	↓7	↑7	↑7	↓7	↓7	↑7
	4n+4	↓7	↑7	↑7	↓7	↓7	↑7	↑7	↓7
29	4n+1	8	8	↓7	↑7	↑7	↓7	↓7	↑7
	4n+2	↓7	↑7	↑7	↓7	8	8	↑7	↓7
	4n+3	↑7	↓7	↓7	↑7	↑7	↓7	8	8
	4n+4	↓7	↑7	8	8	↓7	↑7	↑7	↓7
30	4n+1	8	8	↓7	↑7	8	8	↓7	↑7
	4n+2	8	8	↑7	↓7	8	8	↑7	↓7
	4n+3	↑7	↓7	8	8	↑7	↓7	8	8
	4n+4	↓7	↑7	8	8	↓7	↑7	8	8
31	4n+1	8	8	8	8	8	8	↓7	↑7
	4n+2	8	8	↑7	↓7	8	8	8	8
	4n+3	8	8	8	8	↑7	↓7	8	8
	4n+4	↓7	↑7	8	8	8	8	8	8
32	4n+1	8	8	8	8	8	8	8	8
	4n+2	8	8	8	8	8	8	8	8
	4n+3	8	8	8	8	8	8	8	8
	4n+4	8	8	8	8	8	8	8	8

Remarks 1. n: Integer from 0 to 31.

2. ↑A: Rising edge of pulse during line A output.

3. ↓A: Rising edge of pulse at start of line A output.

4. A: PWM pulse width (A/8)

5.7.2 Full-dot frame rate control

When combined with pulse width modulation as described in Table 5-15, the μPD16488A's frame speed is based on 8-frame cycles. The subsampling pattern is output based on the palette stored in the IC.

Full-Dot Gray-Scale Palette (Output Pulse Width: x/8 Pulses)

Gray Scale	Frames								Comments
	1	2	3	4	5	6	7	8	
Level 0	0	0	0	0	0	0	0	0	OFF data
Level 1	1	1	0	0	0	0	0	0	
Level 2	1	1	0	0	1	1	0	0	
Level 3	1	1	1	1	1	1	0	0	
Level 4	1	1	1	1	1	1	1	1	
Level 5	2	2	1	1	1	1	1	1	
Level 6	2	2	1	1	2	2	1	1	
Level 7	2	2	2	2	2	2	1	1	
Level 8	2	2	2	2	2	2	2	2	
Level 9	3	3	2	2	2	2	2	2	
Level 10	3	3	2	2	3	3	2	2	
Level 11	3	3	3	3	3	3	2	2	
Level 12	3	3	3	3	3	3	3	3	
Level 13	4	4	3	3	3	3	3	3	
Level 14	4	4	3	3	4	4	3	3	
Level 15	4	4	4	4	4	4	3	3	
Level 16	4	4	4	4	4	4	4	4	50%
Level 17	5	5	4	4	4	4	4	4	
Level 18	5	5	4	4	5	5	4	4	
Level 19	5	5	5	5	5	5	4	4	
Level 20	5	5	5	5	5	5	5	5	
Level 21	6	6	5	5	5	5	5	5	
Level 22	6	6	5	5	6	6	5	5	
Level 23	6	6	6	6	6	6	5	5	
Level 24	6	6	6	6	6	6	6	6	
Level 25	7	7	6	6	6	6	6	6	
Level 26	7	7	6	6	7	7	6	6	
Level 27	7	7	7	7	7	7	6	6	
Level 28	7	7	7	7	7	7	7	7	
Level 29	8	8	7	7	7	7	7	7	
Level 30	8	8	7	7	8	8	7	7	
Level 31	8	8	8	8	8	8	7	7	
Level 32	8	8	8	8	8	8	8	8	100%

Remark The gradation in the Comments column are images of the gray-scale level.

5.7.3 Line shift driver

If the frame rate control is performed with equal pulse widths and the same gray scale is displayed on the LCD's full screen, problems such as flickering may occur on the LCD panel. The μPD16488A provides a line shift driver as a countermeasure against such screen image problems.

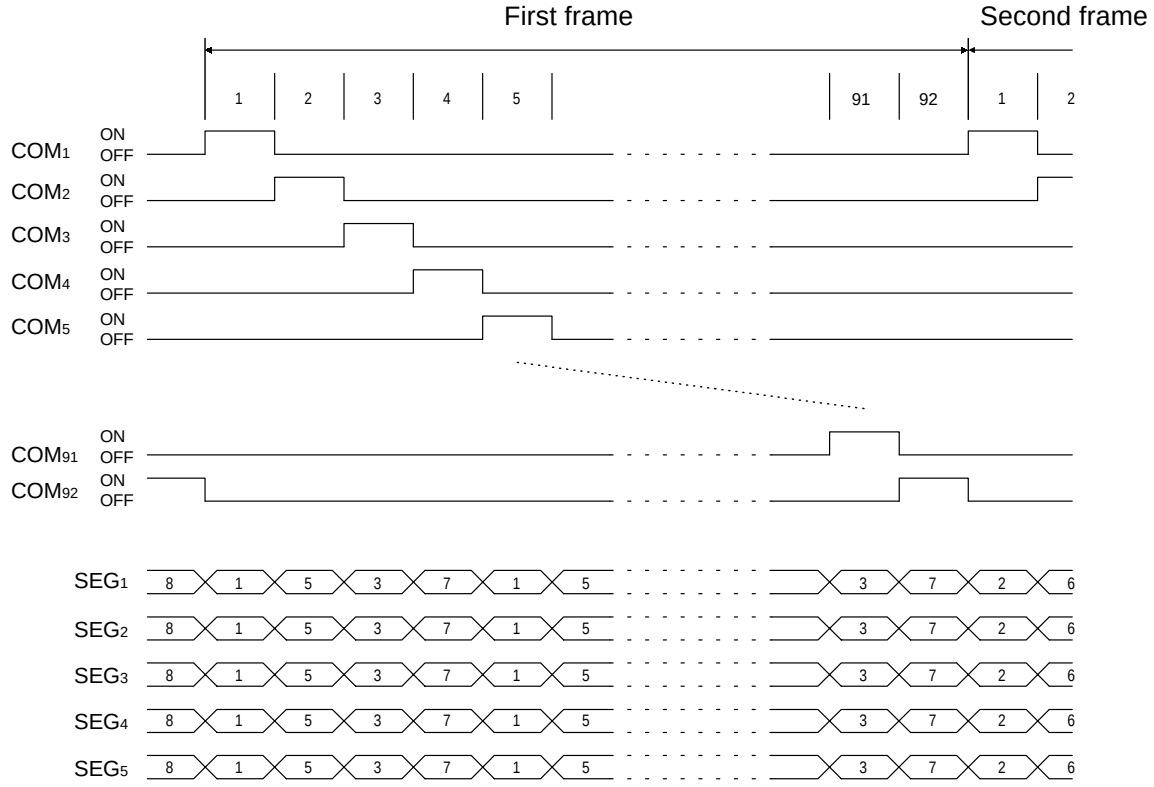
Using 8 frames per cycle, the segment PWM output timing is shifted among the common outputs, as shown in Table 5-16 below.

Table 5-16. Line Shift Driver

	Turn 1								Turn 2											
Frame	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4
COM_1	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4
COM_2	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8
COM_3	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6
COM_4	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2
COM_5	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4
COM_6	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8
COM_7	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6
COM_8	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2
COM_9	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4
COM_{10}	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

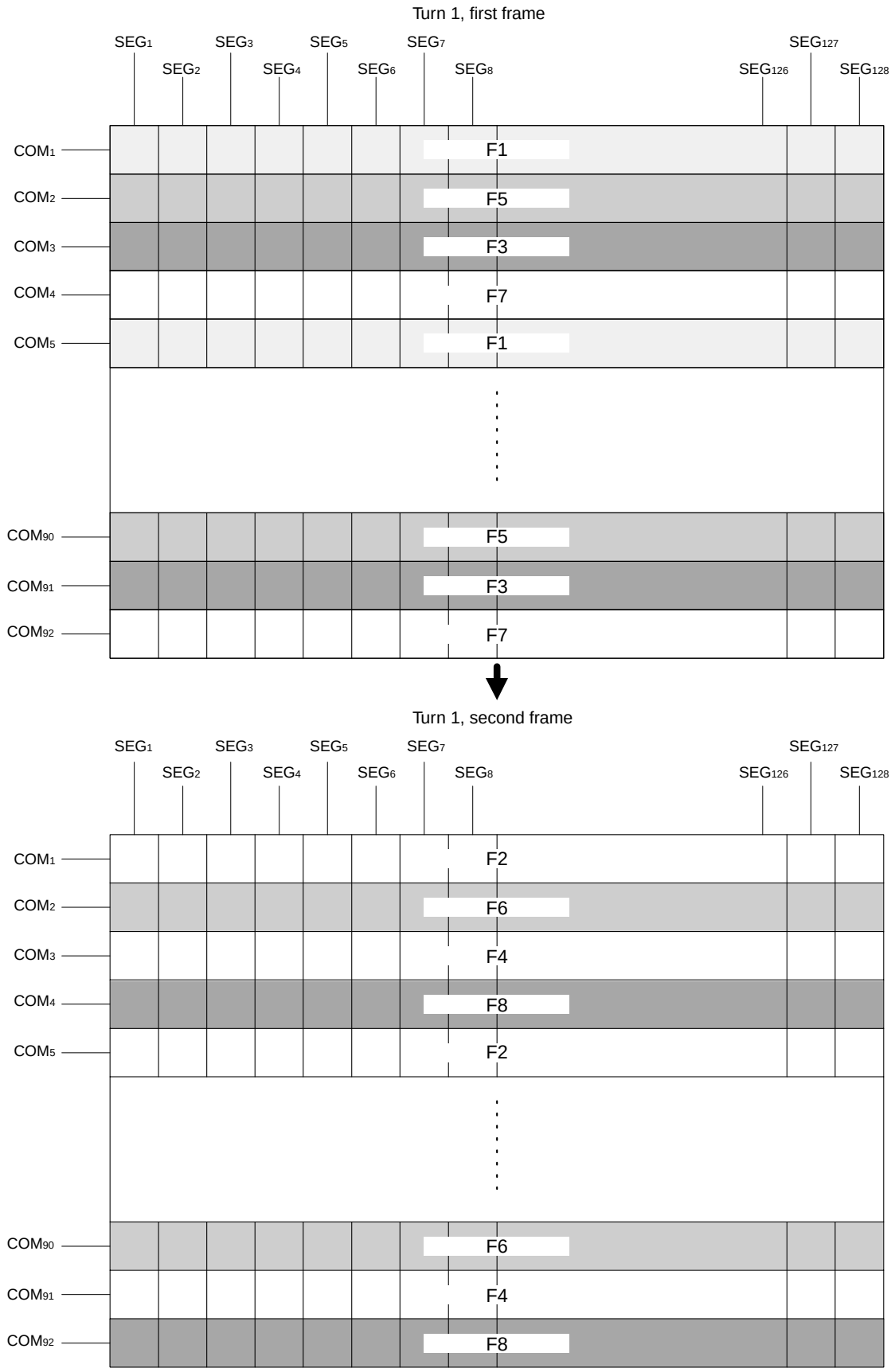
Remark Fx: Pulse width modulated output frame (See **5.7.2 Full-dot frame rate control**).

Figure 5-22. Full Dot Frame Rate Control



Remark Numerical values in the segment data correspond to the gray-scale palette's frame numbers.

Figure 5-23. Line Shift Driver Image



5.7.4 Display size settings

The μPD16488A can be set for any duty value from 1/1 to 1/92. This duty setting can be made via bits DT6 to DT0 in the duty setting register (R5), as shown in Table 5-17.

Table 5-17. Duty Settings

DT6	DT5	DT4	DT3	DT2	DT1	DT0	Duty
0	0	0	0	0	0	0	1/1
0	0	0	0	0	0	1	1/2
0	0	0	0	0	1	0	1/3
0	0	0	0	0	1	1	1/4
			:				:
1	0	1	1	0	0	1	1/90
1	0	1	1	0	1	0	1/91
1	0	1	1	0	1	1	1/92
1	0	1	1	1	0	0	prohibited

Caution The duty setting can not be over 1/92 duty (5CH). If 1/92 duty is exceeded, operation is not guaranteed.

5.7.5 Setting of LCD AC driver's inversion cycle and AC driver's inversion position

The μPD16488A enable any setting to be made for the AC driver's inversion position and the inversion position shift amount for each displayed frame via settings made in the AC driver inversion cycle register (R6) and the AC driver inversion position shift register (R7) for normal display mode or via settings made in the partial AC driver inversion cycle register (R8) and the partial AC driver inversion position shift register (R9) for partial display mode.

In normal display mode, the AC driver inversion cycle can be set for any number of inverted (reverse display) lines listed in Table 5-18, based on the NID6 to NID0 bit settings in the AC driver inversion cycle register (R6).

If the screen display size has been changed via settings made in the duty setting register (R5), the NIDn values are automatically overwritten by values from the corresponding DTYn bits.

The shift amount for each displayed frame can be set as shown in Table 5-19 via settings made to bits MSD6 to MSD0 in the AC driver inversion position shift register (R7).

Table 5-18. Settings of AC Driver Inversion Cycle Register (R6)

NID6	NID5	NID4	NID3	NID2	NID1	NID0	Inverted Lines
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	2
0	0	0	0	0	1	0	3
0	0	0	0	0	1	1	4
			:				:
1	0	1	1	0	0	1	90
1	0	1	1	0	1	0	91
1	0	1	1	0	1	1	92
1	0	1	1	1	0	0	prohibited

Caution The inversion line can not be over 92-inversion line (5CH). If 92-inversion line is exceeded, operation is not guaranteed.

Table 5-19. Settings of AC Driver Inversion Position Shift Register

MSD6	MSD5	MSD4	MSD3	MSD2	MSD1	MSD0	Inversion Position Shift Amount
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
			:				:
1	0	1	1	0	0	1	89
1	0	1	1	0	1	0	90
1	0	1	1	0	1	1	91
1	0	1	1	1	0	0	prohibited

Caution The inversion position shift amount can not be over 91 (5CH). If 91 is exceeded, operation is not guaranteed.

In partial display mode, the AC driver inversion cycle can be set for any number of inverted (reverse display) lines listed in Table 5-20, based on the PID5 to PID0 bit settings in the partial AC driver inversion cycle register (R8).

The shift amount for each displayed frame can be set as shown in Table 5-21 via settings made to bits PSD5 to PSD0 in the partial AC driver inversion position shift register (R9).

Table 5-20. Settings of Partial AC Driver Inversion Cycle Register (R8)

PID5	PID4	PID3	PID2	PID1	PID0	Inverted Lines
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
		:				:
1	0	0	0	1	1	36
1	0	0	1	0	0	37
1	0	0	1	0	1	38

Table 5-21. Setting of Partial AC Driver Inversion Position Shift Register (R9)

PSD5	PSD4	PSD3	PSD2	PSD1	PSD0	Inversion Position Shift Amount
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
			:			:
1	0	0	0	1	1	35
1	0	0	1	0	0	36
1	0	0	1	0	1	37

Be sure to maintain the following relationship among the display size, AC inversion cycle, and AC inversion position.

Display size (duty) ≥ AC inversion cycle ≥ AC inversion shift amount

Caution Setting a small inversion cycle will cause a reduction in the IC's display drive capacity and an increase in the current consumption. We therefore recommend determining the inversion cycle after making a thorough evaluation of the actual LCD panel.

5.8 Display Modes

5.8.1 Partial display mode

The μPD16488A includes a function for outputting a display that uses only part of the LCD panel. The duty setting for partial display mode can be selected as 1/12, 1/25, or 1/38. Parts of the LCD panel that are outside of the specified display area are scanned with non-select waveforms. The partial start line address register (R21) is used to select which part of the LCD panel to use for the partial display. The display area starts from the start line address and includes the number of lines (12, 25, or 38 lines) that has been specified via the partial display mode setting (R10).

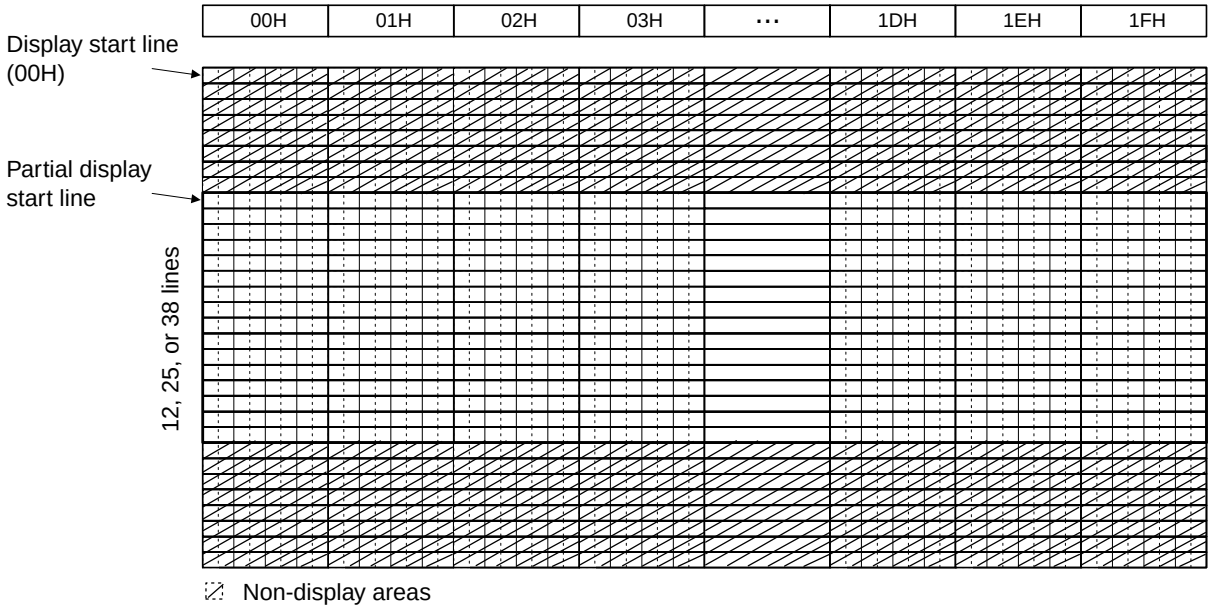
When entering this mode, the booster is set to the boost level number that has been set via the power system control register 3 (partial display boost register) (R34) and the display start line is fixed as 00H. In addition, the bias level is automatically changed to the value that has been set via the partial display mode setting (R10). The relationship between the oscillator's frequency and the frame frequency in partial mode is also automatically changed.

Figure 5-24 shows the mutual relationship between the partial line start address and the LCD display.

When using the partial display mode, the blinking and reverse display functions can be used in the same way as during full-dot display mode.

Caution The LCD driver voltage is lower in partial display mode, because the duty is lower than in normal display mode. There may be restrictions on the usable duty depending on the LCD panel characteristics. We recommend determining the partial duty after making a thorough evaluation of the actual LCD panel.

Figure 5-24. Relationship Between Partial Line Start Address and LCD Display (in Partial Display Mode)



Caution In partial display mode, the display start line setting register (R12) command is ignored.

When switching from normal display mode to partial display mode or from partial display mode to normal display mode, if an electric charge remains in the smoothing capacitor that is connected between the LCD drive voltage pins (V_{LCD}, V_{LC1} to V_{LC4}) and the V_{SS} pin, troubles such as a brief all-black display may occur during the mode switching operation. To avoid such troubles, we recommend using the following power-on sequence.

(1) Normal display → partial display switch sequence

DISP = 0	R0	Display OFF
↓		
HPM1 = 1, HPM0 = 0	R32	High power mode settings
↓		
Switch display mode	R1	Control register 2: switch DTY flag
↓		
Wait time		700 ms (stabilization time for LCD drive voltage and booster)[Note]
↓		
HPM1 = X, HPM0 = X	R32	High power mode settings (to mode used during normal display)
↓		
DISP = 1	R0	Display ON, internal operations status

Note This 700 ms wait time indicates the time for the V_{LCD} level to change from 15 V to 6 V and thus varies according to the panel characteristics and the capacitance value of the boost/smoothing capacitor. We recommend determining the wait time after making a thorough evaluation of the actual device.

(2) Partial display → Normal display switch sequence

DISP = 0	R0	Display OFF
↓		
HPM1 = 1, HPM0 = 1	R32	Power ON mode settings
↓		
Switch display mode	R1	Control register 2: switch DTY flag
↓		
Wait time		400 ms (stabilization time for LCD drive voltage and booster)[Note]
↓		
HPM1 = X, HPM0 = X	R32	High power mode settings (to mode used during normal display)
↓		
DISP = 1	R0	Display ON, internal operations status

Note This 400 ms wait time indicates the time for the V_{LCD} level to change from 6 V to 15 V and thus varies according to the panel characteristics and the capacitance value of the boost/smoothing capacitor. We recommend determining the wait time after making a thorough evaluation of the actual device.

5.8.2 Monochrome (black/white) display

The μPD16488A provides both a four-level gray scale display mode and a monochrome display mode.

To switch to the monochrome display mode, set GRAY = H. The display RAM for one screen of monochrome display mode contents is configured as 128 bits x 128 bits (16 x 8 bits). When using these IC's in monochrome display mode, two screens of data can be written to the display RAM and the two screens can be switched by setting the DSEL bit in the control register 2 (R1). Screen 1 is displayed on the LCD panel when DSEL = L and screen 2 is displayed when DSEL = H.

When writing data, the display RAM uses the same X address (00H to 0FH) and Y address and the BWW bit value in the control register 2 (R1) determines which of the two screens the data will be written to: when BWW = L, data is written to screen 1 and when BWW = H, data is written to screen 2, as shown in Figure 5-25.

When accessing a specified bit, specify both the X address and Y address. The display data in D_0 to D_7 (sent from the CPU) corresponds to the SEGx portions of the LCD display, as shown in Figure 5-26. Figure 5-27 shows the relationship between the display data in monochrome display mode and the page/column addresses.

Figure 5-25. Display RAM Image in Monochrome (Black/White) Mode

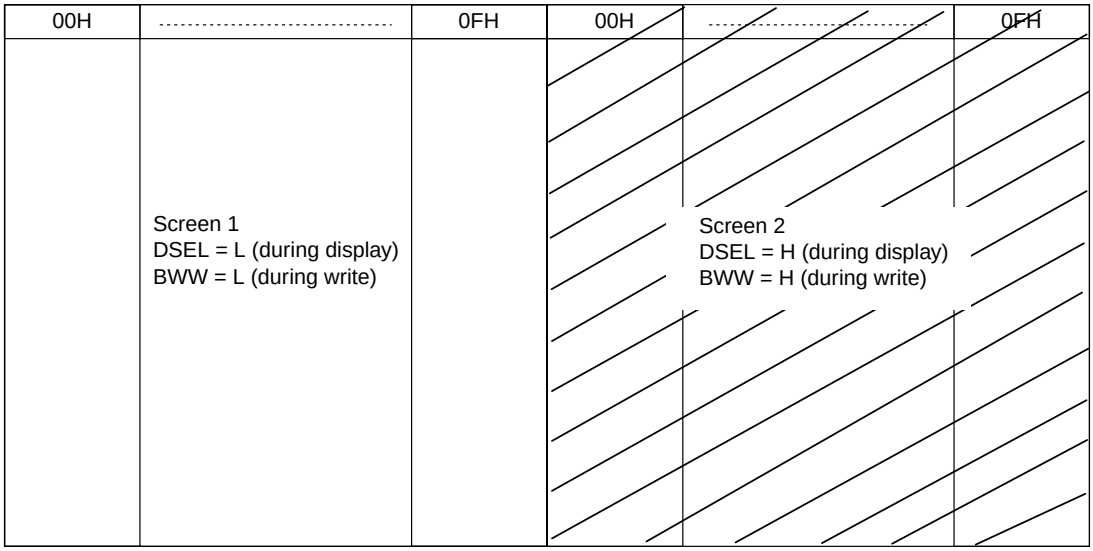


Figure 5-26. Relationship Between Display Data and LCD Display

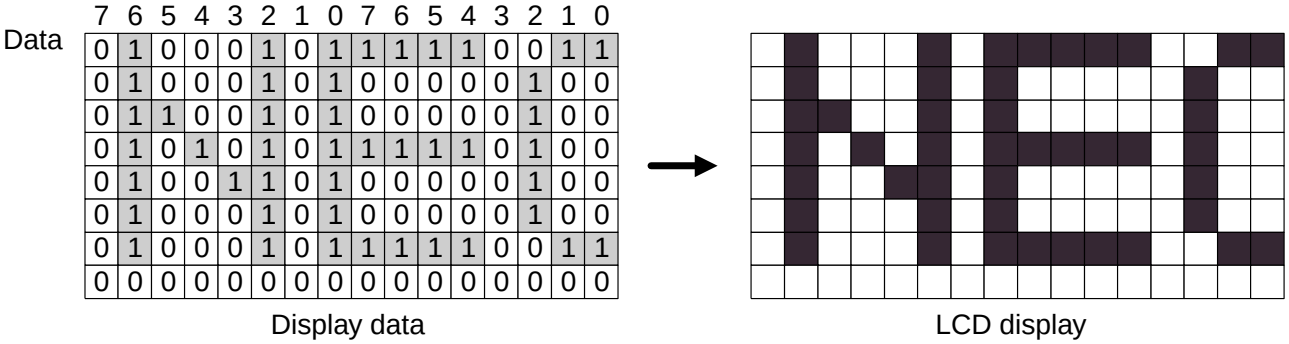
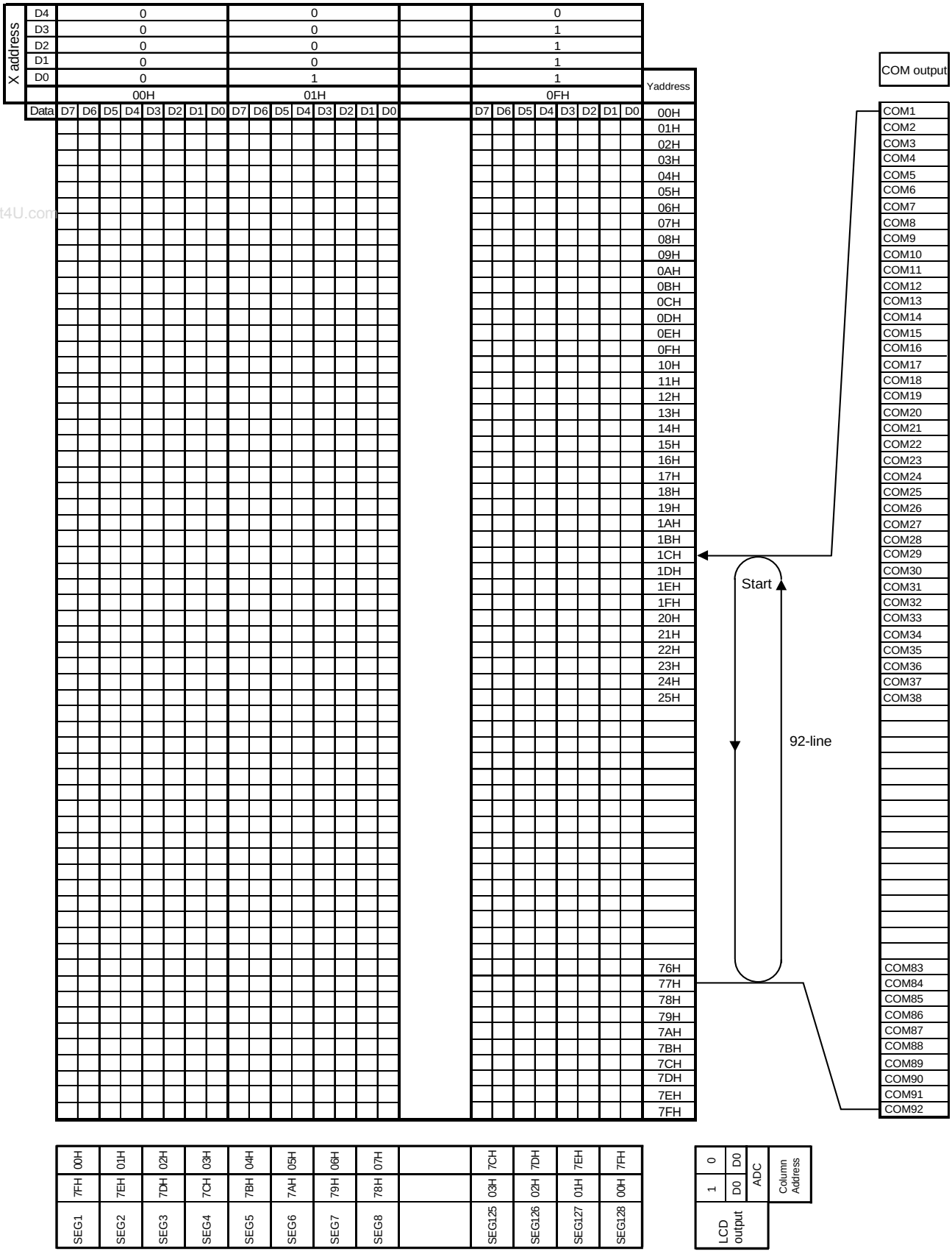


Figure 5-27. Relation Between the Display Data and X/Y Address (in Monochrome Display Mode)



5.9 Reset

In the μPD16488A, a reset is executed when the /RES input is at low level or when a reset command is entered. The IC is reset to its default settings. These default settings are listed in the table below.

Register	Number	/RES	Reset Command
Control register 1	R0	Enabled (DISP flag only)	Enabled
Control register 2	R1	Enabled (IDIS flag only)	
X address register	R3	Disabled	
Y address register	R4		
Duty setting register	R5		Enabled[Note2]
AC driver inversion cycle register	R6		
AC driver inversion position shift register	R7		Enabled
Partial AC driver inversion cycle register	R8		
Partial AC driver inversion position shift register	R9		
Partial display mode setting register	R10		
Display memory access register[Note1]	R11		Disabled
Display start line setting register	R12		Enabled
Blink X address register	R13		
Blink start line address register	R14		
Blink end line address register	R15		
Blink data memory access register[Note1]	R16		Disabled
Inverted X address register	R17		Enabled
Inversion start line address register	R18		
Inversion end line address register	R19		
Inverted data memory access register[Note1]	R20		Disabled
Partial start line address register	R21		Enabled
Gray scale data register 1 (0, 0)	R23		
Gray scale data register 2 (0, 1)	R24		
Gray scale data register 3 (1, 0)	R25		
Gray scale data register 4 (1, 1)	R26		
Partial gray scale data register 1 (0, 0)	R27		
Partial gray scale data register 2 (0, 1)	R28		
Partial gray scale data register 3 (1, 0)	R29		
Partial gray scale data register 4 (1, 1)	R30		
Power system control register 1	R32		
Power system control register 2	R33		
Power system control register 3	R34		
Electronic volume register	R35		
Partial electronic volume register	R36		
Boost adjustment register	R37		
RAM test mode setting register	R44		
Signature read register	R45		Disabled

Enabled: Default value is input, Disabled: Default value is not input

Notes 1. When using the /RES pin to reset, the contents of memory are not retained. Use the reset command to reset if the memory contents need to be retained.

2. Be sure to set this register again after input the reset command.

Cautions 1. Using the /RES pin to reset initializes the shift clock counter.

2. Always input the reset command as the first command after power ON.

6. COMMAND REGISTERS

The μPD16488A uses a combination of RS, /RD (E), and /WR (R,/W) signals to identify data bus signals. Command interpretation and execution is performed using internal timing that does not depend on any external clock. Therefore, processing is very fast and there is usually no need to check for a busy status.

The i80 series CPU interface activates read commands using a low pulse input to the /RD pin and activates write commands using a low pulse input to the /WR pin. The M68 series CPU interface sets read mode using a high level input to the R,/W pin and sets write mode using a low level input to the same pin. It activates both read and write commands using a high-level pulse input to the E pin.

Command descriptions using an i80 series CPU interface are shown as follows. The M68 series CPU interface differs from the i80 series CPU interface in that /RD (E) is at high level during status read and display data read operations, as shown in the following command descriptions and command table.

If the serial interface has been selected, data is input sequentially starting from D_7.

6.1 Control Register 1 (R0)

This command specifies the μPD16488A's general operation modes.

RS	E /RD	R,/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	RMW	DISP	STBY	BLD	IVD	HALT	ADC	COMR

Flag	Function
RMW	0: Address is incremented after both write access and read access. 1: Read/modify/write mode (Address is incremented only after write access)
DISP	0: Display OFF (All LCD output pins output the V_{SS} level and oscillator and DC/DC converter are operating) 1: Display ON
STBY	0: Normal operation 1: Internal operation and oscillation are stopped. Display is OFF.
BLD	The blinking dots are specified via the blink start/end line address registers and data is set to blink data RAM. 0: Stop blinking 1: Start blinking
IVD	The number of inverted dots is specified via the inversion start/end line address registers and data is set to inverted data RAM. 0: Stop inversion 1: Start inversion
HALT	0: Start internal operation 1: Stop internal operation (since different display modes are used, when switching between partial and normal display modes, the LCD output pins all output the V_{SS} level and the oscillator is operating, but the DC/DC converter is stopped)
ADC **Note**	The column address corresponding to the SEG outputs (see **Table 6-1**) for displaying the contents of the display data RAM.
COMR **Note**	This inverts (reverses) the scan direction for common outputs. (See **Table 6-2**)

Note The reset command must be executed before changing this flag's setting.

Table 6-1. Relationship between Display RAM Column Address and SEG Outputs

SEG Output		SEG_1				SEG_{128}
ADC	0	00H	→	Column addresses	→	7FH
(D_1)	1	7FH	←	Column addresses	←	00H

Table 6-2. Relationship between Common Scan Circuit and Scan Direction

COM Output		Scan Direction		
COMR	0	COM_1	→	COM_{92}
(D_0)	1	COM_{92}	→	COM_1

Default settings (initial values set by reset command)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

6.2 Control Register 2 (R1)

This command specifies the μPD16488A's general operation modes.

RS	E /RD	R,/W /WR	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	FDM	–	–	DSEL	BWW	GRAY	DTY	INC

Flag	Function
FDM	Settings for full screen display mode 0: Normal operation 1: Full screen display (set entire screen to ON) (When using four-level gray scale, gray-scale level 32 is output for full screen display).
DSEL	Selects display screen during monochrome display mode. 0: Screen 1 1: Screen 2
BWW	Selects data write screen during monochrome display mode. 0: Screen 1 1: Screen 2
GRAY Note	0: 4-level gray scale display mode 1: Monochrome display mode
DTY Note	0: Normal display mode (1/1 to 1/128 duty) 1: Partial display mode (1/12, 1/25, or 1/38 duty, 1/5 or 1/6 bias)
INC	0: Increments X address at each access 1: Increments Y address at each access

Note The HALT command must be executed before changing this flag's setting.

Table 6-3. Relationship between IC's Functions and Display Modes

Item	Normal Display Mode (DTY = 0)		Partial Display Mode (DTY = 1)
Duty	1/1 to 1/92 duty	↔	1/12, 1/25, or 1/38 duty
Booster	×4, ×5, ×6, ×7, ×8, ×9	↔	×2, ×3, ×4
Bias level	1/11, 1/12, 1/10, 1/9, 1/8, 1/7	↔	1/5, 1/6
Gray scale data	Uses levels set to the gray scale data registers (R23 to R26)	↔	Uses levels set to the partial gray scale data registers (R27 to R30)
(1+Rb/Ra) V_{LCD} regulator resistance factor	Uses values of VRR2 to VRR0 in the power system control register 2 (R33)	↔	Uses values of PVR2 to PVR0 in the power system control register 2 (R33)
Electronic volume	Uses value from the electronic volume register (R35)	↔	Uses value from the partial electronic volume register (R36)

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

6.3 Reset Command (R2)

★ When this command is input, the IC's registers (R0 to R44) are reset to their initial values. However, the contents of memory are retained.

Always input the reset command as the first command after power application.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	0	1

6.4 X Address Register (R3)

The X address register specifies the X address in the display RAM accessed by the CPU. This address is automatically incremented each time the display RAM is accessed (INC = 0, RMW = 0).

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	–	–	–	XA4	XA3	XA2	XA1	XA0

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
–	–	–	0	0	0	0	0

6.5 Y Address Register (R4)

The Y address register specifies the Y address in the display RAM accessed by the CPU. This address is automatically incremented each time the display RAM is accessed (INC = 1, RMW = 0).

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	–	YA6	YA5	YA4	YA3	YA2	YA1	YA0

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
–	0	0	0	0	0	0	0

6.6 Duty Setting Register (R5)

The display duty can be set to any duty ratio between 1/1 and 1/92, as is shown in Table 6-4.

Before modifying this register, be sure to use the HALT command (control register 1 (R0)) to stop internal operations.

Also, be sure to set this register again after input the reset command.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	–	DT6	DT5	DT4	DT3	DT2	DT1	DT0

Table 6-4. Duty Setting Register (R5) Settings

DT6	DT5	DT4	DT3	DT2	DT1	DT0	Duty
0	0	0	0	0	0	0	1/1
0	0	0	0	0	0	1	1/2
0	0	0	0	0	1	0	1/3
0	0	0	0	0	1	1	1/4
			:				:
1	0	1	1	0	0	1	1/90
1	0	1	1	0	1	0	1/91
1	0	1	1	0	1	1	1/92
1	0	1	1	0	0	0	inhibited

Caution The display size can not be over 1/92 duty (5CH). If 1/92 duty is exceeded, operation is not guaranteed.

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
–	–	–	–	–	–	–	–

6.7 AC Driver Inversion Cycle Register (R6)

The AC driver's line position for normal display mode can be set as shown in Table 6-5.

When a DTYn value is changed in the duty setting register (R5), the NIDn value is automatically overwritten by the DTYn value.

Be sure to set this register again after input the reset command.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	–	NID6	NID5	NID4	NID3	NID2	NID1	NID0

Table 6-5. AC Driver Inversion Cycle Register (R6) Settings

NID6	NID5	NID4	NID3	NID2	NID1	NID0	Inversion Line
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	2
0	0	0	0	0	1	0	3
0	0	0	0	0	1	1	4
			:				:
1	0	1	1	0	0	1	90
1	0	1	1	0	1	0	91
1	0	1	1	0	1	1	92
1	0	1	1	1	0	0	Inhibited

Caution The inversion line can not be over 92 (5CH). If 92-line is exceeded, operation is not guaranteed.

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
–	–	–	–	–	–	–	–

6.8 AC Driver Inversion Position Shift Register (R7)

This register shifts the inversion position for each frame in normal display mode by the shift amount shown in Table 6-6.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	–	MSD6	MSD5	MSD4	MSD3	MSD2	MSD1	MSD0

Table 6-6. AC Driver Inversion Position Shift Register (R7) Settings

MSD5	MSD5	MSD4	MSD3	MSD2	MSD1	MSD0	Inversion Position Shift Amount
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
			:				:
1	0	1	1	0	0	1	89
1	0	1	1	0	1	0	90
1	0	1	1	0	1	1	91
1	0	1	1	1	0	0	92

Caution The inversion position shift amount can not be over 91 (5CH). If 91 is exceeded, operation is not guaranteed.

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
–	0	0	0	0	0	0	0

6.9 Partial AC Driver Inversion Cycle Register (R8)

The AC driver's line position can be set as shown in Table 6-7.

When a PDTn value is changed in the partial display mode setting register (R10), the PIDn value is automatically overwritten by the PDTn value.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	–	–	PID5	PID4	PID3	PID2	PID1	PID0

Table 6-7. Partial AC Driver Inversion Cycle Register (R8) Settings

PID5	PID4	PID3	PID2	PID1	PID0	Inversion Line
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
			:			:
1	0	0	0	1	1	36
1	0	0	1	0	0	37
1	0	0	1	0	1	38

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
–	–	1	0	0	1	0	1

6.10 Partial AC Driver Inversion Position Shift Register (R9)

This register shifts the inversion position for each frame by the shift amount shown in Table 6-8.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	–	–	PSD5	PSD4	PSD3	PSD2	PSD1	PSD0

Table 6-8. Partial AC Driver Inversion Position Shift Register (R9) Settings

PSD5	PSD4	PSD3	PSD2	PSD1	PSD0	Inversion Position Shift Amount
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
		:				:
1	0	0	0	1	1	35
1	0	0	1	0	0	36
1	0	0	1	0	1	37

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
–	–	–	0	0	0	0	0

6.11 Partial Display Mode Setting Register (R10)

This command specifies the operation mode to be used in the μPD16488A's partial display mode.

Before modifying this register, be sure to use the HALT command (control register 1 (R0)) to stop internal operations.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	–	–	–	–	PBIS	–	PDT1	PDT0

Flag	Function		
PBIS	Sets bias level for partial display mode 0: 1/5 bias 1: 1/6 bias		
PDT1, PDT0	PDT1	PDT0	Duty in partial display mode
	0	0	1/38 duty
	0	1	1/25 duty
	1	0	1/12 duty
	1	1	Prohibited

★ **Caution With the setting of 1/12 duty, the level voltage (V_{LCn}) for driving liquid crystal pannel may not reach the set value depending on the panel used. Thoroughly evaluate the relationship between the duty and driving voltage with the actual system.**

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
–	–	–	–	0	–	0	0

6.12 Display Memory Access Register (R11)

The display memory access register is used when accessing the display RAM. When this register is write-accessed, data is written directly to the display RAM. When this register is read-accessed, data from the display RAM is first latched to this register before being sent to the bus during the next read operation. Accordingly, one dummy read access is required after display RAM access has been set.

★ When using reset command to reset, the contents of memory are retained.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
–	–	–	–	–	–	–	–

6.13 Display Start Line Setting Register (R12)

Display start line set specifies the top line in the display.

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	–	DSL6	DSL5	DSL4	DSL3	DSL2	DSL1	DSL0

Default settings (initial values set by reset command)

D7	D6	D5	D4	D3	D2	D1	D0
–	0	0	0	0	0	0	0

6.14 Blink X Address Register (R13)

The blink X address register specifies the X address of the blink data RAM accessed by the CPU. This address is automatically incremented each time the blink data RAM is accessed.

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	–	–	–	–	BXA3	BXA2	BXA1	BXA0

Default settings (initial values set by reset command)

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	0	0	0	0

6.15 Blink Start Line Address Register (R14)

The blink start line address register specifies the start line address of the display RAM accessed when the CPU uses blink display mode. The range of blinking lines is determined based on the contents of this register and the blink end line address register.

RS	D7	D6	D5	D4	D3	D2	D1	D0	Setting
1	–	BSL6	BSL5	BSL4	BSL3	BSL2	BSL1	BSL0	–

Default settings (initial values set by reset command)

D7	D6	D5	D4	D3	D2	D1	D0
–	0	0	0	0	0	0	0

6.16 Blink End Line Address Register (R15)

The blink end line address register specifies the end line address of the display RAM accessed when the CPU uses blink display mode. The range of blinking lines is determined based on the contents of this register and the blink start line address register.

RS	D7	D6	D5	D4	D3	D2	D1	D0	Setting
1	–	BEL6	BEL5	BEL4	BEL3	BEL2	BEL1	BEL0	–

Default settings (initial values set by reset command)

D7	D6	D5	D4	D3	D2	D1	D0
–	0	0	0	0	0	0	0

6.17 Blink Data Memory Access Register (R16)

The blink data memory access register is used to access the blink data RAM. When this register is write-accessed, data is written directly to the blink data RAM.

★ When using reset command to reset, the contents of memory are retained.

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	D7	D6	D5	D4	D3	D2	D1	D0

Data	Status
0	Normal
1	Blink

Default settings (initial values set by reset command, all data)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

6.18 Inverted X Address Register (R17)

The inverted X address register specifies the X address in the inverted data RAM accessed by the CPU. This address is incremented each time the inversion RAM is accessed.

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	–	–	–	–	IXA3	IXA2	IXA1	IXA0

Default settings (initial values set by reset command)

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	0	0	0	0

6.19 Inversion Start Line Address Register (R18)

The inversion start line address register specifies the start line address in the display RAM accessed by the CPU when using reverse (inverted) display mode. The range of inverted lines is determined based on the contents of this register and the inversion end line address register.

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	–	ISL6	ISL5	ISL4	ISL3	ISL2	ISL1	ISL0

Default settings (initial values set by reset command)

D7	D6	D5	D4	D3	D2	D1	D0
–	0	0	0	0	0	0	0

6.20 Inversion End Line Address Register (R19)

The inversion end line address register specifies the end line address in the display RAM accessed by the CPU when using reverse (inverted) display mode. The range of inverted lines is determined based on the contents of this register and the inversion start line address register.

RS	D7	D6	D5	D4	D3	D2	D1	D0	Setting
1	–	IEL6	IEL5	IEL4	IEL3	IEL2	IEL1	IEL0	–

Default settings (initial values set by reset command)

D7	D6	D5	D4	D3	D2	D1	D0
–	0	0	0	0	0	0	0

6.21 Inverted Data Memory Access Register (R20)

The inverted data memory access register is used when accessing the inverted data RAM. When this register is accessed, the data is written directly to the inverted data RAM.

★ When using reset command to reset, the contents of memory are retained.

RS	D7	D6	D5	D4	D3	D2	D1	D0	Setting
1	D7	D6	D5	D4	D3	D2	D1	D0	–

Data	Status
0	Normal
1	Inverted

Default settings (initial values set by reset command, all data)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

6.22 Partial Start Line Address Register (R21)

The partial start line address register specifies the start line address in the display RAM accessed by the CPU when using partial display mode. The partial display area is determined as the number of lines specified in the partial display mode setting register (R10), starting from this start line address.

RS	D7	D6	D5	D4	D3	D2	D1	D0	Setting
1	–	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	–

Default settings (initial values set by reset command)

D7	D6	D5	D4	D3	D2	D1	D0
–	0	0	0	0	0	0	0

6.23 Gray Scale Data Registers 1 to 4 (R23 to R26)

The gray scale data registers specify the gray scale level when using normal four-level gray scale display mode. Use of this register optimizes the gray scale display.

Rx	Data	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
R23	0, 0	1	–	–	GD5	GD4	GD3	GD2	GD1	GD0	–
R24	0, 1	1	–	–	GD5	GD4	GD3	GD2	GD1	GD0	–
R25	1, 0	1	–	–	GD5	GD4	GD3	GD2	GD1	GD0	–
R26	1, 1	1	–	–	GD5	GD4	GD3	GD2	GD1	GD0	–

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Gray scale level
Disable	Disable	0	0	0	0	0	0	Level 0
Disable	Disable	0	0	0	0	0	1	Level 1
Disable	Disable	0	0	0	0	1	0	Level 2
Disable	Disable	0	0	0	0	1	1	Level 3
			:					:
Disable	Disable	0	1	1	1	1	1	Level 31
Disable	Disable	1	0	0	0	0	0	Level 32

Default settings (initial values set by reset command, for all gray scale data registers)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
–	–	0	0	0	0	0	0

6.24 Partial Gray Scale Data Registers 1 to 4 (R27 to R30)

The partial gray scale data registers specify the gray scale level when using partial four-level gray scale display mode. Use of this register optimizes the gray scale display.

Rx	Data	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
R27	0, 0	1	–	–	PGD5	PGD4	PGD3	PGD2	PGD1	PGD0	–
R28	0, 1	1	–	–	PGD5	PGD4	PGD3	PGD2	PGD1	PGD0	–
R29	1, 0	1	–	–	PGD5	PGD4	PGD3	PGD2	PGD1	PGD0	–
R30	1, 1	1	–	–	PGD5	PGD4	PGD3	PGD2	PGD1	PGD0	–

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Gray scale level
Disable	Disable	0	0	0	0	0	0	Level 0
Disable	Disable	0	0	0	0	0	1	Level 1
Disable	Disable	0	0	0	0	1	0	Level 2
Disable	Disable	0	0	0	0	1	1	Level 3
			:					:
Disable	Disable	0	1	1	1	1	1	Level 31
Disable	Disable	1	0	0	0	0	0	Level 32

Default settings (initial values set by reset command, for all partial gray scale data registers)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
–	–	0	0	0	0	0	0

6.25 Power System Control Register 1 (R32)

This command sets the μPD16488A's power system mode.

RS	E /RD	R,/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	HPM1	HPM0	–	TCS1	TCS0	OP2	OP1	OP0

Flag	Function
HPM1, HPM0	These flags set the driver mode as shown in Table 6-9.
TCS1, TCS0	These flags set the value for selecting the V_{REG} voltage's temperature curve, as shown in Table 6-10.
OP2 to OP0	These flags control the booster's ON/OFF status, the voltage regulator (V regulator) and voltage follower (V/F). The functions controlled via these three bits by the power control setting command are listed in Table 6-11.

Table 6-9. Driver Mode Setting

HPM1	HPM0	Mode Setting
0	0	Normal mode
0	1	Low-power mode
1	0	High-power mode
1	1	Power activation mode

Table 6-10. Selection V_{REG} Voltage's Temperature Curve Value

TCS1	TCS0	Temperature gradient (%/°C)	V_{REG} (TYP.) (V)
0	0	−0.06	1.04
0	1	−0.08	0.98
1	0	−0.09	0.93
1	1	−0.12	0.85

Table 6-11. Detailed Description of Functions Controlled by Flags of Power System Control 1

Item		Status 1	Status 0
OP2	Booster control flag	ON	OFF
OP1	V regulator control flag	ON	OFF
OP0	Voltage follower control flag	ON	OFF

Default settings (initial values set by reset command)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	–	0	0	1	1	1

6.26 Power System Control Register 2 (R33)

This command is used to control the on-chip register for V_{LCD} voltage regualation.

RS	E /RD	R,/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
1	1	0	–	VRR2	VRR1	VRR0	–	PVR2	PVR1	PVR0	–

Flag	Function
VRR2 to VRR0	When using normal display mode, power system control 2 (V_{LCD} regulator resistance factor setting command) can be used to change the resistance factor at 8 levels. The three flags in power system control 2 set the values shown in Table 6-12 as reference values for (1 + Rb/Ra).
PVR2 to PVR0	When using partial display mode, power system control 2 (V_{LCD} regulator resistance factor setting command) can be used to change the resistance factor at 8 levels. The three flags in power system control 2 set the values shown in Table 6-12 as reference values for (1 + Rb/Ra).

Table 6-12. Reference Values for V_{LCD} Internal Resistance Factor Regulator Register

Register			1+Rb/Ra
VRR2	VRR1	VRR0	
PVR2	PVR1	PVR0	
0	0	0	5
0	0	1	8
0	1	0	12
0	1	1	13
1	0	0	16
1	0	1	19
1	1	0	21
1	1	1	24

Default settings (initial values set by reset command)

D7	D6	D5	D4	D3	D2	D1	D0
–	0	0	0	–	0	0	0

6.27 Power System Control Register 3 (R34)

This command sets the power system mode, including the bias setting for the μPD16488A's normal display mode and the number of boost levels for partial display mode.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1	BIS2	BIS1	BIS0	FBS2	FBS1	FBS0	BST1	BST0	–

Flag	Function			
BIS2 to BIS0 Note	These three flags select the bias ratio as shown below.			
	BIS2	BIS1	BIS0	Bias ratio
	0	0	0	1/12 bias
	0	0	1	1/11 bias
	0	1	0	1/10 bias
	0	1	1	1/9 bias
	1	0	0	1/8 bias
	1	0	1	1/7 bias
	1	1	0	Prohibited
	1	1	1	Prohibited
	When partial display mode is set, the bias ratio set by the partial mode setting register (R10) is automatically selected.			
FBS2 to FBS0 Note	The number of boost levels in booster for normal display mode is selected as shown below.			
	FBS2	FBS1	FBS0	Boost level
	0	0	0	x4
	0	0	1	x5
	0	1	0	x6
	0	1	1	x7
	1	0	0	x8
	1	0	1	x9
	1	1	0	Prohibited
	1	1	1	Prohibited
BST1, BST0	The number of boost levels in the booster for partial display mode is selected as shown below.			
	BST1	BST0	Boost level	
	0	0	x2	
	0	1	x3	
	1	0	x4	
	1	1	Prohibited	

Note Be sure to execute the HALT command before changing these flag settings.

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

6.28 Electronic Volume Register (R35)

The electronic volume register specifies the electronic volume value for adjusting the contrast when using normal display mode. Any value among 256 steps can be selected.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	–

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

6.29 Partial Electronic Volume Register (R36)

The partial electronic volume register specifies the electronic volume value for adjusting the contrast when using partial display mode. Any value among 256 steps can be selected.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1	PEV7	PEV6	PEV5	PEV4	PEV3	PEV2	PEV1	PEV0	–

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

6.30 Boost Adjustment Register (R37)

The voltage (range: 1/8 V_{DD2} to 7/8 V_{DD2}) set to this register is applied to the boost level set for the booster.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1	–	–	–	–	–	DDC2	DDC1	DDC0	–

Table 6-13. Boost Adjustment Register (R37) Settings

DDC2	DDC1	DDC0	Boost Adjustment Voltage
0	0	0	Regulator Circuit Stopped
0	0	1	1/8 V_{DD2}
0	1	0	2/8 V_{DD2}
0	1	1	3/8 V_{DD2}
1	0	0	4/8 V_{DD2}
1	0	1	5/8 V_{DD2}
1	1	0	6/8 V_{DD2}
1	1	1	7/8 V_{DD2}

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
–	–	–	–	–	0	0	0

6.31 RAM Test Mode Setting Register (R44)

The RAM test mode setting register directly writes the data for each type of display mode to the display RAM, as shown in Table 6-15.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	–	–	–	–	RTS3	RTS2	RTS1	RTS0

Table 6-15. RAM Test Mode Setting Register (R44) Setting

RTS3	RTS2	RTS1	RTS0	Write Data
0	0	0	0	Normal operation
0	1	0	0	Displays list of gray scales
1	0	0	0	all 00/pixel
1	0	0	1	all 11/pixel
1	0	1	0	Checker pattern: 00/11
1	0	1	1	Checker pattern: 11/00
1	1	0	0	Checker pattern: 01/10
1	1	0	1	Checker pattern: 10/01
1	1	1	0	Vertical striped pattern: 00/11
1	1	1	1	Horizontal striped pattern: 00/11

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
–	–	–	–	0	0	0	0

6.32 Signature Read Register (R45)

This command is used to read the IC signature set via the SIGIN1 and SIGIN2 pins. This is a read-only register.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	–	–	–	–	–	–	SIGIN2	SIGIN1

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
–	–	–	–	–	–	–	–

7. LIST OF μPD16488A REGISTERS

CS	RS	Index Register 5	4	3	2	1	0		Register Name	R/W	Data Bits 7	6	5	4	3	2	1	0
1																		
0	0							IR	Index Register	W			IR5	IR4	IR3	IR2	IR1	IR0
0	1	0	0	0	0	0	0	R0	Control register 1	R/W	RMW	DISP	STBY	BLD	IVD	HALT	ADC	COMR
0	1	0	0	0	0	0	1	R1	Control register 2	R/W	FDM			DSEL	BWW	GRAY	DTY	INC
0	1	0	0	0	0	1	0	R2	Reset command	W								CRES
0	1	0	0	0	0	1	1	R3	X address register	R/W				XA4	XA3	XA2	XA1	XA0
0	1	0	0	0	1	0	0	R4	Y address register	R/W		YA6	YA5	YA4	YA3	YA2	YA1	YA0
0	1	0	0	0	1	0	1	R5	Duty setting register	R/W		DT6	DT5	DT4	DT3	DT2	DT1	DT0
0	1	0	0	0	1	1	0	R6	AC driver inversion cycle register	R/W		NID6	NID5	NID4	NID3	NID2	NID1	NID0
0	1	0	0	0	1	1	1	R7	AC driver inversion position shift register	W		MSD6	MSD5	MSD4	MSD3	MSD2	MSD1	MSD0
0	1	0	0	1	0	0	0	R8	Partial AC driver inversion cycle register	W				PID4	PID3	PID2	PID1	PID0
0	1	0	0	1	0	0	1	R9	Partial AC driver inversion potision shift register	W				PSD4	PSD3	PSD2	PSD1	PSD0
0	1	0	0	1	0	1	0	R10	Partial display mode setting register	R/W					PBIS		PDT1	PDT0
0	1	0	0	1	0	1	1	R11	Display memory access register	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	1	0	0	R12	Display start line setting register	W		DSL6	DSL5	DSL4	DSL3	DSL2	DSL1	DSL0
0	1	0	0	1	1	0	1	R13	Blink X address register	R/W					BXA3	BXA2	BXA1	BXA0
0	1	0	0	1	1	1	0	R14	Blink start line address register	R/W		BSL6	BSL5	BSL4	BSL3	BSL2	BSL1	BSL0
0	1	0	0	1	1	1	1	R15	Blink end line address register	R/W		BEL6	BEL5	BEL4	BEL3	BEL2	BEL1	BEL0
0	1	0	1	0	0	0	0	R16	Blink data memory access register	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	0	0	1	R17	Inverted X address register	R/W					IXA3	IXA2	IXA1	IXA0
0	1	0	1	0	0	1	0	R18	Inversion start line address register	R/W		ISL6	ISL5	ISL4	ISL3	ISL2	ISL1	ISL0
0	1	0	1	0	0	1	1	R19	Inversion end line address register	R/W		IEL6	IEL5	IEL4	IEL3	IEL2	IEL1	IEL0
0	1	0	1	0	1	0	0	R20	Inverted data memory access register	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	1	R21	Partial start line address register	W		PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0
0	1	0	1	0	1	1	0	R22										
0	1	0	1	0	1	1	1	R23	Gray scale data register 1 (0, 0)	W			GD5	GD4	GD3	GD2	GD1	GD0
0	1	0	1	1	0	0	0	R24	Gray scale data register 2 (0, 1)	W			GD5	GD4	GD3	GD2	GD1	GD0
0	1	0	1	1	0	0	1	R25	Gray scale data register 3 (1, 0)	W			GD5	GD4	GD3	GD2	GD1	GD0
0	1	0	1	1	0	1	0	R26	Gray scale data register 4 (1, 1)	W			GD5	GD4	GD3	GD2	GD1	GD0
0	1	0	1	1	0	1	1	R27	Patial gray scale data register 1 (0, 0)	W			PGD5	PGD4	PGD3	PGD2	PGD1	PGD0
0	1	0	1	1	1	0	0	R28	Patial gray scale data register 2 (0, 1)	W			PGD5	PGD4	PGD3	PGD2	PGD1	PGD0
0	1	0	1	1	1	0	1	R29	Patial gray scale data register 3 (1, 0)	W			PGD5	PGD4	PGD3	PGD2	PGD1	PGD0
0	1	0	1	1	1	1	0	R30	Patial gray scale data register 4 (1, 1)	W			PGD5	PGD4	PGD3	PGD2	PGD1	PGD0
0	1	0	1	1	1	1	1	R31										
0	1	1	0	0	0	0	0	R32	Power system control register 1	W	HPM1	HPM0		TCS1	TSC0	OP2	OP1	OP0
0	1	1	0	0	0	0	1	R33	Power system control register 2	W		VRR2	VRR1	VRR0		PVR2	PVR1	PVR0
0	1	1	0	0	0	1	0	R34	Power system control register 3	W	BIS2	BIS1	BIS0	FBS2	FBS1	FBS0	BST1	BST0
0	1	1	0	0	0	1	1	R35	Electronic volume register	W	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0
0	1	1	0	0	1	0	0	R36	Partial electronic volume register	W	PEV7	PEV6	PEV5	PEV4	PEV3	PEV2	PEV1	PEV0
0	1	1	0	0	1	0	1	R37	Boost adjustment register	W						DDC2	DDC1	DDC0
0	1	1	0	0	1	1	0	R38										
0	1	1	0	0	1	1	1	R39										
0	1	1	0	1	0	0	0	R40										
0	1	1	0	1	0	0	1	R41										
0	1	1	0	1	0	1	0	R42										
0	1	1	0	1	0	1	1	R43										
0	1	1	0	1	1	0	0	R44	RAM test mode setting register	W					RTS3	RTS2	RTS1	RTS0
0	1	1	0	1	1	0	1	R45	Signature read register	R							SIG2	SIG1
0	1	1	0	1	1	1	0	R46										
0	1	1	0	1	1	1	1	R47										
0	1	1	1	0	0	0	0	R48										
0	1	1	1	0	0	0	1	R49										
0	1	1	1	0	0	1	0	R50										
0	1	1	1	0	0	1	1	R51										
0	1	1	1	0	1	0	0	R52										
0	1	1	1	0	1	0	1	R53										
0	1	1	1	0	1	1	0	R54										
0	1	1	1	0	1	1	1	R55										
0	1	1	1	1	0	0	0	R56										
0	1	1	1	1	0	0	1	R57										
0	1	1	1	1	0	1	0	R58										
0	1	1	1	1	0	1	1	R59										
0	1	1	1	1	1	0	0	R60										
0	1	1	1	1	1	0	1	R61										
0	1	1	1	1	1	1	0	R62										
0	1	1	1	1	1	1	1	R63										

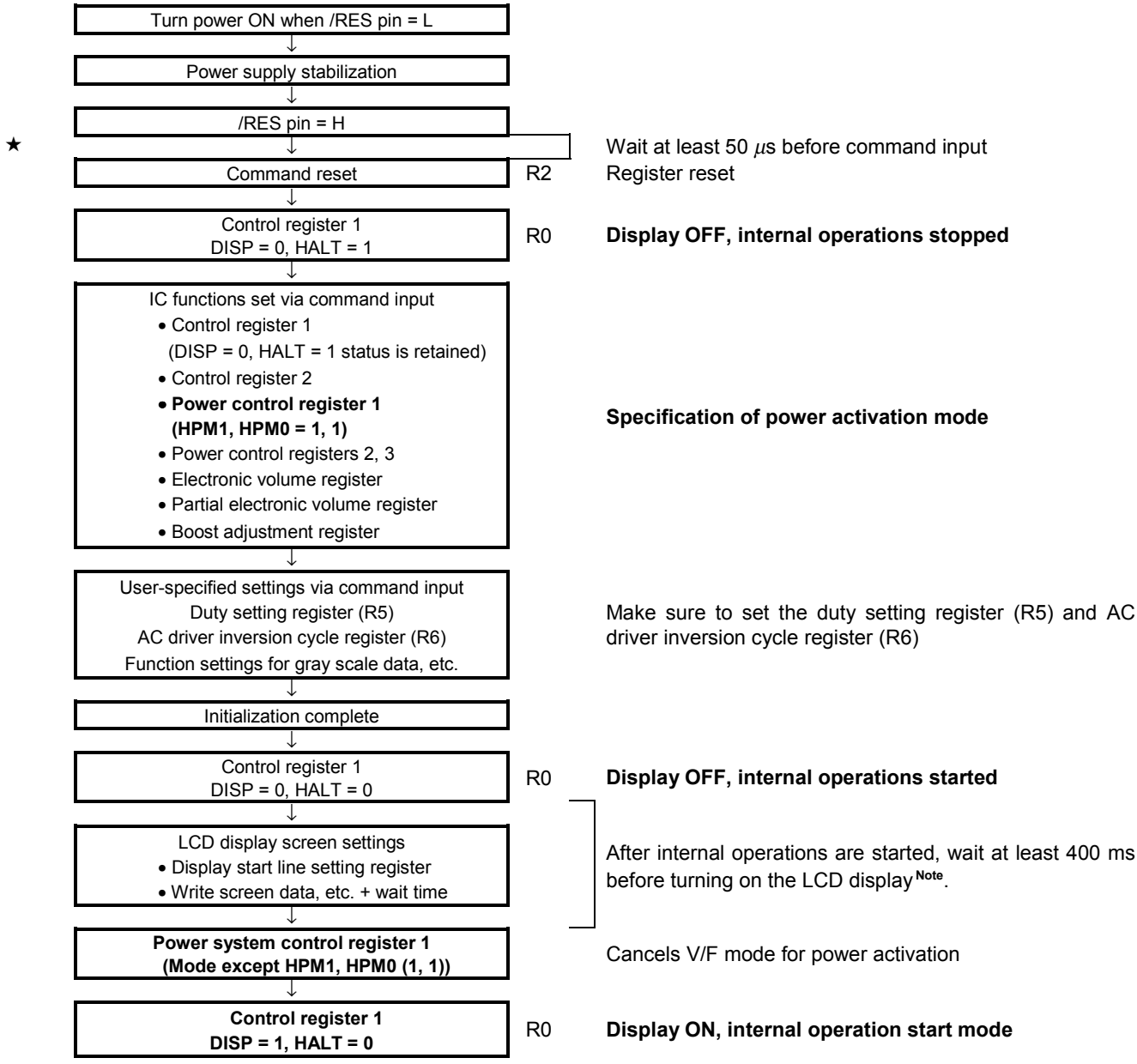
Remark : Not to use these registers.

8. POWER SUPPLY SEQUENCE

The μPD16488A includes power supply circuitry, such as a booster and a voltage follower. When a reset is performed using the /RES pin, the reset function is restricted so as to prevent operation faults that may occur due to noise effects, etc.

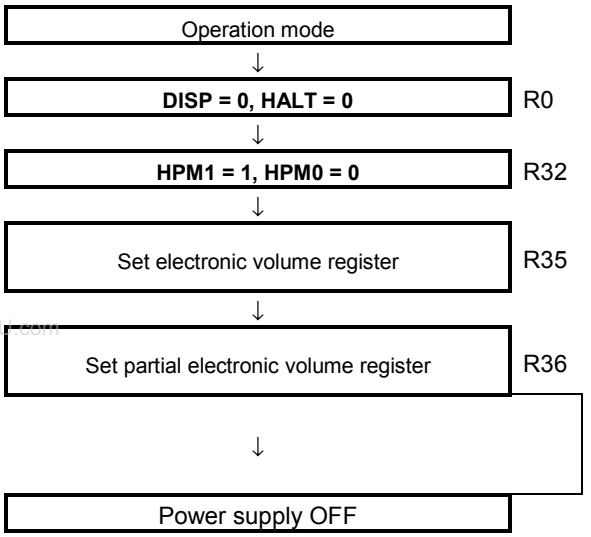
When electric charge remains in the smoothing capacitor that is connected between the V_{SS} pin and the voltage pins related to the LCD driver (V_{LCD}, V_{LC1} to V_{LC4}), troubles such as a brief all-black display screen may occur when the power is switched ON or OFF. The following power-on sequence is recommended as a means to avoid such troubles when switching the power ON or OFF.

8.1 Power ON Sequence (When Using On-Chip Power Supply, Power Supply ON → Display ON)



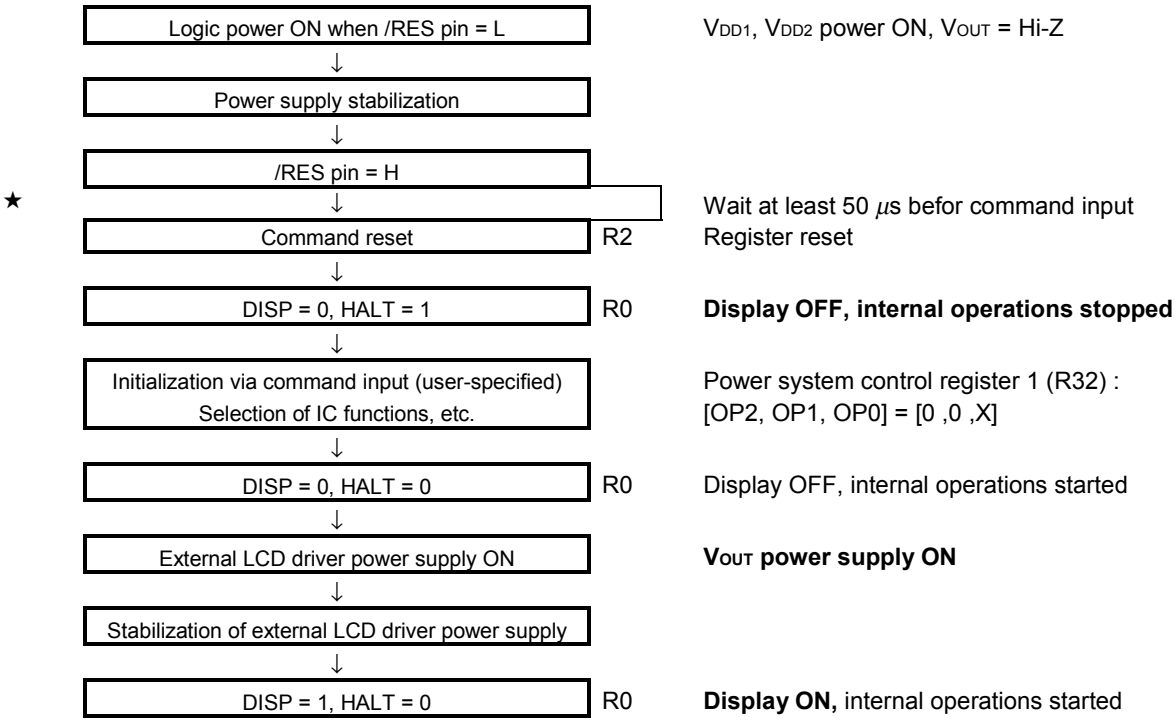
Note This 400 ms wait time varies according to the panel characteristics and the capacitance value of the boost/smoothing capacitor. We recommend determining the wait time after making a thorough evaluation of the actual device (refer to **8.5 V_{OUT}, V_{LCD} Voltage Sequence (Power ON → Power OFF)**).

8.2 Power OFF Sequence (When Using On-Chip Power Supply)



Note This 1200 ms wait time varies according to the panel characteristics and the capacitance value of the boost/smoothing capacitor. NEC recommends determining the wait time after making a thorough evaluation of the actual device (refer to **8.5 V_{OUT}, V_{LCD} Voltage Sequence (power ON → power OFF)**).

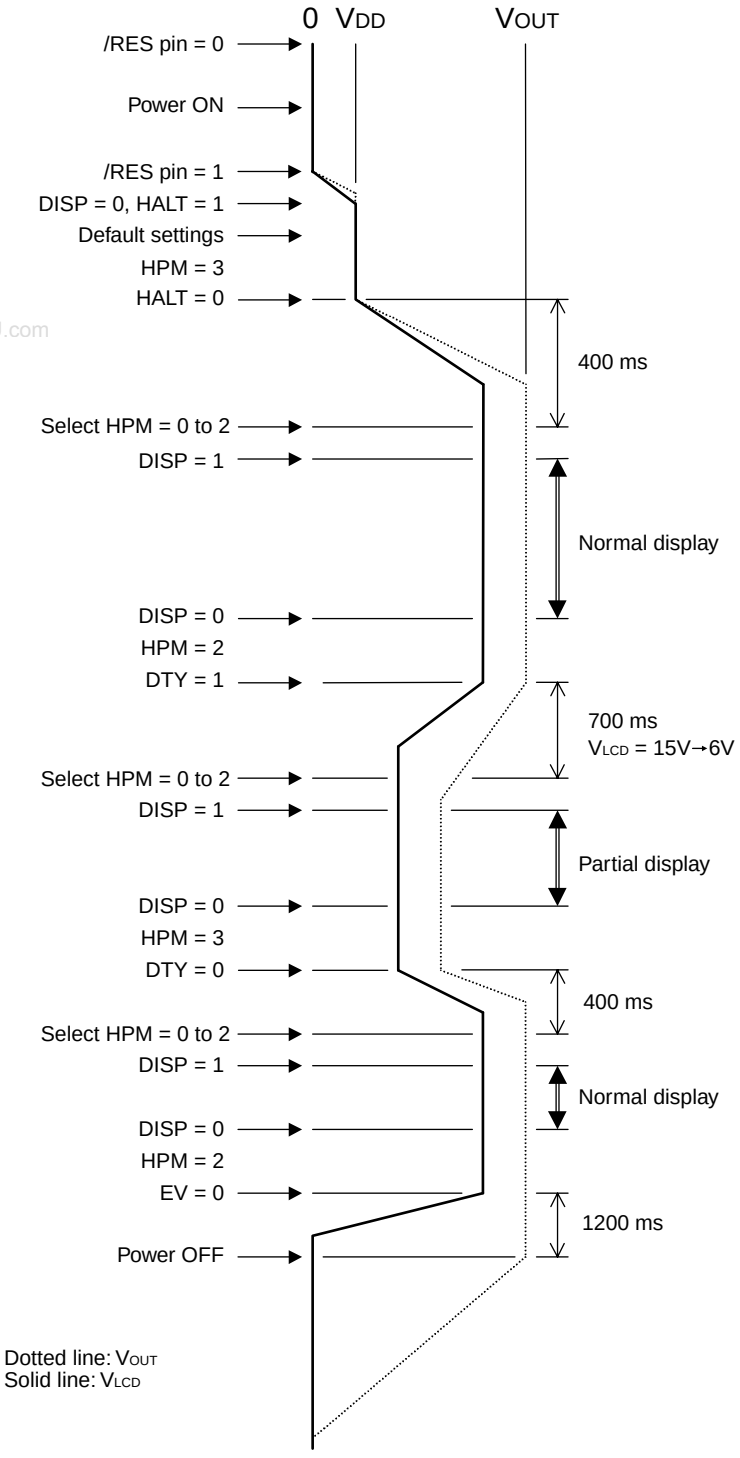
8.3 Power ON Sequence (When Using External Driver Power Supply, Power ON → Display ON)



8.4 Power Supply OFF Sequence (When Using External Driver Power Supply)

Operation mode		
↓		
DISP = 0, HALT = 0	R0	**Display OFF**, internal operation start mode
↓		
External driver power supply OFF		**V_{OUT} = Hi-Z**
↓		
DISP = 0, HALT = 1	R0	Display OFF, **internal operations stopped**
↓		
Logic power supply OFF		V_{DD1}, V_{DD2}, power supply OFF

8.5 V_{OUT}, V_{LCD} Voltage Sequence (Power ON → Power OFF)



Conditions:

V_{DD}: $V_{DD1} = V_{DD2} = 3.0$ V

Boost levels: x6 (in normal display mode), x3 (in partial display mode)

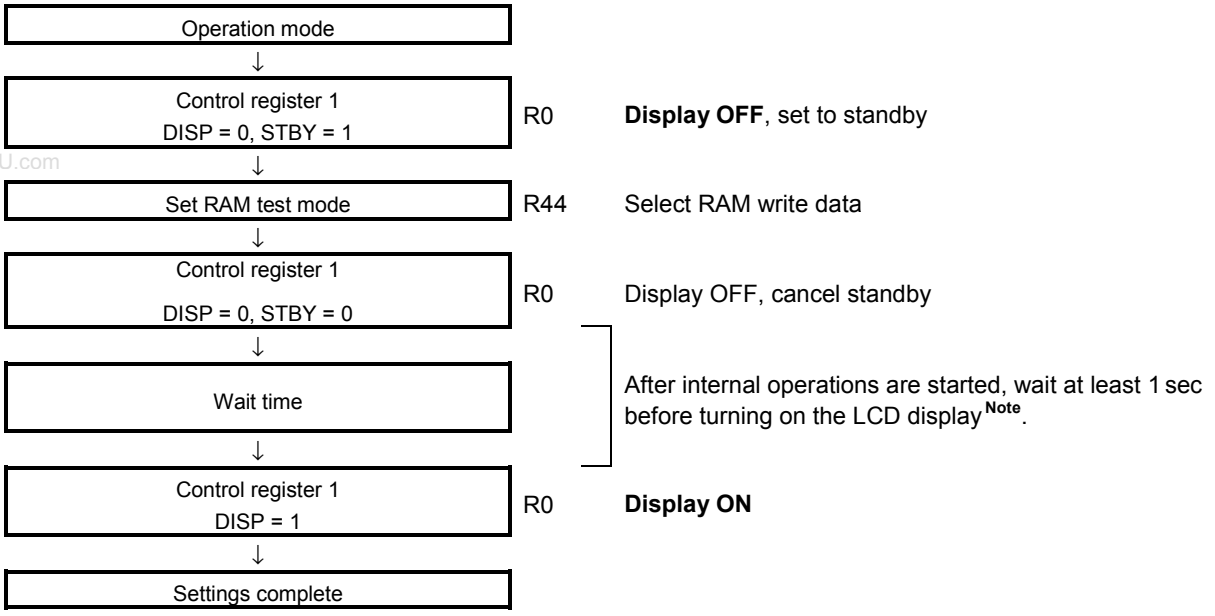
Capacitors: V_{LCn} pin to $C_n^{+}/^{-}$ pin = 1 μF,

AMP_{OUT} pin, AMP_{OUTP} pin, V_{RS} pin = 0.1 μF

Caution Connect a capacitor of less than 0.1 μF to both AMP_{OUT} and AMP_{OUTP} pins.

9. USE OF RAM TEST MODE

The μPD16488A has a test mode for writing nine types of screen data to display RAM. When using the test mode, be sure to execute via the sequence shown below. If executing the test mode by some other sequence, troubles may appear in the screen display.



Note This 1 sec wait time varies according to the panel characteristics and the capacitance value of the boost/smoothing capacitor. We recommend determining the wait time after making a thorough evaluation of the actual device.

10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = +25°C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic system supply voltage	V_{DD1}	−0.3 to +4.0	V
Booster supply voltage	V_{DD2}	−0.3 to +4.0	V
Driver supply voltage	V_{OUT}	−0.3 to +20.0	V
Driver reference supply input voltage	V_{LCD}, V_{LC1} to V_{LC4}	−0.3 to V_{OUT}+0.3	V
Logic system input voltage	V_{IN1}	−0.3 to V_{DD1}+0.3	V
Logic system output voltage	V_{OUT1}	−0.3 to V_{DD1}+0.3	V
Logic system input/output voltage	$V_{I/O1}$	−0.3 to V_{DD1}+0.3	V
Driver system input voltage	V_{IN2}	−0.3 to V_{OUT}+0.3	V
Driver system output voltage	V_{OUT2}	−0.3 to V_{OUT}+0.3	V
Operating ambient temperature	T_A	−40 to +85	°C
Storage temperature	T_{stg}	−55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic system supply voltage	V_{DD1}	1.7		3.6	V
Booster supply voltage	V_{DD2} Note1	2.4		3.6	V
Driver system supply voltage	V_{OUT} Note2	5.5		18.0	V
Logic system input voltage	V_{IN}	0		V_{DD1}	V
Driver system supply voltage	V_{LCD}, V_{LC1} to V_{LC4} Note2	0		V_{OUT}	V
Maximum setting for LCD driver voltage	V_{LCD} Note3			V_{OUT} − 0.5	V

Notes 1. V_{DD1} must be less than or equal to V_{DD2}

2. This item is the recommended parameter when the LCD has an external driver.

3. This item is the recommended parameter when an on-chip power supply circuit drives the LCD.

Cautions 1. When using an external LCD driver, be sure to maintain these relations:

$V_{SS} < V_{LC4} < V_{LC3} < V_{LC2} < V_{LC1} < V_{LCD} \leq V_{OUT}$.

2. Maintain the relations shown in 8. POWER SUPPLY SEQUENCE when turning the power ON or OFF.

3. When using an external resister (when not using an on-chip resister for V_{LCD} adjustment), maintain supply of a voltage between 1.0 V and the V_{DD1} voltage to the V_R and V_{RS} pins.

Electrical Characteristics 1

(Unless Otherwise Specified, T_A = −40 to +85°C, V_{DD1} = 1.7 to 3.6 V, V_{DD2} = 2.4 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.[Note1]	MAX.	Unit
High-level input voltage	V_{IH}		0.8 V_{DD1}			V
Low-level input voltage	V_{IL}				0.2 V_{DD1}	V
High-level input current	I_{IH1}	Except for D_7 (SI), D_6 (SCL) and D_5 to D_0			1	μA
Low-level input current	I_{IL1}	Except for D_7 (SI), D_6 (SCL) and D_5 to D_0			−1	μA
High-level output voltage	V_{OH}	I_{OUT} = −1 mA except OSC_{OUT}	V_{DD1} − 0.5			V
Low-level output voltage	V_{OL}	I_{OUT} = 1 mA except OSC_{OUT}			0.5	V
High-level leakage current	I_{LOH}	D_7 (SI), D_6 (SCL) and D_5 to D_0, $V_{IN/OUT}$ = V_{DD1}			10	μA
Low-level leakage current	I_{LOL}	D_7 (SI), D_6 (SCL) and D_5 to D_0, $V_{IN/OUT}$ = V_{SS}			−10	μA
Common output ON resistance	R_{COM}	V_{LCn} → COM_n, V_{OUT} = 15 V, V_{LCD} = 12 V, 1/10 bias, $\|I_O\|$ = 50 μA			4	kΩ
Segment output ON resistance	R_{SEG}	V_{LCn} → SEG_n, V_{OUT} = 15 V, V_{LCD} = 12 V, 1/10 bias, $\|I_O\|$ = 50 μA			4	kΩ
Driver voltage (boost voltage)	V_{OUT}	In x5 boost mode, V_{DD} = 3.0 V, Checker pattern display	13.8			V
		In x6 boost mode, V_{DD} = 3.0 V, Checker pattern display	16.6			V
★ Reference voltage	V_{REG} [Note2]	V_{DD} = 3.0 V, T_A = 85°C, TSC1,TSC0 = 1,1 (temperature characteristic curves:−0.12%/°C)	0.720	0.790	0.860	V
Oscillation frequency	f_{OSC}[Note3]	V_{DD1} = 3.0 V, T_A = 25°C, 1/92 duty, in B/W mode, R = 1100 kΩ		26.9		kHz
		V_{DD1} = 3.0 V, T_A = 25°C, 1/38 duty, in B/W mode, R = 3 MΩ		10.6		kHz

Notes 1. TYP. values are reference values when T_A = 25°C (except V_{REG}).

★ **2.** The reference voltage values when T_A = 25°C are shown below:
MIN. = 0.775 V, TYP.= 0.850 V, MAX. = 0.925 V

★ **3.** The oscillation frequency varies according to the parasitic capacitance of the wiring capacitance. We therefore recommend determining the oscillation resister's value after making a thorough evaluation of the actual device.

Electrical Characteristics 2

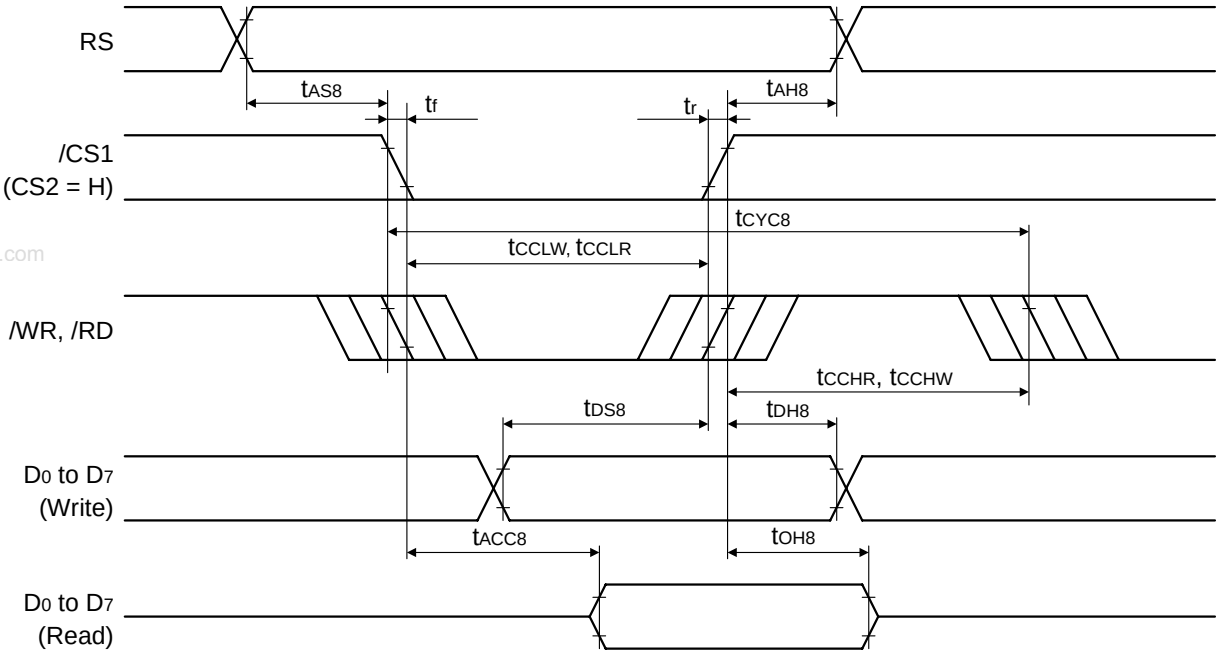
(Unless Otherwise Specified, T_A = −40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Current consumption (normal mode)	I_{DD11}	Frame frequency = 70 Hz, B/W all display OFF data output, 1/92 duty, V_{DD1} = V_{DD2} = 3.0 V, in x5 boost mode, V_{LCD} = 12 V		160	220	μA
		Frame frequency = 70 Hz, B/W checker pattern display data output, 1/92 duty, V_{DD1} = V_{DD2} = 3.0 V, in x5 boost mode, V_{LCD} = 12 V		210	310	μA
Current consumption (high-power mode)	I_{DD12}	Frame frequency = 70 Hz, B/W all display OFF data output, 1/92 duty, V_{DD1} = V_{DD2} = 3.0 V, in x5 boost mode, V_{LCD} = 12 V		270	390	μA
		Frame frequency = 70 Hz, B/W checker pattern display data output, 1/92 duty, V_{DD1} = V_{DD2} = 3.0 V, in x5 boost mode, V_{LCD} = 12 V		325	480	μA
Current consumption (low-power mode)	I_{DD13}	Frame frequency = 70 Hz, B/W all display OFF data output, 1/92 duty, V_{DD1} = V_{DD2} = 3.0 V, in x5 boost mode, V_{LCD} = 12 V		115	155	μA
		Frame frequency = 70 Hz, B/W checker pattern display data output, 1/92 duty, V_{DD1} = V_{DD2} = 3.0 V, in x5 boost mode, V_{LCD} = 12 V		165	230	μA
Current consumption (partial display mode)	I_{DD21}	Frame frequency = 70 Hz, B/W all display OFF data output, 1/38 duty, V_{DD1} = V_{DD2} = 3.0 V, in x3 boost mode, V_{LCD} = 7.0 V, normal mode		95	140	μA
		Frame frequency = 70 Hz, B/W checker pattern display data output, 1/38 duty, V_{DD1} = V_{DD2} = 3.0 V, V_{LCD} = 7.0 V, in x3 boost mode, normal mode		105	160	μA
Current consumption (standby mode)	I_{DD22}	V_{DD1} = V_{DD2} = 3.0 V			10	μA

Note TYP. values are reference values when T_A = 25°C.

Required Timing Conditions (Unless Otherwise Specified, T_A = −30 to +85°C)

(1) i80 CPU interface



When V_{DD1} = 1.7 V to 2.0 V

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		1000			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	160			ns
Control low-level pulse width (/RD)	t_{CCLR}	/RD	430			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	160			ns
Control high-level pulse width (/RD)	t_{CCHR}	/RD	160			ns
Data setup time	t_{DS8}	D_0 to D_7	160			ns
Data hold time	t_{DH8}	D_0 to D_7	0			ns
/RD access time	t_{ACC8}	D_0 to D_7, C_L = 100 pF	0		470	ns
Output disable time	t_{OH8}	D_0 to D_7, C_L = 5 pF, R = 3 kΩ	0		170	ns

Note TYP. values are reference values when T_A = 25°C.

When V_{DD1} = 2.0 to 2.5 V

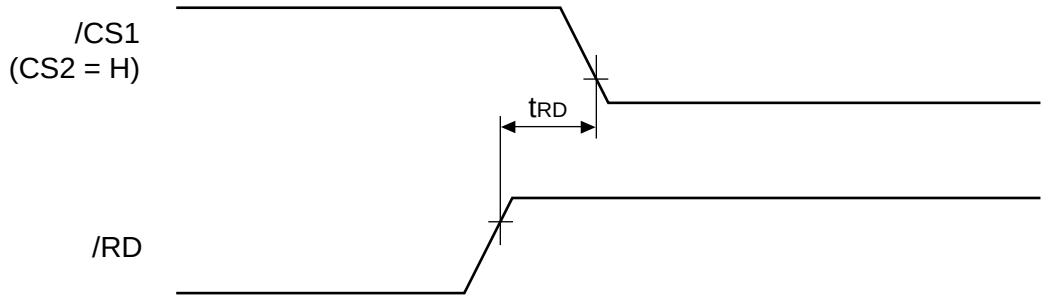
Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		600			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	120			ns
Control low-level pulse width (/RD)	t_{CCLR}	/RD	240			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	120			ns
Control high-level pulse width (/RD)	t_{CCHR}	/RD	120			ns
Data setup time	t_{DS8}	D_0 to D_7	120			ns
Data hold time	t_{DH8}	D_0 to D_7	0			ns
/RD access time	t_{ACC8}	D_0 to D_7, C_L = 100 pF	0		280	ns
Output disable time	t_{OH8}	D_0 to D_7, C_L = 5 pF, R = 3 kΩ	0		170	ns

Note TYP. values are reference values when T_A = 25°C.

When V_{DD1} = 2.5 to 3.6 V

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		250			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	60			ns
Control low-level pulse width (/RD)	t_{CCLR}	/RD	120			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	60			ns
Control high-level pulse width (/RD)	t_{CCHR}	/RD	60			ns
Data setup time	t_{DS8}	D_0 to D_7	60			ns
Data hold time	t_{DH8}	D_0 to D_7	0			ns
/RD access time	t_{ACC8}	D_0 to D_7, C_L = 100 pF	0		140	ns
Output disable time	t_{OH8}	D_0 to D_5, C_L = 5 pF, R = 3 kΩ	0		70	ns

Note TYP. values are reference values when T_A = 25°C.



(V_{DD1} = 1.8 to 3.6 V)

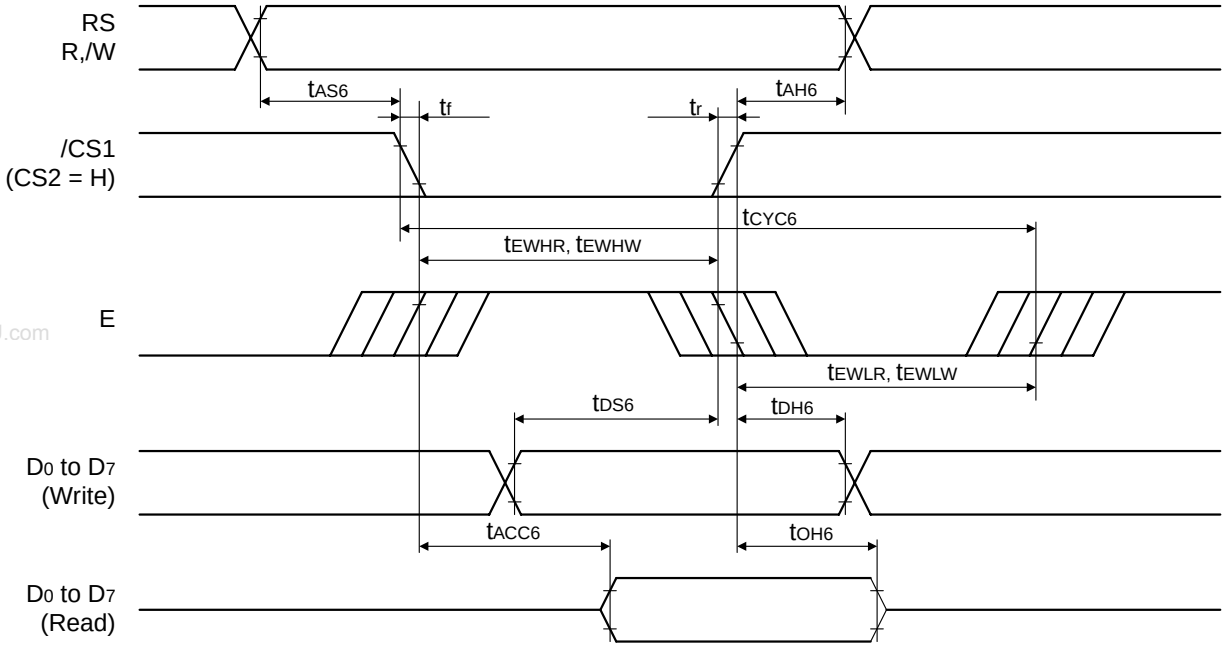
Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Chip select disable time	t_{RD}	/RD-CS	10			ns

Note TYP. values are reference values when T_A = 25°C.

Cautions 1. The rise and fall times of input signal (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20% or 80% of V_{DD1}.

(2) M68 CPU interface



When V_{DD1} = 1.7 to 2.0 V

Parameter		Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time		t_{AH6}	RS	0			ns
Address setup time		t_{AS6}	RS	0			ns
System cycle time		t_{CYC6}		1000			ns
Data setup time		t_{DS6}	D_0 to D_7	160			ns
Data hold time		t_{DH6}	D_0 to D_7	0			ns
Access time		t_{ACC6}	D_0 to D_7, C_L = 100 pF	0		470	ns
Output disable time		t_{OH6}	D_0 to D_7, C_L = 5 pF, R = 3 kΩ	0		170	ns
Enable high pulse width	Read	t_{EWHR}	E	430			ns
	Write	t_{EWHW}	E	160			ns
Enable low pulse width	Read	t_{EWLR}	E	160			ns
	Write	t_{EWLW}	E	160			ns

Note TYP. values are reference values when T_A = 25°C.

When V_{DD1} = 2.0 to 2.5 V

Parameter		Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time		t_{AH6}	RS	0			ns
Address setup time		t_{AS6}	RS	0			ns
System cycle time		t_{CYC6}		600			ns
Data setup time		t_{DS6}	D_0 to D_7	120			ns
Data hold time		t_{DH6}	D_0 to D_7	0			ns
Access time		t_{ACC6}	D_0 to D_7, C_L = 100 pF	0		280	ns
Output disable time		t_{OH6}	D_0 to D_7, C_L = 5 pF, R = 3 kΩ	0		170	ns
Enable high pulse width	Read	t_{EWHR}	E	240			ns
	Write	t_{EWHW}	E	120			ns
Enable low pulse width	Read	t_{EWLR}	E	120			ns
	Write	t_{EWLW}	E	120			ns

Note TYP. values are reference values when T_A = 25°C.

When V_{DD1} = 2.5 to 3.6 V

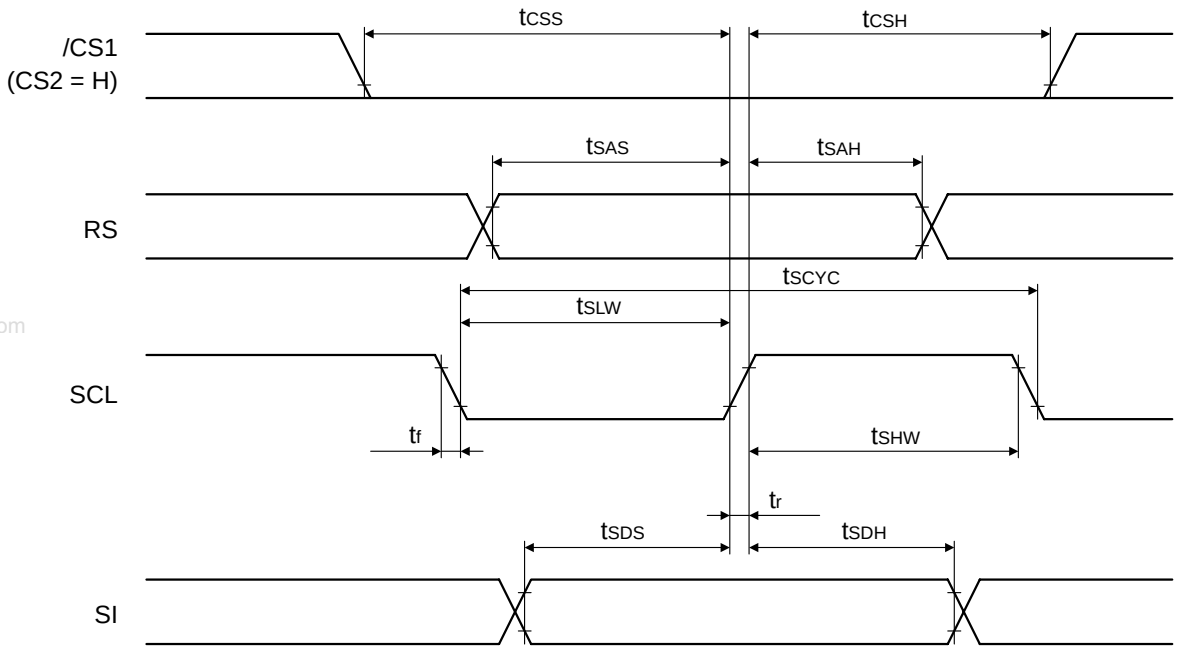
Parameter		Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time		t_{AH6}	RS	0			ns
Address setup time		t_{AS6}	RS	0			ns
System cycle time		t_{CYC6}		250			ns
Data setup time		t_{DS6}	D_0 to D_7	60			ns
Data hold time		t_{DH6}	D_0 to D_7	0			ns
Access time		t_{ACC6}	D_0 to D_7, C_L = 100 pF	0		140	ns
Output disable time		t_{OH6}	D_0 to D_7, C_L = 5 pF, R = 3 kΩ	0		70	ns
Enable high pulse width	Read	t_{EWHR}	E	120			ns
	Write	t_{EWHW}	E	60			ns
Enable low pulse width	Read	t_{EWLR}	E	60			ns
	Write	t_{EWLW}	E	60			ns

Note TYP. values are reference values when T_A = 25°C.

Cautions 1. The rise and fall times of input signals (t_r and t_f) are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either ($t_r + t_f$) ≤ ($t_{CYC6} – t_{EWLW} – t_{EWHW}$) or ($t_r + t_f$) ≤ ($t_{CYC6} – t_{EWLR} – t_{EWHR}$).

2. All timing is rated based on 20% or 80% of V_{DD1}.

(3) Serial interface



When V_{DD1} = 1.7 to 2.5 V

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Serial clock cycle	t_{SCYC}	SCL	250			ns
SCL high-level pulse width	t_{SHW}	SCL	100			ns
SCL low-level pulse width	t_{SLW}	SCL	100			ns
Address hold time	t_{SAH}	RS	150			ns
Address setup time	t_{SAS}	RS	150			ns
Data setup time	t_{SDS}	SI	100			ns
Data hold time	t_{SDH}	SI	100			ns
CS-SCL time	t_{CSS}	CS	150			ns
	t_{CSH}	CS	150			ns

Note TYP. values are reference values when T_A = 25°C.

When V_{DD1} = 2.5 to 3.6 V

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Serial clock cycle	t_{SCYC}	SCL	150			ns
SCL high-level pulse width	t_{SHW}	SCL	60			ns
SCL low-level pulse width	t_{SLW}	SCL	60			ns
Address hold time	t_{SAH}	RS	90			ns
Address setup time	t_{SAS}	RS	90			ns
Data setup time	t_{SDS}	SI	60			ns
Data hold time	t_{SDH}	SI	60			ns
CS-SCL time	t_{CSS}	CS	90			ns
	t_{CSH}	CS	90			ns

Note TYP. values are reference values when T_A = 25°C.

Cautions 1. The rise and fall times of input signal (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20% or 80% of V_{DD1}.

(4) Common

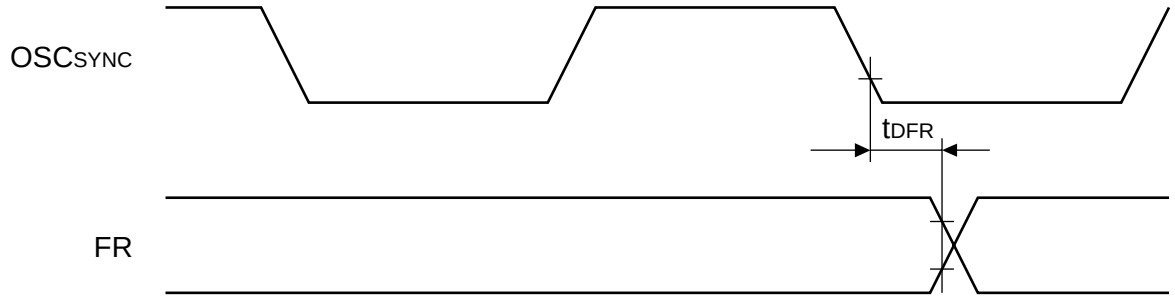
Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Clock input 1	f_N	When using OSC_{IN1}, external clock, and on-chip divider, 1/92 duty, B/W mode		26.9	150	kHz
		When using OSC_{IN1}, external clock, and on-chip divider, 1/92 duty, four-level gray scale mode		53.8	150	kHz
Clock input 2	f_P	When using OSC_{IN2}, external clock for partial display mode, but not using on-chip divider, B/W mode		10.6	50	kHz
		When using OSC_{IN2}, external clock for partial display mode, but not using on-chip divider, four-level gray scale mode		21.3	50	kHz

Note TYP. values are reference values when frame frequency = 70 Hz.

Cautions 1. The rise and fall times of input signal (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20% or 80% of V_{DD1}.

(a) Display control output timing



(V_{DD1} = 1.7 to 2.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
FR delay time	t_{DFR}	FR, C_L = 50 pF		50	200	ns

Note TYP. values are reference values when T_A = 25°C.

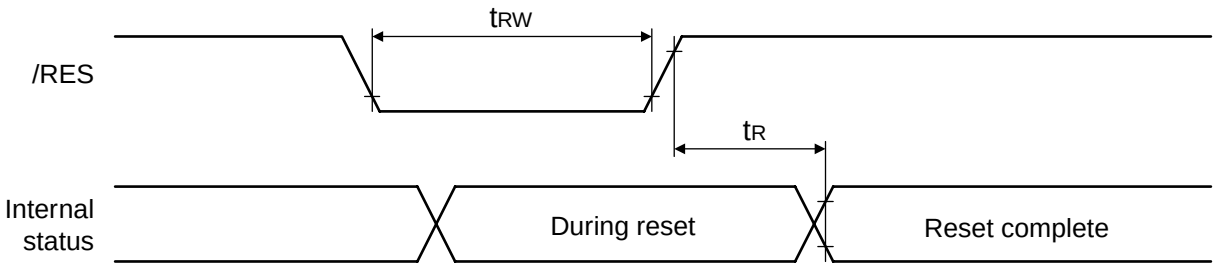
(V_{DD1} = 2.5 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
FR delay time	t_{DFR}	FR, C_L = 50 pF		20	80	ns

Note TYP. values are reference values when T_A = 25°C.

Caution All timing is rated based on 20% or 80% of V_{DD1}.

(b) Reset timing



When V_{DD1} = 1.7 to 2.5 V

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Reset time	t_R				50	μs
Reset low pulse width	t_{RW}	/RES	50			μs

Note TYP. values are reference values when T_A = 25°C.

When V_{DD1} = 2.5 to 3.6 V

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Reset time	t_R				50	μs
Reset low pulse width	t_{RW}	/RES	50			μs

Note TYP. values are reference values when T_A = 25°C.

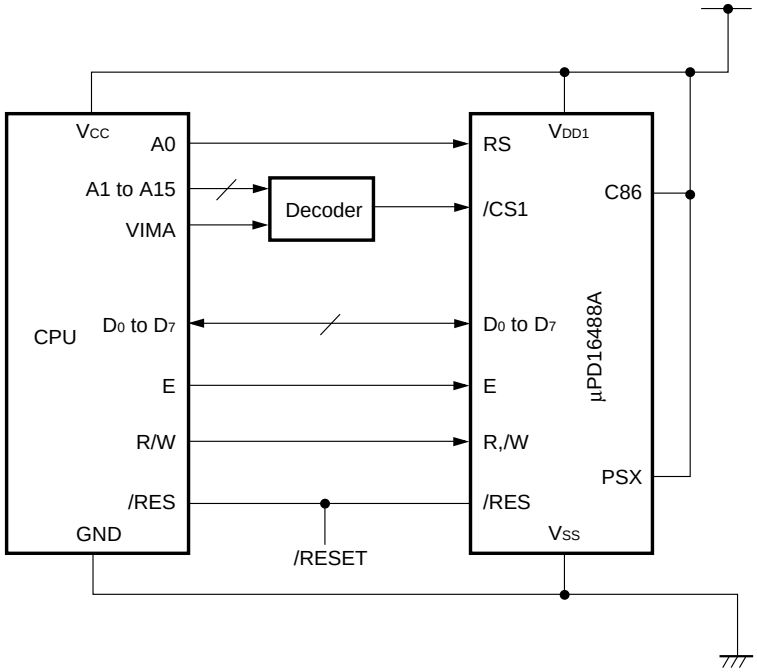
Caution All timing is rated based on 20% or 80% of V_{DD1}.

11. CPU INTERFACE (REFERENCE EXAMPLE)

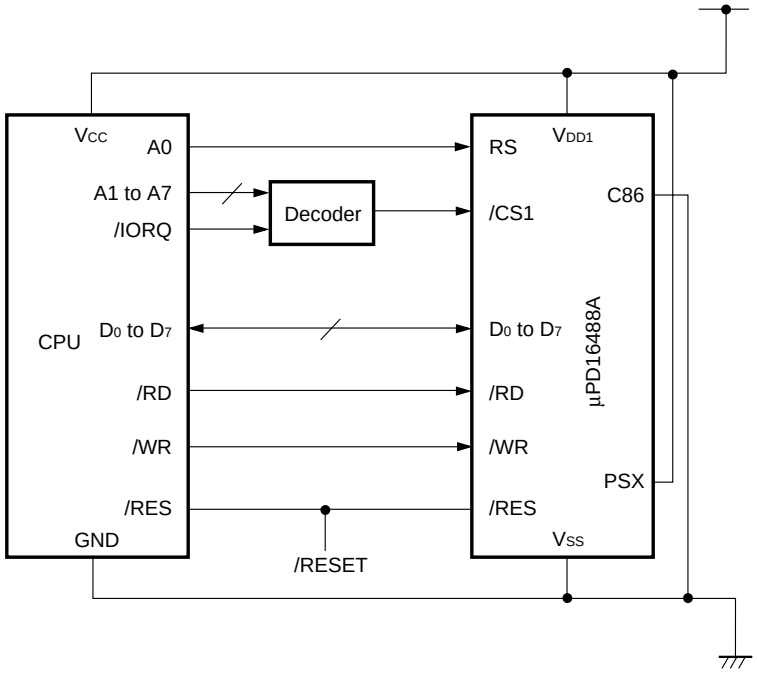
The μPD16488A can be connected to either an i80 series CPU or an M68 series CPU. Also, if a serial interface connection is used, the number of signal lines can be reduced.

If several μPD16488A chip is used, the display area can be enlarged. When using this method, use the chip select signal to select and access the ICs.

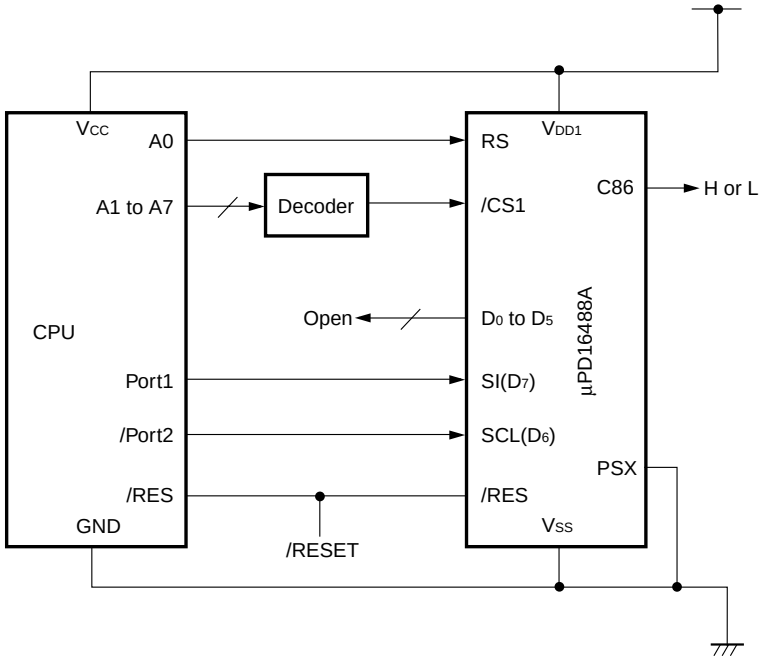
(1) M68 series CPU



(2) i80 series CPU



(3) When using serial interface



[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.