NEC

MOS INTEGRATED CIRCUIT

μPD16647

402/384-OUTPUT TFT-LCD SOURCE DRIVER (64 GRAY SCALE)

DESCRIPTION

The μPD16647 is a source driver for TFT-LCD 64 gray scale displays. Its logic circuit operates at 3.3 V and the driver circuit operates at 5.0 V. The input data is digital data at 6 bits x 3 dots, and 260,000 colors can be displayed in 64-value outputs γ-corrected by the internal D/A converter and 10 external power supplies. The clock frequency is 50 MHz MIN. μPD16647 can be used in TFT-LCD panels conforming to the SVGA standards.

FEATURES

- CMOS level input
- 402/384 outputs
- 6 bits (gray scale data) x 3 dots input
- 64-value output by 10 external power supplies and internal D/A converter
- Output dynamic range : V_{SS2} + 0.1 V to V_{DD2} – 0.1 V
- High-speed data transfer: f_{MAX} =50 MHz MIN.(internal data transfer rate at supply voltage V_{DD1} of logic circuit =3.0 V)
- Level of γ-corrected power supply can be inverted
- Input data inversion function (INV)
- Precharge-less output buffer
- Logic supply voltage (V_{DD1}) : 3.3 V ± 0.3 V
- Driver supply voltage (V_{DD2}) : 5.0 V ± 0.5 V
- Slim TCP

ORDERING INFORMATION

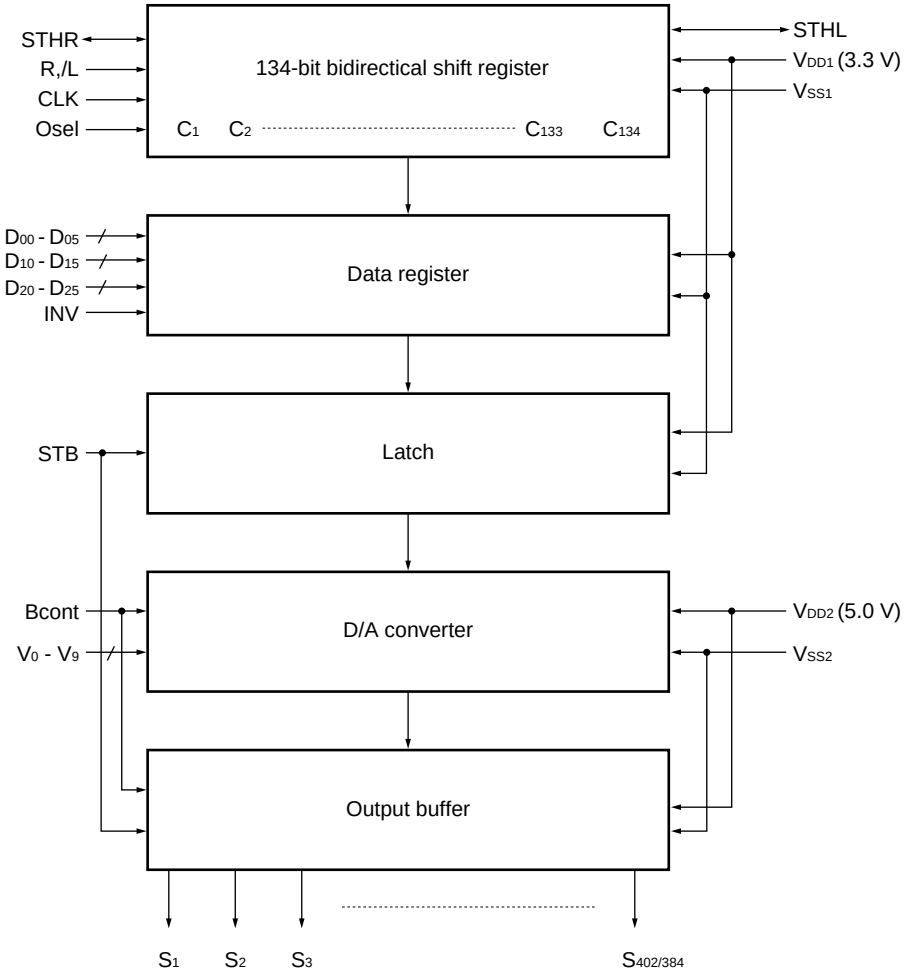
Part Number	Package
μPD16647N-xxx	TCP (TAB package)

Remark The TCP package is a custom-ordered item. Users are requested to consult with an NEC sales representative.

Document No. S13607EJ2V0DS00 (2nd edition)
Date Published August 1999 NS CP (K)
Printed in Japan

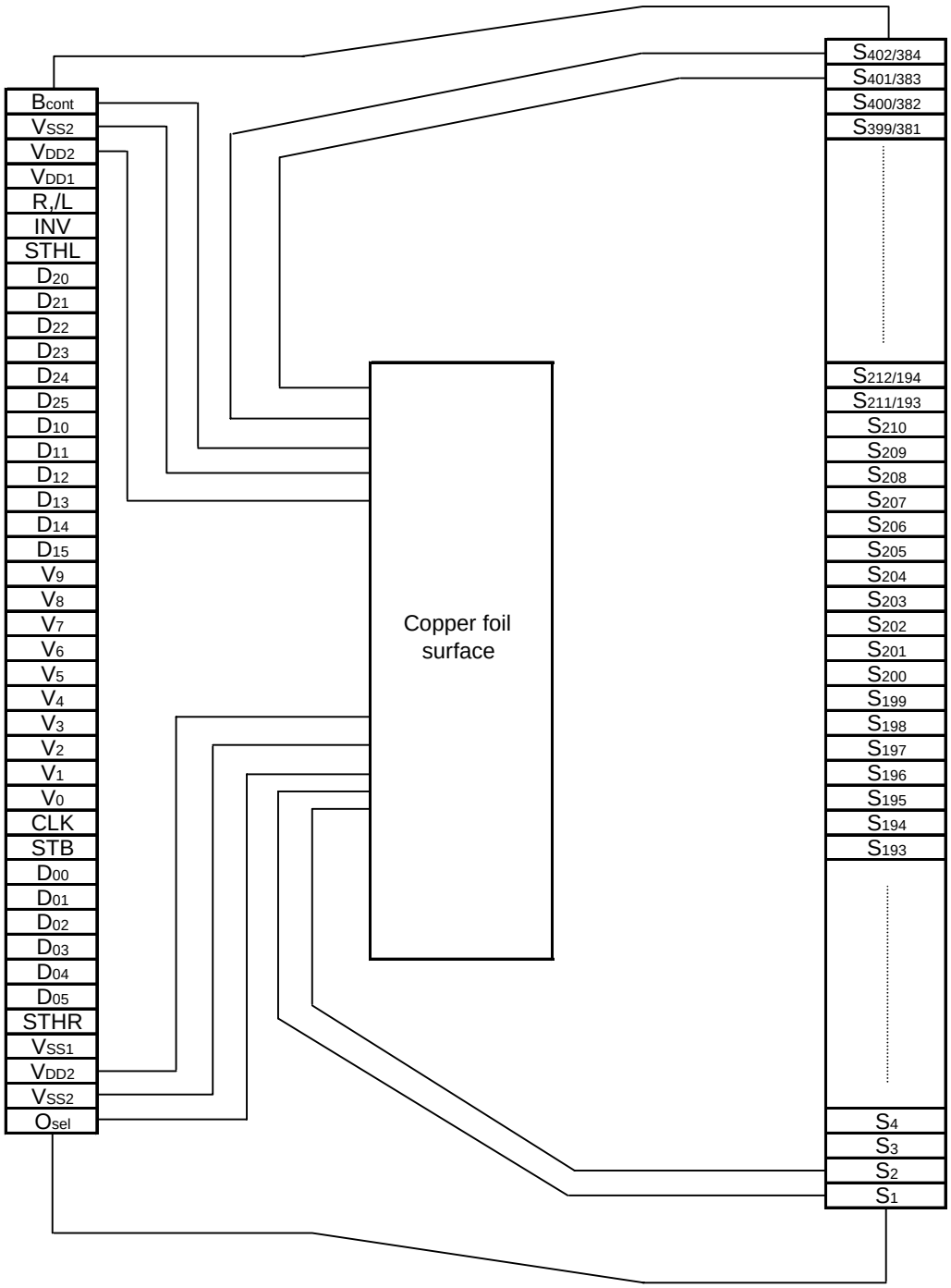
The mark ★ shows major revised points.

1. BLOCK DIAGRAM



Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (μPD16647N-xxx)



Remark This figure does not specify the TCP package.

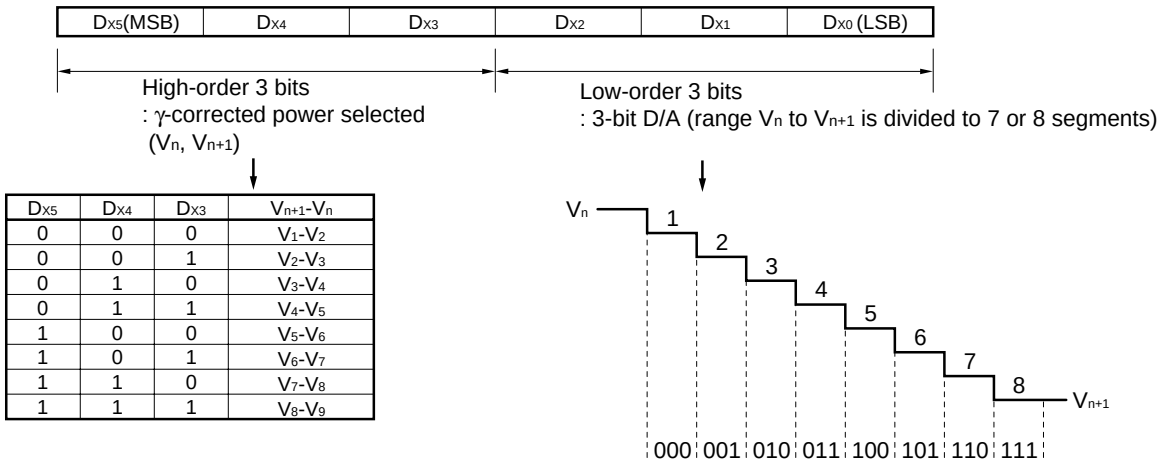
3. PIN DESCRIPTION

Pin Symbol	Pin Name	Description
S_1 to $S_{402/384}$	Driver output	Output 64 gray-scale analog voltages converted from digital signals. Osel = H or open: 402 outputs (S_1 to $S_{402/384}$) Osel = L : 384 outputs (S_1 to S_{192}, $S_{211/193}$ to $S_{402/384}$) S_{193} to S_{210} outputs are invalid in 384 outputs.
D_{00} to D_{05}	Display data input	Inputs 18-bit-wide display gray scale data (6 bits) x 3 dots (RGB). D_{X0} : LSB, D_{X5} : MSB
D_{10} to D_{15}		
D_{20} to D_{25}		
R,/L	Shift direction select input	This pin inputs/outputs start pulses in cascade mode. Shift direction of shift register is as follows: R,/L = H : STHR input, $S_1 \rightarrow S_{402}$, STHL output R,/L = L : STHL input, $S_{402} \rightarrow S_1$, STHR output
STHR	Right shift start pulse I/O	R,/L = H : Inputs start pulse R,/L = L : Outputs start pulse
STHL	Left shift start pulse I/O	R/L = H : Outputs start pulse R/L = L : Inputs start pulse
Bcont	Bias control	This pin can be used to finely control the bias current inside the output amplifier. In cases when fine-control is necessary, connect this pin to V_{DD2} using a resistor of 10 to 100kΩ (per IC). When this fine-control function is not required, short-circuit this pin to V_{DD2}. Refer to **7. Bias Current Control Function/Bcont**.
CLK	Shift clock input	Inputs shift clock to shift register. Display data is loaded to data register at rising edge of this pin. Start pulse output goes high at rising edge of 134th clock after start pulse has been input, and serves as start pulse to driver in next stage. 134th clock of driver in first stage serves as start pulse of driver in next stage.
STB	Latch input	Contents of data register are latched at rising edge, transferred to D/A converter, and output as analog voltage corresponding to display data. Contents of internal shift register are cleared after STB has been input. One pulse of this signal is input when μPD16647 is started, and then device operates normally. For STB input timing, refer to **9. Switching Characteristics Waveform.**
Osel	Selection of number of outputs	Selects number of outputs. This pin is internally pulled up to V_{DD1}. Osel = H or open : 402 outputs (S_1 to $S_{402/384}$) Osel = L : 384 outputs (S_1 to S_{192}, $S_{211/193}$ to $S_{402/384}$)
V_0 to V_9	γ-corrected power supply	Inputs γ-corrected power from external source. $V_{SS2} \le V_9 \le V_8 \le V_7 \le V_6 \le V_5 \le V_4 \le V_3 \le V_2 \le V_1 \le V_0 \le V_{DD2}$ or $V_{SS2} \le V_0 \le V_1 \le V_2 \le V_3 \le V_4 \le V_5 \le V_6 \le V_7 \le V_8 \le V_9 \le V_{DD2}$ Maintain gray scale power supply during gray scale voltage output.
INV	Data inversion input	Input data can be inverted when display data is loaded. INV = H : Inverts and loads input data. INV = L : Does not invert input data.
V_{DD1}	Logic circuit power supply	3.3 V ± 0.3 V
V_{DD2}	Driver circuit power supply	5.0 V ± 0.5 V
V_{SS1}	Logic ground	Ground
V_{SS2}	Driver ground	Ground

Caution Be sure to turn on power in the order V_{DD1}, logic input, V_{DD2}, and gray scale power (V_0 to V_9), and turn off power in the reverse order, to prevent the μPD16647 from being damaged by latchup. Be sure to observe this power sequence even during a transition period.

4. RELATION BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The 10 major points on the γ-characteristic curve of the LCD panel are arbitrarily set by external power supplies V_0 through V_9. If the display data is 00H or 3FH, gray scale voltage V_0 or V_9 is output. If the display data is in the range 01H to 3EH, the high-order 3 bits select an external power pair V_{n+1}, V_n. The low-order 3 bits evenly divide the range of V_{n+1} to V_n into eight segments by means of D/A conversion (however, the ranges from V_8 to V_7 and from V_1 to V_0 are divided into seven segments) to output a 64 gray scale voltage.



D_{X5}	D_{X4}	D_{X3}	V_{n+1}-V_n
0	0	0	V_1-V_2
0	0	1	V_2-V_3
0	1	0	V_3-V_4
0	1	1	V_4-V_5
1	0	0	V_5-V_6
1	0	1	V_6-V_7
1	1	0	V_7-V_8
1	1	1	V_8-V_9

Figure4-1. Relationship between Input Data and γ-corrected Voltage

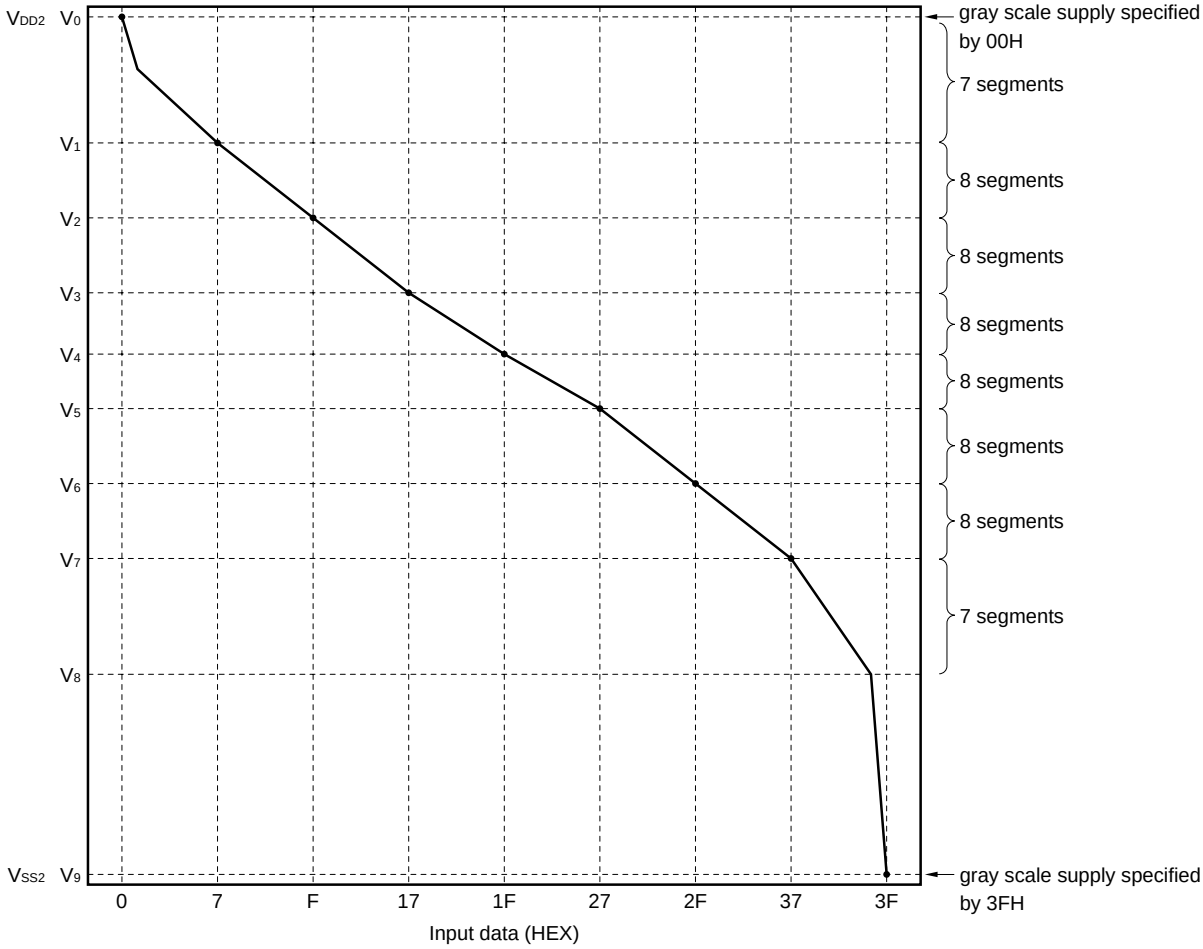


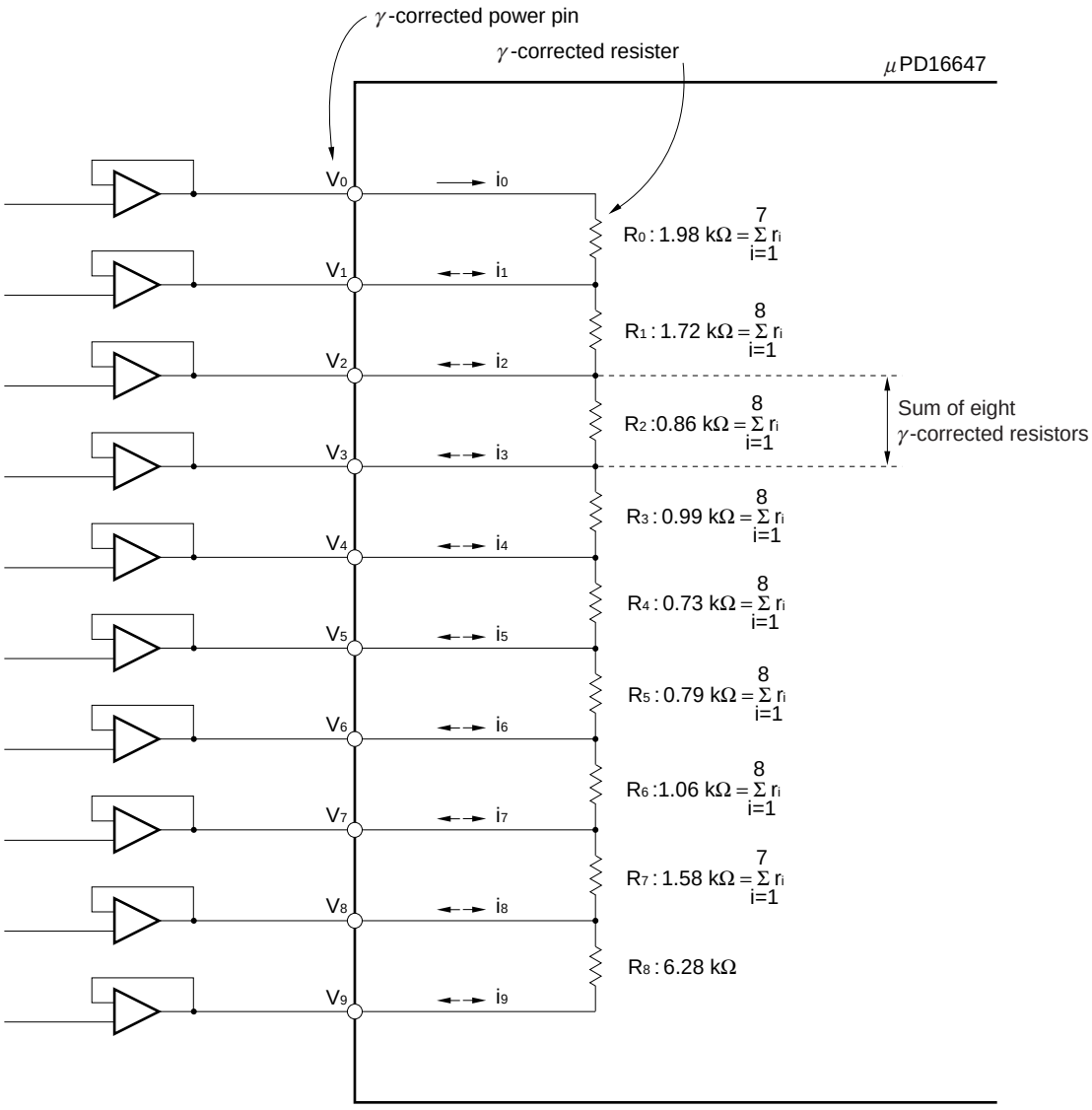
Table 4–1. Relationship between Input Data and Output Voltage

Input Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage
00H	0	0	0	0	0	0	V_0
01H	0	0	0	0	0	1	$V_1 + (V_0 – V_1) \times 6/7$
02H	0	0	0	0	1	0	$V_1 + (V_0 – V_1) \times 5/7$
03H	0	0	0	0	1	1	$V_1 + (V_0 – V_1) \times 4/7$
04H	0	0	0	1	0	0	$V_1 + (V_0 – V_1) \times 3/7$
05H	0	0	0	1	0	1	$V_1 + (V_0 – V_1) \times 2/7$
06H	0	0	0	1	1	0	$V_1 + (V_0 – V_1) \times 1/7$
07H	0	0	0	1	1	1	V_1
08H	0	0	1	0	0	0	$V_2 + (V_1 – V_2) \times 7/8$
09H	0	0	1	0	0	1	$V_2 + (V_1 – V_2) \times 6/8$
0AH	0	0	1	0	1	0	$V_2 + (V_1 – V_2) \times 5/8$
0BH	0	0	1	0	1	1	$V_2 + (V_1 – V_2) \times 4/8$
0CH	0	0	1	1	0	0	$V_2 + (V_1 – V_2) \times 3/8$
0DH	0	0	1	1	0	1	$V_2 + (V_1 – V_2) \times 2/8$
0EH	0	0	1	1	1	0	$V_2 + (V_1 – V_2) \times 1/8$
0FH	0	0	1	1	1	1	V_2
10H	0	1	0	0	0	0	$V_3 + (V_2 – V_3) \times 7/8$
11H	0	1	0	0	0	1	$V_3 + (V_2 – V_3) \times 6/8$
12H	0	1	0	0	1	0	$V_3 + (V_2 – V_3) \times 5/8$
13H	0	1	0	0	1	1	$V_3 + (V_2 – V_3) \times 4/8$
14H	0	1	0	1	0	0	$V_3 + (V_2 – V_3) \times 3/8$
15H	0	1	0	1	0	1	$V_3 + (V_2 – V_3) \times 2/8$
16H	0	1	0	1	1	0	$V_3 + (V_2 – V_3) \times 1/8$
17H	0	1	0	1	1	1	V_3
18H	0	1	1	0	0	0	$V_4 + (V_3 – V_4) \times 7/8$
19H	0	1	1	0	0	1	$V_4 + (V_3 – V_4) \times 6/8$
1AH	0	1	1	0	1	0	$V_4 + (V_3 – V_4) \times 5/8$
1BH	0	1	1	0	1	1	$V_4 + (V_3 – V_4) \times 4/8$
1CH	0	1	1	1	0	0	$V_4 + (V_3 – V_4) \times 3/8$
1DH	0	1	1	1	0	1	$V_4 + (V_3 – V_4) \times 2/8$
1EH	0	1	1	1	1	0	$V_4 + (V_3 – V_4) \times 1/8$
1FH	0	1	1	1	1	1	V_4
20H	1	0	0	0	0	0	$V_5 + (V_4 – V_5) \times 7/8$
21H	1	0	0	0	0	1	$V_5 + (V_4 – V_5) \times 6/8$
22H	1	0	0	0	1	0	$V_5 + (V_4 – V_5) \times 5/8$
23H	1	0	0	0	1	1	$V_5 + (V_4 – V_5) \times 4/8$
24H	1	0	0	1	0	0	$V_5 + (V_4 – V_5) \times 3/8$
25H	1	0	0	1	0	1	$V_5 + (V_4 – V_5) \times 2/8$
26H	1	0	0	1	1	0	$V_5 + (V_4 – V_5) \times 1/8$
27H	1	0	0	1	1	1	V_5
28H	1	0	1	0	0	0	$V_6 + (V_5 – V_6) \times 7/8$
29H	1	0	1	0	0	1	$V_6 + (V_5 – V_6) \times 6/8$
2AH	1	0	1	0	1	0	$V_6 + (V_5 – V_6) \times 5/8$
2BH	1	0	1	0	1	1	$V_6 + (V_5 – V_6) \times 4/8$
2CH	1	0	1	1	0	0	$V_6 + (V_5 – V_6) \times 3/8$
2DH	1	0	1	1	0	1	$V_6 + (V_5 – V_6) \times 2/8$
2EH	1	0	1	1	1	0	$V_6 + (V_5 – V_6) \times 1/8$
2FH	1	0	1	1	1	1	V_6
30H	1	1	0	0	0	0	$V_7 + (V_6 – V_7) \times 7/8$
31H	1	1	0	0	0	1	$V_7 + (V_6 – V_7) \times 6/8$
32H	1	1	0	0	1	0	$V_7 + (V_6 – V_7) \times 5/8$
33H	1	1	0	0	1	1	$V_7 + (V_6 – V_7) \times 4/8$
34H	1	1	0	1	0	0	$V_7 + (V_6 – V_7) \times 3/8$
35H	1	1	0	1	0	1	$V_7 + (V_6 – V_7) \times 2/8$
36H	1	1	0	1	1	0	$V_7 + (V_6 – V_7) \times 1/8$
37H	1	1	0	1	1	1	V_7
38H	1	1	1	0	0	0	$V_8 + (V_7 – V_8) \times 6/7$
39H	1	1	1	0	0	1	$V_8 + (V_7 – V_8) \times 5/7$
3AH	1	1	1	0	1	0	$V_8 + (V_7 – V_8) \times 4/7$
3BH	1	1	1	0	1	1	$V_8 + (V_7 – V_8) \times 3/7$
3CH	1	1	1	1	0	0	$V_8 + (V_7 – V_8) \times 2/7$
3DH	1	1	1	1	0	1	$V_8 + (V_7 – V_8) \times 1/7$
3EH	1	1	1	1	1	0	V_8
3FH	1	1	1	1	1	1	V_9

4.1 γ-Corrected Power Circuit

The reference power supply of the D/A converter consists of a ladder circuit with a total of 64 resistors, and resistance Σri between γ-corrected power pins differs depending on each pair of γ-corrected power pins. One pair of γ-corrected power pins consists of seven or eight series resistors, and resistance Σri in the figure below is indicated as the sum of the seven or eight resistors. The resistance ratio between the γ-corrected power pins (Σri ratio) is designed to be a value relatively close to the ratio of the γ-corrected voltages V_1 through V_8 (gray scale voltages in 7 steps) used in an actual LCD panel. Under ideal conditions where there is no difference between the two, therefore, there is no voltage difference between the voltage of the γ-corrected power supplies and the gray scale voltages in 7 steps of the resistor ladder circuits of the μPD16647, and no current flows into the γ-corrected power pins V_1 through V_8. As a result, a voltage follower circuit is not necessary.

Figure4–2. γ-Corrected Power Circuit



5. RELATION BETWEEN INPUT DATA AND OUTPUT VOLTAGE

Data format : 6 bits x RGB (3 dots)
Input width : 18 bits (1 pixel data)

(1) R,/L = H (right shift)

Output	S_1	S_2	S_3	S_4	…	$S_{401/383}$	$S_{402/384}$
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{00} to D_{05}	…	D_{10} to D_{15}	D_{20} to D_{25}

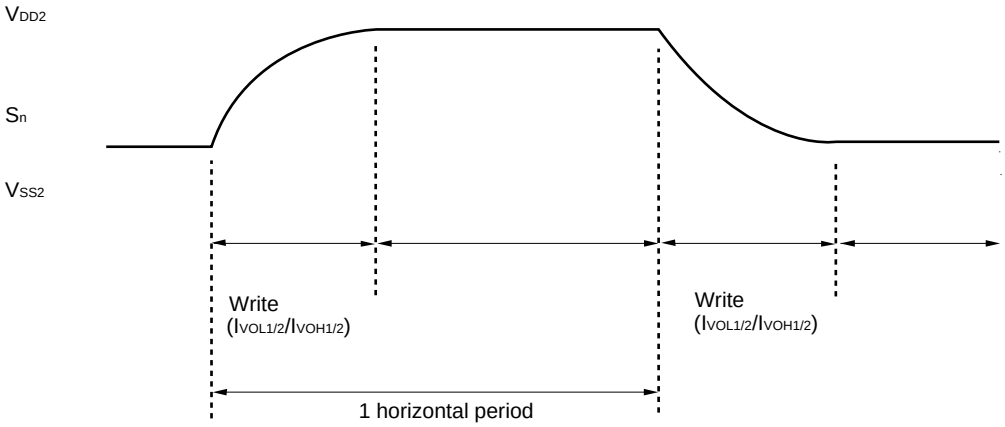
(2) R,/L = L (left shift)

Output	S_1	S_2	S_3	S_4	…	$S_{401/383}$	$S_{402/384}$
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{00} to D_{05}	…	D_{10} to D_{15}	D_{20} to D_{25}

6. OPERATION OF OUTPUT BUFFER

The output buffer consists of an operational amplifier circuit that does not perform precharge operation. Therefore, driver output current $I_{VOH1/2}$ is the charging current to the LCD, and $I_{VOL1/2}$ is the discharging current.

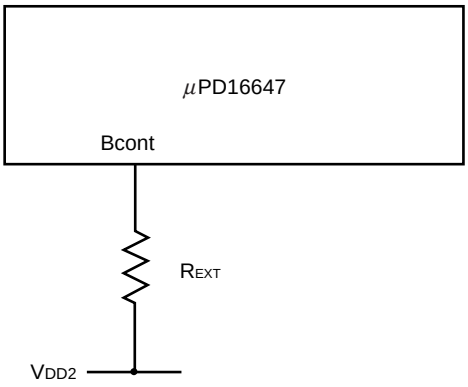
Figure6–1. LCD panel driving waveform of μPD16647



7. BIAS CURRENT CONTROL FUNCTION/Bcont

It is possible to fine-control the current consumption by using the bias current control function (Bcont pin). When using this function, connect this pin to the stabilized V_{DD2} potential using an external resistor (R_{EXT}). When not using this function, however, short-circuit this pin to V_{DD2}.

Figure7–1. Bias Current Control Function/Bcont



Refer to the table below for the percentage of current regulation when using the bias current control function.

Table7–1. Current Consumption Regulation Percentage Compared to Normal Mode

R_{EXT}	Current Consumption Regulation Percentage
SHORT	100 %
10 kΩ	95 %
20 kΩ	91 %
40 kΩ	85 %
80 kΩ	79 %

Remark Be aware that the above current consumption regulation percentages are not product-characteristic guaranteed as they are based on the results of simulation.

Caution Because the low-power and bias-current control functions control the bias current in the output amplifier and regulate the over-all current consumption of the driver IC, when this occurs, the characteristics of the output amplifier will simultaneously change. Therefore, when using these functions, be sure to sufficiently evaluate the picture quality.

8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic Supply Voltage	V_{DD1}	–0.3 to +4.5	V
Driver Supply Voltage	V_{DD2}	–0.3 to +6.0	V
Input Voltage	V_I	–0.3 to $V_{DD1,2}$ + 0.3	V
Output Voltage	V_O	–0.3 to $V_{DD1,2}$ + 0.3	V
Operating Ambient Temperature	T_A	–10 to +75	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range (T_A = –10 to +75 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Supply Voltage	V_{DD1}	3.0	3.3	3.6	V
Driver Supply Voltage	V_{DD2}	4.5	5.0	5.5	V
High-level Input Voltage	V_{IH}	0.7 V_{DD1}		V_{DD1}	V
Low-level Input Voltage	V_{IL}	0		0.3 V_{DD1}	V
γ -corrected Supply Voltage	V_0 to V_9	V_{SS2} + 0.1		V_{DD2} – 0.1	V
Maximum Clock Frequency	$f_{MAX.}$	50			MHz

Electrical Characteristics (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ± 0.3 V, V_{DD2} = 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input Leakage Current	I_{IL}	D_{00}-D_{05},D_{10}-D_{15},D_{20}-D_{25} R,/L,STB				±1.0	μA
Pull-up Resistor	R_{PU}	V_{DD1} = 3.3 V		40	100	250	kΩ
High-level Output Voltage	V_{OH}	STHR(STHL),I_O = –1.0 mA		V_{DD1} – 0.5			V
Low-level Output Voltage	V_{OL}	STHR(STHL),I_O = +1.0 mA				0.5	V
Static Current Consumption of γ-corrected Power	I_{vn1}	V_{DD1} = 3.3 V, V_n – V_{n+1} = 0.5 V, V_{DD2} = 5.0 V	V_0-V_1	126	253	506	μA
			V_1-V_2	145	291	582	μA
			V_2-V_3	289	579	1158	μA
			V_3-V_4	252	504	1008	μA
			V_4-V_5	343	686	1372	μA
			V_5-V_6	315	631	1262	μA
			V_6-V_7	237	474	948	μA
			V_7-V_8	158	316	632	μA
			V_8-V_9	40	80	160	μA
Driver Output Current	I_{VOH2}	V_{OUT} = 4.4 V, V_X = 4.9 V **Note1** V_{DD1} = 3.3 V, V_{DD2} = 5.0 V		(–0.12)		–0.03	mA
	I_{VOL2}	V_{OUT} = 0.6 V, V_X = 0.1 V **Note1** V_{DD1} = 3.3 V, V_{DD2} = 5.0 V		0.04		(0.16)	mA
Output Voltage Deviation	ΔV_O	V_{DD1} = 3.3 V, V_{DD2}=5.0 V, V_{OUT}=2.5 V **Note1**			±10	±20	mV
Output Swing Difference Deviation	ΔV_{P-P}	Input data			(±5)		mV
Output Voltage Range	V_O	Input data : 00H to 3FH		V_{SS2} + 0.1		V_{DD2} – 0.1	V
Dynamic Logic Current Consumption	I_{DD1}	No load, V_{DD2} = 3.3 V **Note2**			0.5	2.5	mA
Dynamic Driver Current Consumption	I_{DD2}	No load, V_{DD2} = 5.0 V **Note2**			5.0	10.0	mA

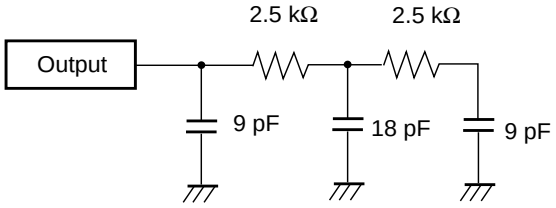
Notes 1. V_X refers to the output voltage of analog output pins S_1 to $S_{402/384}$.
V_{OUT} refers to the voltage applied to analog output pins S_1 to $S_{402/384}$.

2. The STB cycle is specified at 31 μs and f_{CLK}= 16 MHz.

Switching Characteristics (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ± 0.3 V, V_{DD2} = 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	C_L = 15 pF			7	12	ns
	t_{PHL1}				7	12	ns
Driver Output Delay Time	t_{PLH2}	V_{DD2} = 5.0 V	V_O: 0.1 V → 4.9 V		2.2	10	μs
	t_{PLH3}	5 kΩ +36 pF			2.9	12	μs
	t_{PHL2}		V_O: 4.9 V → 0.1 V		2.6	10	μs
	t_{PHL3}				3.6	12	μs
Input Capacitance	C_{I1}	STHR (STHL), T_A = 25 °C			10	20	pF
	C_{I2}	V_0 to V_9, T_A = 25 °C			100	150	pF
	C_{I3}	STHR (STHL), other than V_0 to V_9 , T_A = 25 °C			10	15	pF

<Output Load>

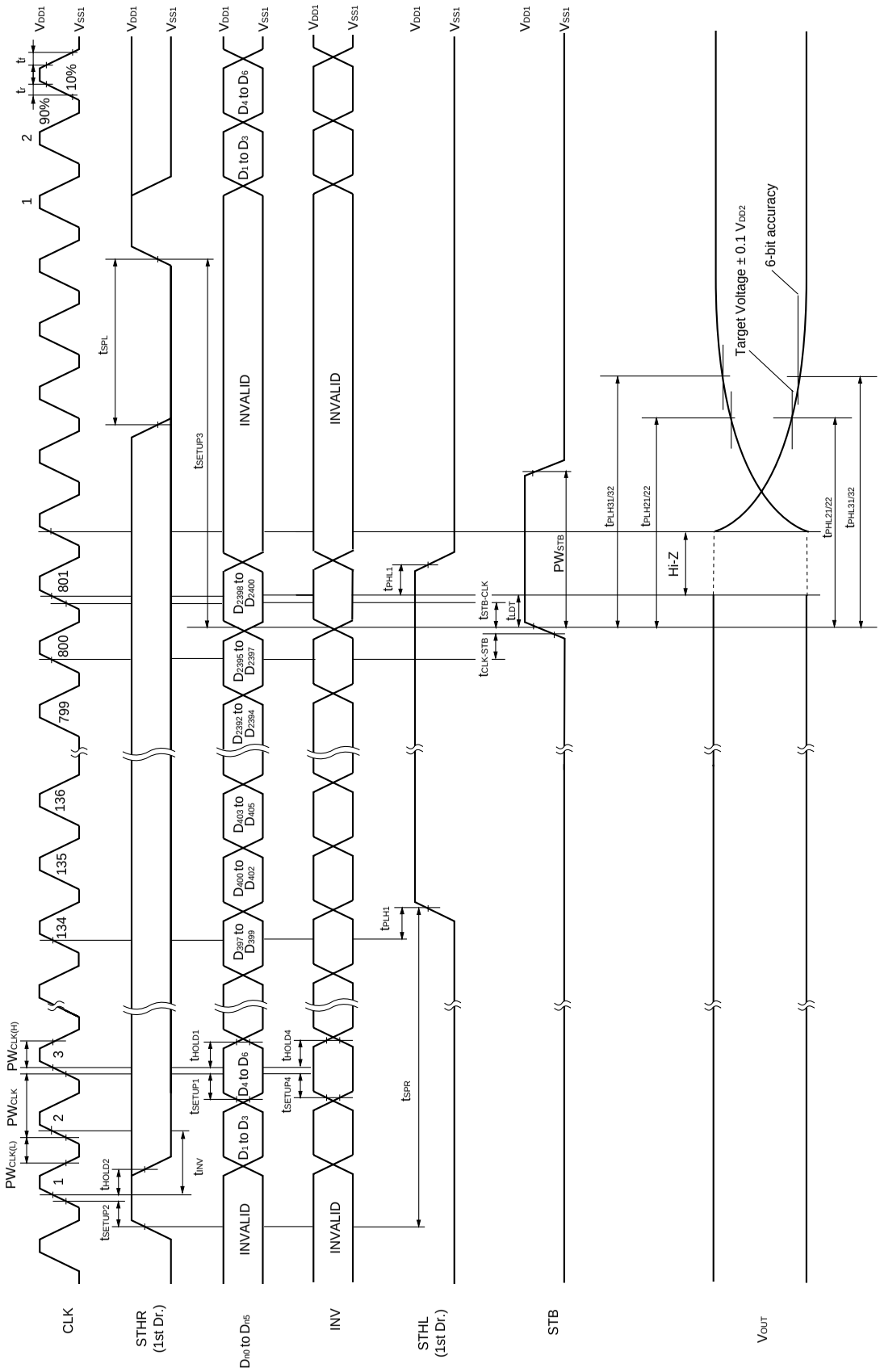


Timing Requirements (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ± 0.3 V, V_{DD2} = 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		20			ns
Clock Low Period	$PW_{CLK (L)}$		4			ns
Clock High Period	$PW_{CLK (H)}$		4			ns
Data Setup Time	t_{SETUP1}		4			ns
Data Hold Time	t_{HOLD1}		0			ns
Start Pulse Setup Time	t_{SETUP2}		4			ns
Start Pulse Hold Time	t_{HOLD2}		0			ns
INV Setup Time	t_{SETUP4}		4			ns
INV Hold Time	t_{HOLD4}		0			ns
Start Pulse Low Period	t_{SPL}		2			CLK
Start Pulse Rise Time	t_{SPR}	384 outputs		128		CLK
		402 outputs		134		CLK
STB Setup Time	t_{SETUP3}		1			CLK
★ STB Pulse Width	PW_{STB}		2			CLK
Data Invalid Period	t_{INV}			1		CLK
Last Data Timing	t_{LDT}				1	CLK
CLK-STB Time	$t_{CLK-STB}$	CLK ↑ → STB ↑	7			ns
STB-CLK Time	$t_{STB-CLK}$	STB ↑ → CLK ↑	7			ns

★ 9. SWITCHING CHARACTERISTIC WAVEFORM(R,/L= H)

Unless otherwise specified, the input level is V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.



10. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μPD16647.

For more details, refer to the **Semiconductor Device Mounting Technology Manual(C10535E).**

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD16647N-xxx : TCP(TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350 °C, heating for 2 to 3 sec ; pressure 100g(per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100 °C ; pressure 3 to 8 kg/cm^2; time 3 to 5 sec. Real bonding 165 to 180 °C pressure 25 to 45 kg/cm^2 time 30 to 40secs(When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite,Ltd).

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System(C10983E)

Quality Grades to NEC's Semiconductor Devices(C11531E)

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  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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