NEC

MOS INTEGRATED CIRCUIT

μPD16654

150/154 OUTPUT TFT-LCD GATE DRIVE

The μPD16654 is a TFT-LCD gate driver. Because this gate driver has a level shift circuit for logic input, it can output a high gate scanning voltage in response to a CMOS-level input.

Moreover, it can also drive both the XGA/SXGA panel (154 outputs) and SVGA panel (150 outputs) by changing the number of outputs over between 150 and 154.

FEATURES

- High breakdown voltage output (ON/OFF range: V_{DD2}-V_{EE2} = 40 V MAX.)
- 3.3 V CMOS level input
- Number of output select function (150/154 outputs)

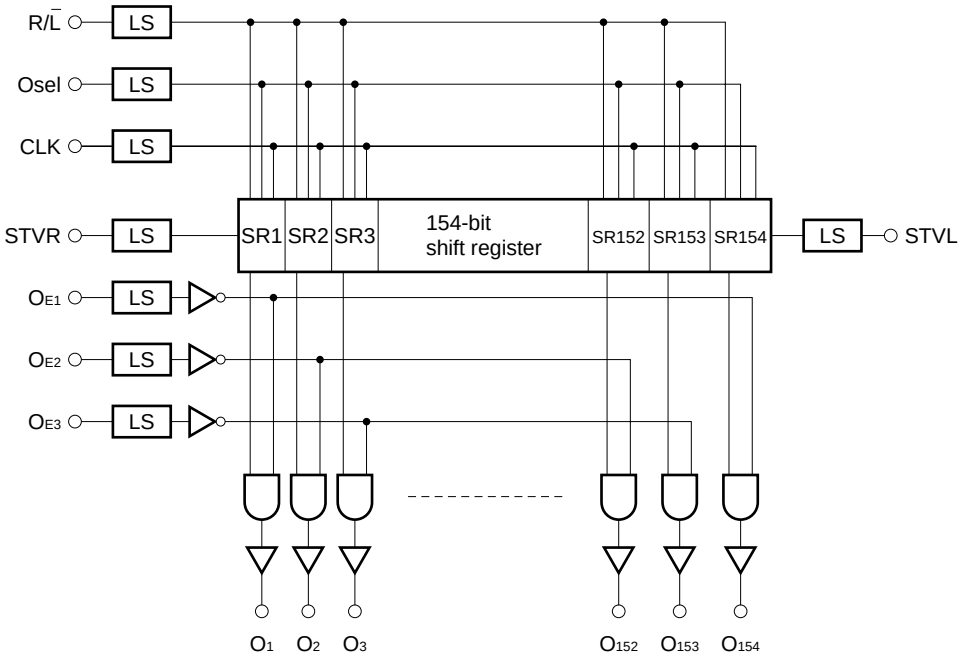
ORDERING INFORMATION

Part Number	Package
μPD16654N-×××	TCP (TAB package)

The TCP's external shape is customized. To order your TCP's external shape, please contact an NEC salesperson.

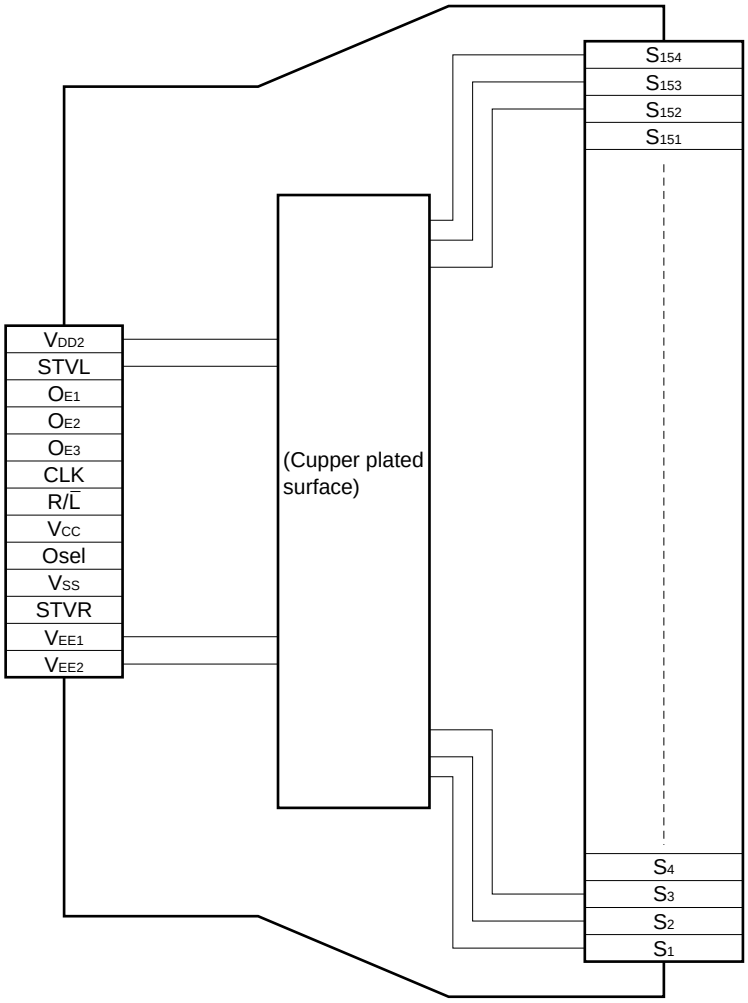
Document No. S11647EJ1V0DS00 (1st edition)
Date Published May 1998 N CP(K)
Printed in Japan

1. BLOCK DIAGRAM



LS (level shifter): Interfaces between 3.3 V CMOS level and V_{DD2}-V_{EE1} level.

2. PIN CONFIGURATION (μPD16654N-xxx)



Caution This figure does not specify the TCP package.

3. PIN FUNCTIONS

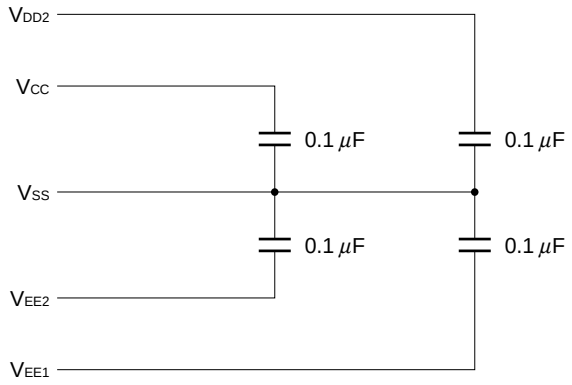
Pin Symbol	Pin Name	Description
O_1 to O_{154}	Driver output pins	Scan signal output pins that drive the gate electrode of a TFT-LCD. The status of each output pin changes in synchronization with the rising edge of shift clock CLK. The output voltage of the driver is V_{DD2} to V_{EE2}.
STVR STVL	Start pulse input/output pin	Input/output pin of the internal shift register. Start pulse signal is read at the rising edge of shift clock CLK and a scan signal is output from the driver output pin. The interface of this terminal is CMOS of 3.3 V. When O_{sel} signal is Low level, start pulse goes up to high level at the 154th falling edge of shift clock CLK and goes down to low level at the 155th falling edge. And when O_{sel} signal is High level, start pulse goes up to high level at the 150th falling edge of shift clock CLK and goes down to low level at the 151st falling edge. The output level is V_{CC}-V_{SS} (logic level).
CLK	Shift clock input	Shift clock input for the internal shift register. The contents of internal shift register is shifted at the rising edge of CLK.
R/$\overline{L}$	Shift direction switching input	Shift direction switching input pin of the internal shift register. R/L = H (right shift) : STVR → O_1 → O_2 ⋯ O_{153} → O_{154} → STVL R/L = L (left shift) STVL → O_{154} → O_{153} ⋯ O_2 → O_1 → STVR
O_{E1} O_{E2} O_{E3}	Enable input	This pin fixes the driver output to the L level when it is high. However, the shift register is not cleared. And, output enable actuation is asynchronous in the clock. And, refer to “RELATIONS OF ENABLE INPUT AND OUTPUT TERMINAL“.
O_{sel}	Number of output select input	Selects the number of outputs. O_{sel} = L : 154 outputs (SVGA) O_{sel} = H: 150 outputs (VGA, XGA, SXGA) When O_{sel} = H (150 outputs), O_{76} through O_{79} outputs of the shift register are fixed to the V_{EE2} level. Fix this pin to V_{CC} (V_{DD2}) or V_{SS} (V_{EE1}) on TCP.
V_{DD2}	Positive power supply for driver	Shared with internal logic and driver
V_{CC}	Reference power supply	3.3 V ± 0.3 V. Reference power supply for level shifter: LS
V_{SS}	Ground (GND)	Connect this pin to the system ground.
V_{EE1}	Negative power supply for internal logic	Negative power supply for internal logic
V_{EE2}	Negative power supply for driver	Negative power supply for driver

Caution 1. Power ON/OFF sequence

To prevent the μPD16654 from damage due to latch up, turn on power in the order V_{CC} → V_{EE1}, V_{EE2} and V_{DD2} → logic input. Turn off power in the reverse order. Observe these power sequences even during transition period.

Caution 2. Inserting bypass capacitor

Because the internal logic operates at a high voltage (V_{DD2}-V_{EE1}), insert a bypass capacitor of about 0.1 μF between the respective power pins as shown below to secure the noise margin of V_{IH} and V_{IL}.



Do not input a switching signal to the O_{sel} pin that selects the number of outputs. Connect this pin to V_{CC} or V_{SS} (V_{EE1}).

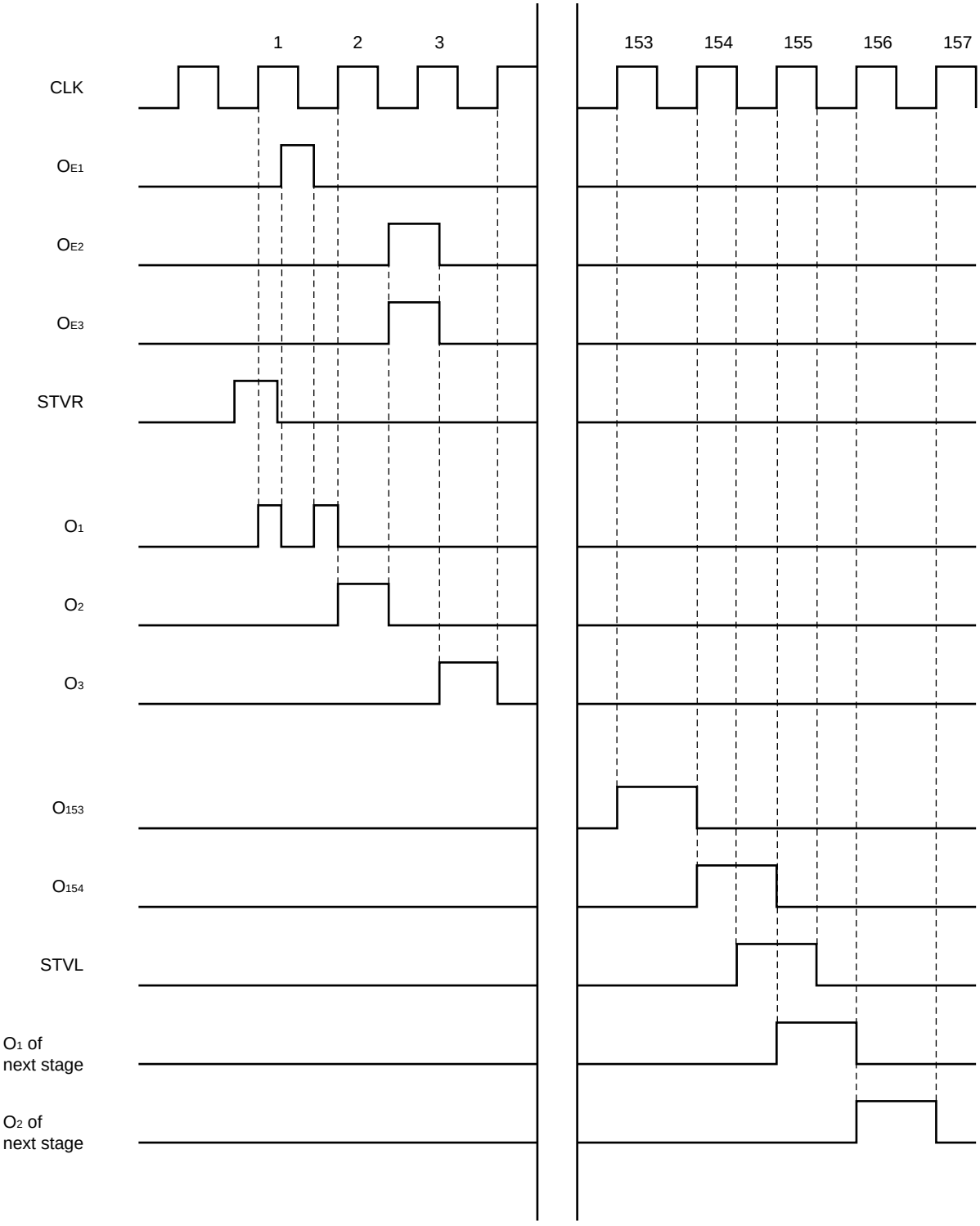
4. RELATIONS OF ENABLE INPUT AND OUTPUT TERMINAL

Switching is possible for 154/150 with μPD16654 by the O_{sel} terminal. And, the output terminal which can be controlled by the enable signal changes as follows along with this function.

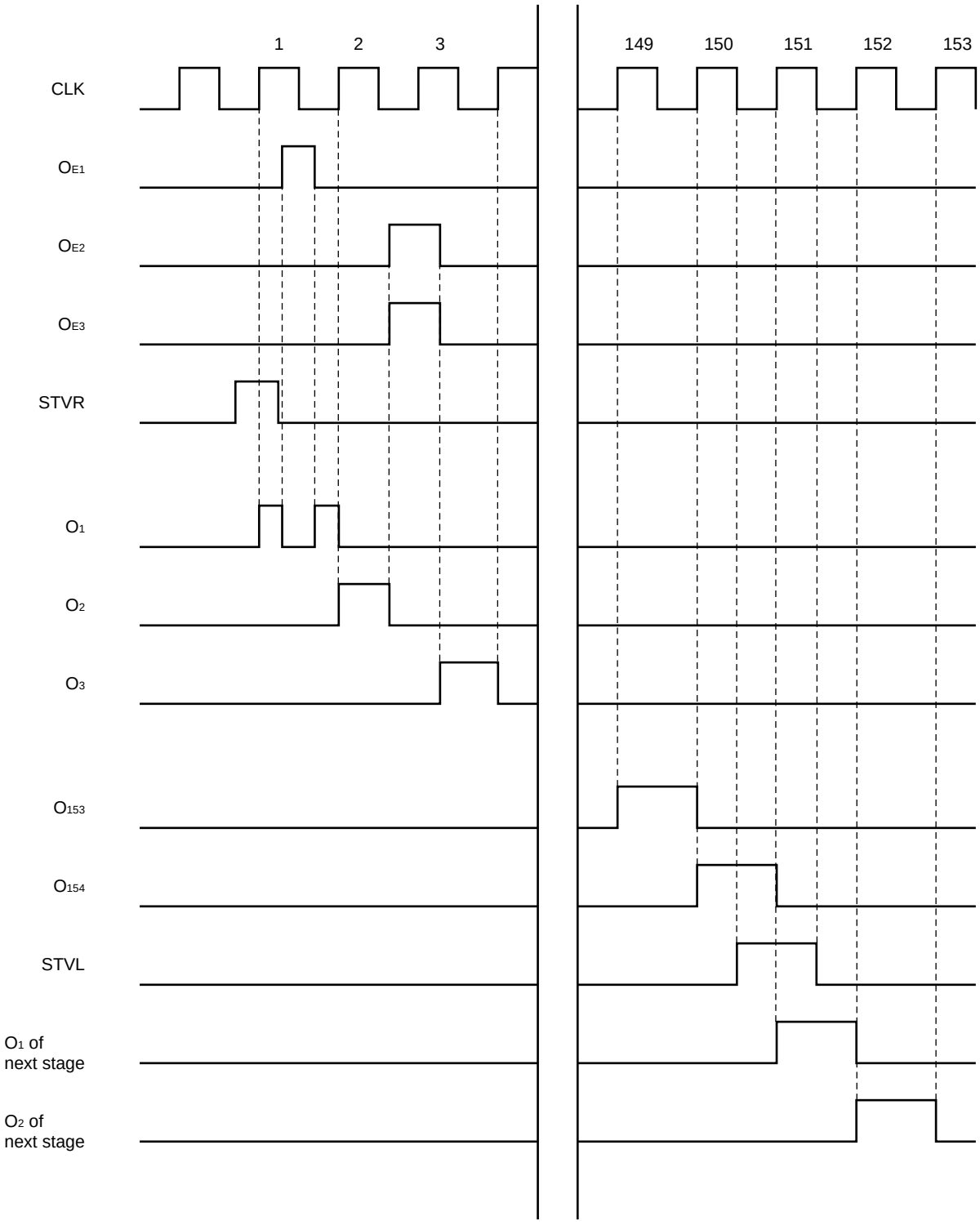
154 out TCP		150 out Mode	
154 out Mode (O_{sel} = L)	150 out Mode (O_{sel} = H)	154 out Mode (O_{sel} = L)	150 out Mode (O_{sel} = H)
O_1 (O_{E1})	O_1 (O_{E1})	O_1 (O_{E1})	O_1 (O_{E1})
O_2 (O_{E2})	O_2 (O_{E2})	O_2 (O_{E2})	O_2 (O_{E2})
O_3 (O_{E3})	O_3 (O_{E3})	O_3 (O_{E3})	O_3 (O_{E3})
O_4 (O_{E1})	O_4 (O_{E1})	O_4 (O_{E1})	O_4 (O_{E1})
O_5 (O_{E2})	O_5 (O_{E2})	O_5 (O_{E2})	O_5 (O_{E2})
O_6 (O_{E3})	O_6 (O_{E3})	O_6 (O_{E3})	O_6 (O_{E3})
• • •	• • •	• • •	• • •
O_{72} (O_{E3})	O_{72} (O_{E3})	O_{72} (O_{E3})	O_{72} (O_{E3})
O_{73} (O_{E1})	O_{73} (O_{E1})	O_{73} (O_{E1})	O_{73} (O_{E1})
O_{74} (O_{E2})	O_{74} (O_{E2})	O_{74} (O_{E2})	O_{74} (O_{E2})
O_{75} (O_{E3})	O_{75} (O_{E3})	O_{75} (O_{E3})	O_{75} (O_{E3})
O_{76} (O_{E1})	V_{out} = V_{EE2}		
O_{77} (O_{E2})	V_{out} = V_{EE2}		
O_{78} (O_{E3})	V_{out} = V_{EE2}		
O_{79} (O_{E1})	V_{out} = V_{EE2}		
O_{80} (O_{E2})	O_{80} (O_{E1})	O_{80} (O_{E2})	O_{80} (O_{E1})
O_{81} (O_{E3})	O_{81} (O_{E2})	O_{81} (O_{E3})	O_{81} (O_{E2})
O_{82} (O_{E1})	O_{82} (O_{E3})	O_{82} (O_{E1})	O_{82} (O_{E3})
• • •	• • •	• • •	• • •
O_{150} (O_{E3})	O_{150} (O_{E2})	O_{150} (O_{E3})	O_{150} (O_{E2})
O_{151} (O_{E1})	O_{151} (O_{E3})	O_{151} (O_{E1})	O_{151} (O_{E3})
O_{152} (O_{E2})	O_{152} (O_{E1})	O_{152} (O_{E2})	O_{152} (O_{E1})
O_{153} (O_{E3})	O_{153} (O_{E2})	O_{153} (O_{E3})	O_{153} (O_{E2})
O_{154} (O_{E1})	O_{154} (O_{E3})	O_{154} (O_{E1})	O_{154} (O_{E3})

5. TIMING CHART

(1) 154 outputs, R/$\overline{L}$ = H O_{sel} = L



(2) 150 outputs, R/$\overline{L}$ = H O_{sel} = H



O_{76} to O_{79} is L (V_{EE2}) level fixation (150 output).

6. ELECTRIC SPECIFICATION

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD2}	–0.5 to +28	V
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Supply Voltage	V_{DD2}-$V_{EE1/2}$	–0.5 to 42	V
Supply Voltage	V_{EE1}	–16.5 to +0.5	V
Supply Voltage	V_{EE2}	V_{EE1} – 0.5 to +0.5	V
Input Voltage	V_I	–0.5 to V_{CC} + 0.5	V
Input Current	I_I	±10	mA
Output Current	I_O	±10	mA
Operating Temperature Range	T_A	–20 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

Recommended Operating Condition (T_A = –20 to +80°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{DD2}	17		25	V
Supply Voltage	V_{EE1}	–15		–5.0	V
Supply Voltage	V_{EE2}	V_{EE1}		V_{EE1} + 6.0	V
Supply Voltage	V_{DD2} – V_{EE1}	22		40	V
Supply Voltage	V_{CC}	3.0	3.3	3.6	V

Electrical Specifications (T_A = –20 to +70°C, V_{DD1} = 25 V, V_{DD2} = 3.3 V ± 0.3 V, V_{EE1} = V_{EE2} = –15 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	CLK, STVR (STVL), R/L, O_{sel}, O_{E1}-O_{E3}	0.8 V_{CC}		V_{CC}	V
Input voltage, low	V_{IL}		V_{SS}		0.2 V_{CC}	V
Output voltage, high	V_{OH}	STVR (STVL), I_{OH} = –40 μA	V_{CC} – 0.4[Note]		V_{CC}[Note]	V
Output voltage, low	V_{OL}	STVR (STVL), I_{OL} = +40 μA	V_{SS}[Note]		V_{SS} + 0.4[Note]	V
Output current, high	I_{nOH}	On, Vn = V_{DD2} – 1.0 V			–1.0	mA
Output current, low	I_{nOL}	On, Vn = V_{EE2} + 1.0 V	1.0			mA
Output ON resistance	R_{on}	Vn = V_{EE2} + 1.0 V or V_{DD2} – 1.0 V			1.0	kΩ
Input leakage current	I_{IL}	V_I = 0 V or 3.6 V			±1.0	μA
Dynamic current	I_{DD2}	V_{DD2}, f_{CLK} = 30 kHz, no loads			400	μA
	I_{CC}	V_{CC1}, f_{CLK} = 30 kHz, no loads			600	μA
	I_{EE}	I_{EE1} + I_{EE2}, f_{CLK} = 30 kHz, no loads			800	μA

Note The cascade output is at the driver level (V_{CC}-V_{SS}).

Switching Characteristics (T_A = –20 to +70°C, V_{DD1} = 25 V, V_{DD2} = 3.3 V ± 0.3 V, V_{EE1} = V_{EE2} = –15 V, V_{SS} = 0 V)

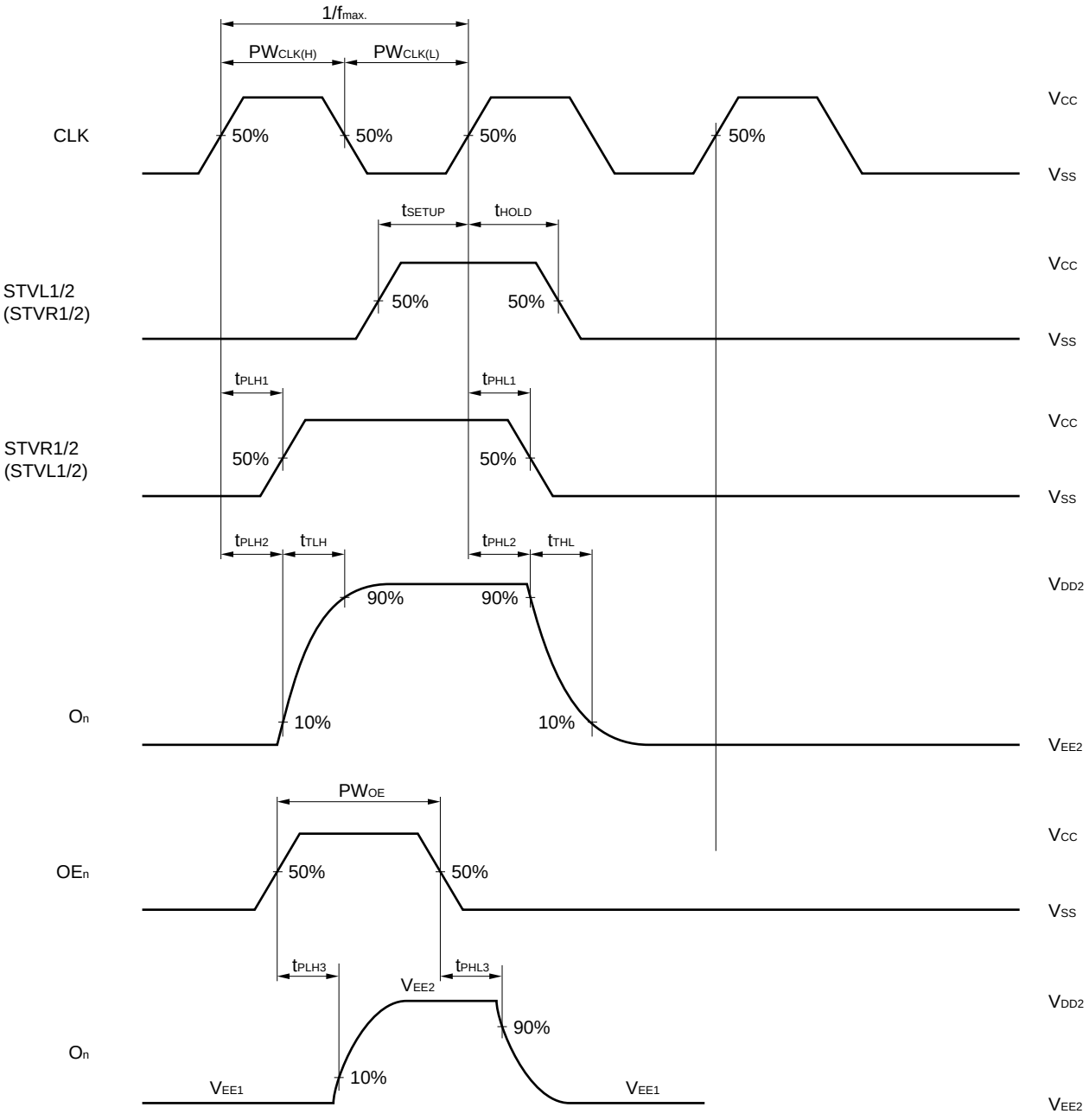
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Cascade output delay time	t_{PHL1}	C_L = 20 pF			800	ns
	t_{PLH1}	CLK → STVL (STVR)			800	ns
Driver output delay time 1	t_{PHL2}	C_L = 300 pF			500	ns
	t_{PLH2}	CLK → On			500	ns
Driver output delay time 2	t_{PHL3}	C_L = 300 pF			500	ns
	t_{PLH3}	O_{En} → On			500	ns
Output rise time	t_{TLH}	C_L = 300 pF			450	ns
Output fall time	t_{THL}				450	ns
Input capacitance	C_I	T_A = 25°C			15	pF
Maximum clock frequency	$f_{max.}$	When connected in cascade	500			kHz

Timing Requirement (T_A = –20 to +70°C, V_{DD1} = 25 V, V_{DD2} = 3.3 V ± 0.3 V, V_{EE1} = V_{EE2} = –15 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Low Period	$PW_{CLK(H)}$		500			ns
Clock Pulse High Period	$PW_{CLK(L)}$		500			ns
Enable Pulse low period	PW_{OE}		1.0			μs
Data Setup Time	t_{SETUP}	STVR (STVL) ↑ → CLK ↑	200			ns
Data Hold Time	t_{HOLD}	CLK ↑ → STVR (STVL) ↓	200			ns

The rise and fall times of logic input must be t_r = t_f = 20 ns (10% to 90%).

7. SWITCHING CHARACTERISTICS WAVEFORM (R/$\overline{L}$ = H)



8. RECOMMENDED MOUNTING CONDITIONS

When mounting this product, please make sure that the following recommended conditions are satisfied.

For packaging methods and conditions other than those recommended below, please contact NEC sales personnel.

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 sec; pressure 100 g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C; pressure 3 to 8 kg/cm^2; time 3 to 5 sec. Real bonding 165 to 180°C; pressure 25 to 45 kg/cm^2, time 30 to 40 secs. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

Reference

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades to NEC's Semiconductor Devices (C11531E)

[MEMO]

[MEMO]

[MEMO]

M4 96.5