

384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

DESCRIPTION

The μ PD16715A is a source driver for TFT-LCDs capable of dealing with displays with 64-gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ -corrected by an internal D/A converter and 5-by-2 external power modules. Because the output dynamic range is as large as $V_{SS2} + 0.1$ V to $V_{DD2} - 0.1$ V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 55 MHz when driving at 3.0 V, this driver is applicable to XGA/SXGA-standard TFT-LCD panels.

FEATURES

- CMOS level input
- 384 outputs
- Input of 6 bits (gradation data) by 6 dots
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter
- Logic power supply (V_{DD1}): 3.3 V \pm 0.3 V
- Driver power supply (V_{DD2}): 11.0 V $\begin{smallmatrix} +2.5 \\ -2.0 \end{smallmatrix}$ V
- High-speed data transfer: $f_{CLK} = 55$ MHz (internal data transfer speed when operating at 3.0 V)
- Output dynamic range $V_{SS2} + 0.1$ V to $V_{DD2} - 0.1$ V
- Apply for only dot-line inversion
- Single bank arrangement is possible (POL)
- Display data inversion function (POL2)
- Low power control function (LPC)
- ★ • Single-sided mounting (Slim TCP)

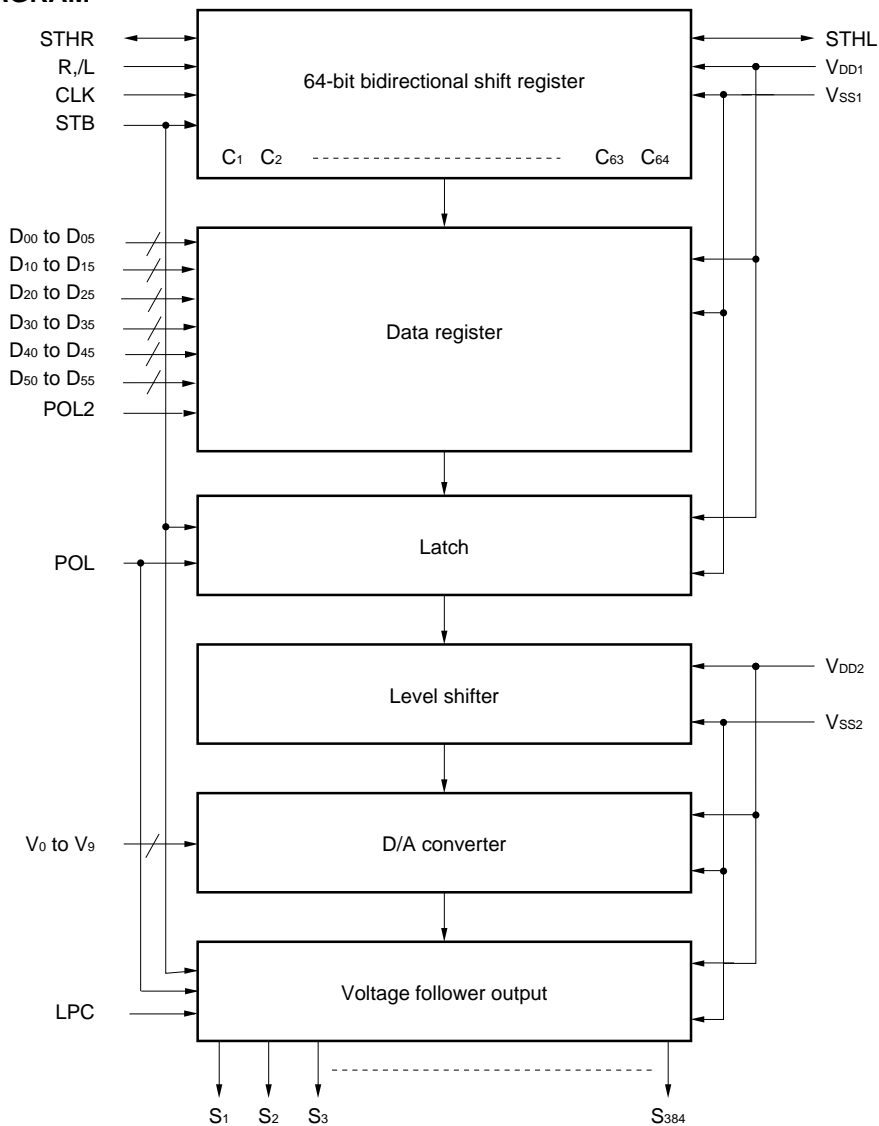
ORDERING INFORMATION

Part Number	Package
μ PD16715AN- xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order your TCP's external shape, please contact an NEC salesperson.

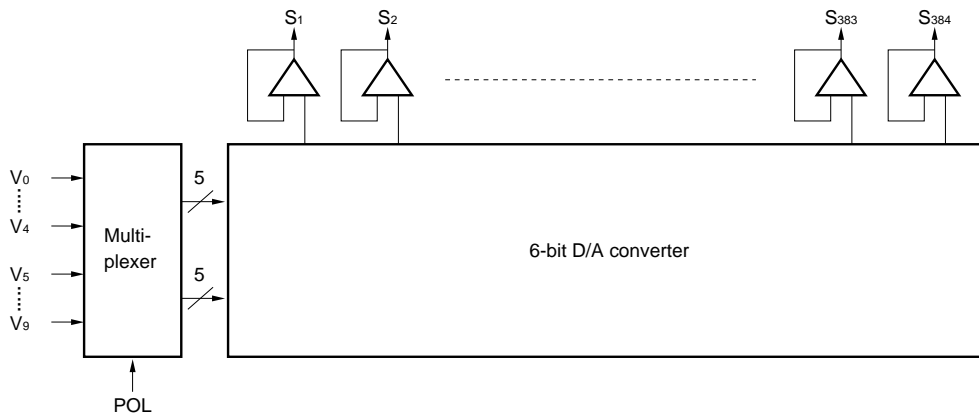
The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

1. BLOCK DIAGRAM

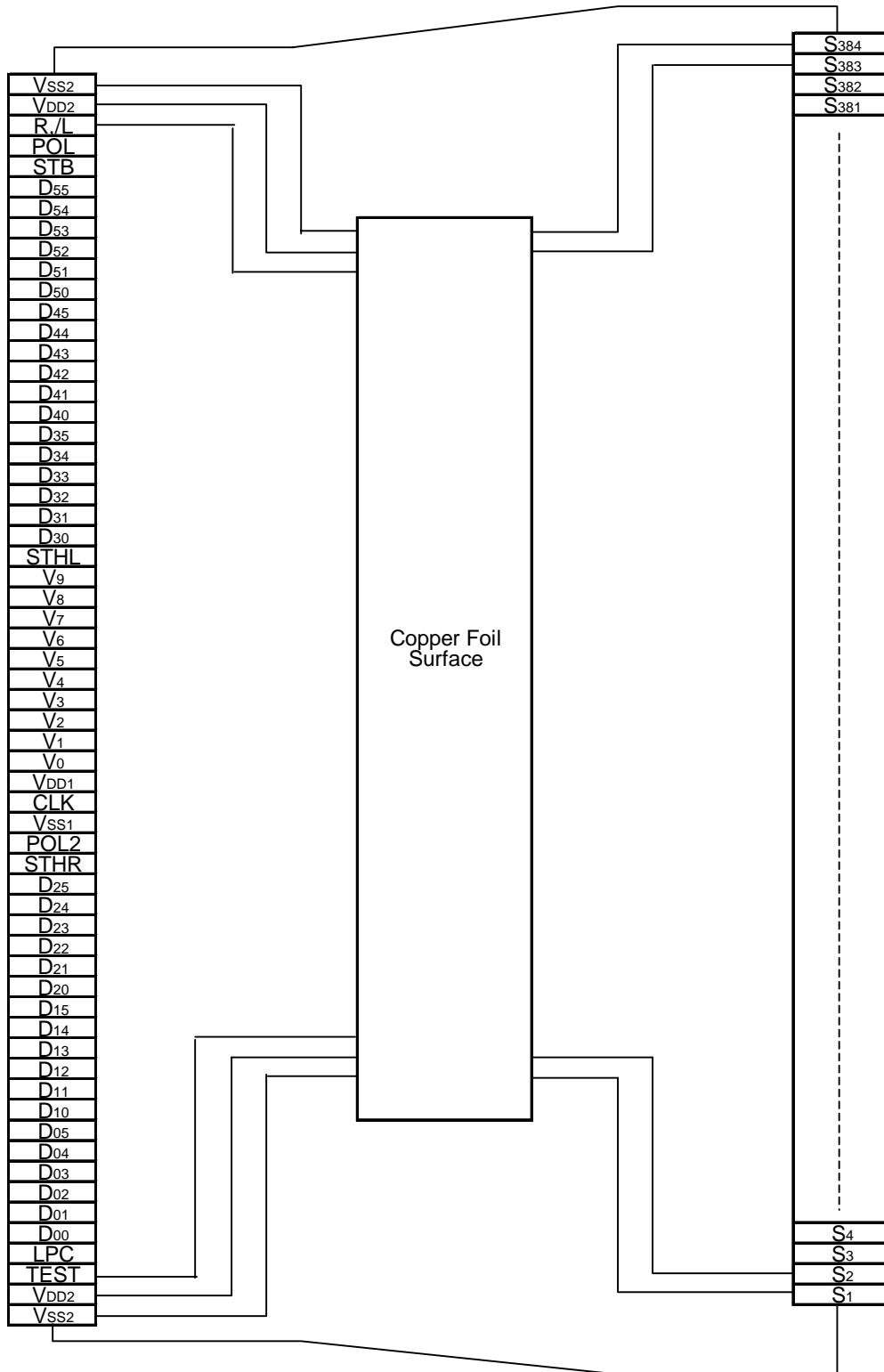


Remark /xxx indicates active low signal.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD16715AN-xxx)



Remark This figure does not specify the TCP package.

4. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	Description
S ₁ to S ₃₈₄	Driver output	The D/A converted 64-gray scale analog voltage is output.
D ₀₀ to D ₀₅	Display data input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D _{X0} : LSB, D _{X5} : MSB
D ₁₀ to D ₁₅		
D ₂₀ to D ₂₅		
D ₃₀ to D ₃₅		
D ₄₀ to D ₄₅		
D ₅₀ to D ₅₅		
R,/L	Shift direction control input	These refer to the start pulse input/output pins when driver ICs are connected in cascade. The shift directions of the shift registers are as follows. R,/L = H: STHR input, S ₁ → S ₃₈₄ , STHL output R,/L = L: STHL input, S ₃₈₄ → S ₁ , STHR output
STHR	Right shift start pulse input/output	R,/L = H: Becomes the start pulse input pin. R,/L = L: Becomes the start pulse output pin.
STHL	Left shift start pulse input/output	R,/L = H: Becomes the start pulse output pin. R,/L = L: Becomes the start pulse input pin.
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 64th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. The initial-level driver's 64th clock becomes valid as the next-level driver's start pulse is input. If 66 clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch input	The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity input	POL = L: The S _{2n-1} output uses V ₀ to V ₄ as the reference supply ; The S _{2n} output uses V ₅ to V ₉ as the reference supply. POL = H: The S _{2n-1} output uses V ₅ to V ₉ as the reference supply ; The S _{2n} output uses V ₀ to V ₄ as the reference supply. S _{2n-1} indicates the odd output: and S _{2n} indicates the even output. Input of the POL signal is allowed the setup time (t _{POL-STB}) with respect to STB's rising edge.
POL2	Data inversion	POL2 = H: Display data is inverted. POL2 = L: Display data is not inverted
LPC	Driver voltage selection	The output buffer constant current source is blocked, reducing current consumption. Low power mode (LPC = 'H': DC-level input possible). The condition that low power mode can be used is that the load constant is at least 10 kΩ + 50 pF.
V ₀ to V ₉	γ -corrected power supplies	Input the γ -corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. V _{DD2} - 0.1 V > V ₀ > V ₁ > V ₂ > V ₃ > V ₄ > V ₅ > V ₆ > V ₇ > V ₈ > V ₉ > V _{SS2} + 0.1 V
TEST	Test pin	Test pin. Please input H or Open.
V _{DD1}	Logic power supply	3.3 V ± 0.3 V
V _{DD2}	Driver power supply	11.0 V ^{+2.5} / _{-2.0} V
V _{SS1}	Logic ground	Grounding
V _{SS2}	Driver ground	Grounding

- Cautions**
1. The power start sequence must be V_{DD1} , logic input, and V_{DD2} & V_0 to V_9 in that order. Reverse this sequence to shut down. (Simultaneous power application to V_{DD2} and V_0 to V_9 is possible.)
 2. To stabilize the supply voltage, please be sure to insert a $0.47 \mu\text{F}$ bypass capacitor between $V_{DD1}-V_{SS1}$ and $V_{DD2}-V_{SS2}$. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about $0.01 \mu\text{F}$ is also advised between the γ -corrected power supply terminals ($V_0, V_1, V_2, \dots, V_9$) and V_{SS2} .

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The μPD16715A incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches. The ladder resistors r_0 to r_{62} are so designed that the ratios between the LCD panel's γ -corrected voltages and V_0 to $V_{63'}$ and V_0'' to $V_{63''}$ are roughly equal; and their respective resistance values are as shown on next page. Among the 5-by-2 γ -corrected voltages, input gray scale voltages of the same polarity with respect to the common voltage, for the respective five γ -corrected voltages of V_0 to V_4 and V_5 to V_9

Figure 5-1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2} , common electrode potential V_{COM} , and γ -corrected voltages V_0 to V_9 and the input data. Be sure to maintain the voltage relationships of

$$V_{DD2} - 0.1 \text{ V} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1 \text{ V}.$$

Figures 5-2 and 5-3 show the relationship between the input data and the output voltage. Therefore, please do not use it for γ -corrected power supply level inversion in double-sided mounting.

Figure 5-1. Relationship Between Input Data and γ -corrected Power Supply

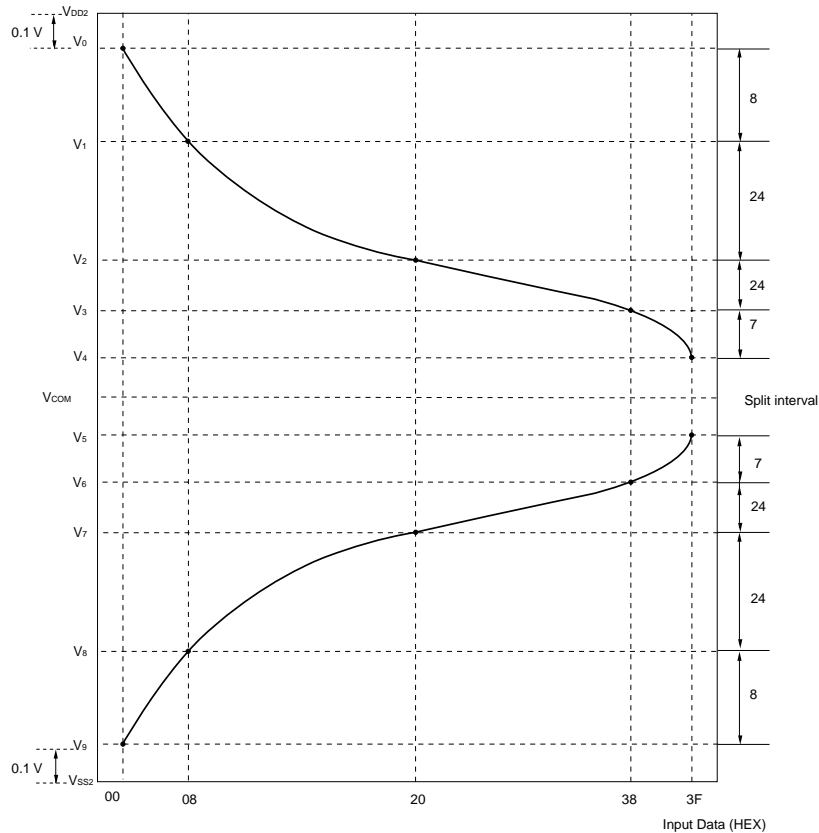
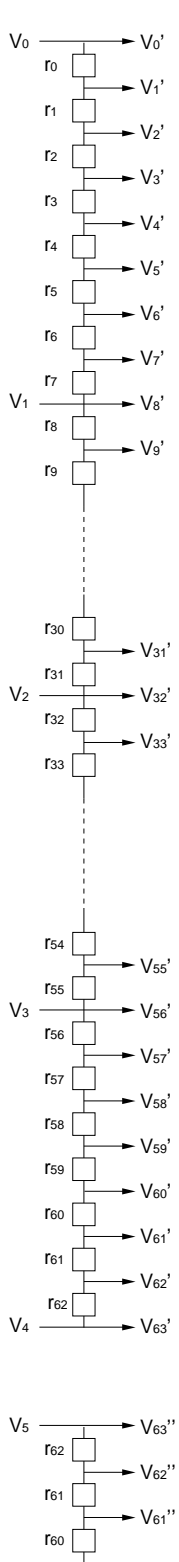


Figure 5-2. Relationship between Input Data and Output Voltage (1/2)

$$V_{DD2} - 0.1 V > V_0 > V_1 > V_2 > V_3 > V_4$$

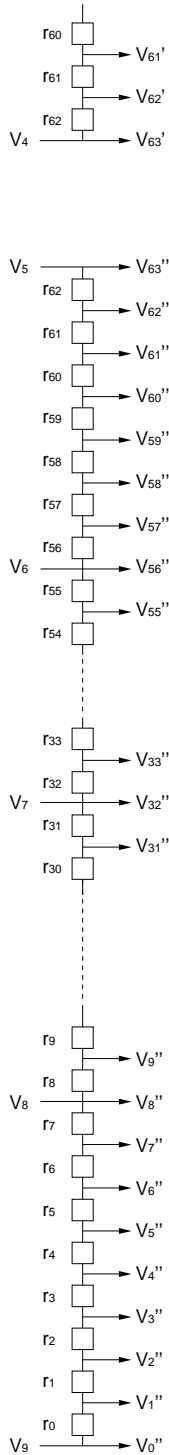


Data	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output Voltage	
00H	0	0	0	0	0	0	V ₀ '	V ₀
01H	0	0	0	0	0	1	V ₁ '	V ₁ +(V ₀ -V ₁)x
02H	0	0	0	0	1	0	V ₂ '	V ₁ +(V ₀ -V ₁)x
03H	0	0	0	0	1	1	V ₃ '	V ₁ +(V ₀ -V ₁)x
04H	0	0	0	1	0	0	V ₄ '	V ₁ +(V ₀ -V ₁)x
05H	0	0	0	1	0	1	V ₅ '	V ₁ +(V ₀ -V ₁)x
06H	0	0	0	1	1	0	V ₆ '	V ₁ +(V ₀ -V ₁)x
07H	0	0	0	1	1	1	V ₇ '	V ₁ +(V ₀ -V ₁)x
08H	0	0	1	0	0	0	V ₈ '	V ₁
09H	0	0	1	0	0	1	V ₉ '	V ₁ +(V ₀ -V ₁)x
0AH	0	0	1	0	1	0	V ₁₀ '	V ₁ +(V ₀ -V ₁)x
0BH	0	0	1	0	1	1	V ₁₁ '	V ₁ +(V ₀ -V ₁)x
0CH	0	0	1	1	0	0	V ₁₂ '	V ₁ +(V ₀ -V ₁)x
0DH	0	0	1	1	0	1	V ₁₃ '	V ₁ +(V ₀ -V ₁)x
0EH	0	0	1	1	1	0	V ₁₄ '	V ₁ +(V ₀ -V ₁)x
0FH	0	0	1	1	1	1	V ₁₅ '	V ₁ +(V ₀ -V ₁)x
10H	0	1	0	0	0	0	V ₁₆ '	V ₁ +(V ₀ -V ₁)x
11H	0	1	0	0	0	1	V ₁₇ '	V ₂ +(V ₁ -V ₂)x
12H	0	1	0	0	1	0	V ₁₈ '	V ₂ +(V ₁ -V ₂)x
13H	0	1	0	0	1	1	V ₁₉ '	V ₂ +(V ₁ -V ₂)x
14H	0	1	0	1	0	0	V ₂₀ '	V ₂ +(V ₁ -V ₂)x
15H	0	1	0	1	0	1	V ₂₁ '	V ₂ +(V ₁ -V ₂)x
16H	0	1	0	1	1	0	V ₂₂ '	V ₂ +(V ₁ -V ₂)x
17H	0	1	0	1	1	1	V ₂₃ '	V ₂ +(V ₁ -V ₂)x
18H	0	1	1	0	0	0	V ₂₄ '	V ₂ +(V ₁ -V ₂)x
19H	0	1	1	0	0	1	V ₂₅ '	V ₂ +(V ₁ -V ₂)x
1AH	0	1	1	0	1	0	V ₂₆ '	V ₂ +(V ₁ -V ₂)x
1BH	0	1	1	0	1	1	V ₂₇ '	V ₂ +(V ₁ -V ₂)x
1CH	0	1	1	1	0	0	V ₂₈ '	V ₂ +(V ₁ -V ₂)x
1DH	0	1	1	1	0	1	V ₂₉ '	V ₂ +(V ₁ -V ₂)x
1EH	0	1	1	1	1	0	V ₃₀ '	V ₂ +(V ₁ -V ₂)x
1FH	0	1	1	1	1	1	V ₃₁ '	V ₂ +(V ₁ -V ₂)x
20H	1	0	0	0	0	0	V ₃₂ '	V ₂
21H	1	0	0	0	0	1	V ₃₃ '	V ₃ +(V ₂ -V ₃)x
22H	1	0	0	0	1	0	V ₃₄ '	V ₃ +(V ₂ -V ₃)x
23H	1	0	0	0	1	1	V ₃₅ '	V ₃ +(V ₂ -V ₃)x
24H	1	0	0	1	0	0	V ₃₆ '	V ₃ +(V ₂ -V ₃)x
25H	1	0	0	1	0	1	V ₃₇ '	V ₃ +(V ₂ -V ₃)x
26H	1	0	0	1	1	0	V ₃₈ '	V ₃ +(V ₂ -V ₃)x
27H	1	0	0	1	1	1	V ₃₉ '	V ₃ +(V ₂ -V ₃)x
28H	1	0	1	0	0	0	V ₄₀ '	V ₃ +(V ₂ -V ₃)x
29H	1	0	1	0	0	1	V ₄₁ '	V ₃ +(V ₂ -V ₃)x
2AH	1	0	1	0	1	0	V ₄₂ '	V ₃ +(V ₂ -V ₃)x
2BH	1	0	1	0	1	1	V ₄₃ '	V ₃ +(V ₂ -V ₃)x
2CH	1	0	1	1	0	0	V ₄₄ '	V ₃ +(V ₂ -V ₃)x
2DH	1	0	1	1	0	1	V ₄₅ '	V ₃ +(V ₂ -V ₃)x
2EH	1	0	1	1	1	0	V ₄₆ '	V ₃ +(V ₂ -V ₃)x
2FH	1	0	1	1	1	1	V ₄₇ '	V ₃ +(V ₂ -V ₃)x
30H	1	1	0	0	0	0	V ₄₈ '	V ₃ +(V ₂ -V ₃)x
31H	1	1	0	0	0	1	V ₄₉ '	V ₄ +(V ₃ -V ₄)x
32H	1	1	0	0	1	0	V ₅₀ '	V ₄ +(V ₃ -V ₄)x
33H	1	1	0	0	1	1	V ₅₁ '	V ₄ +(V ₃ -V ₄)x
34H	1	1	0	1	0	0	V ₅₂ '	V ₄ +(V ₃ -V ₄)x
35H	1	1	0	1	0	1	V ₅₃ '	V ₄ +(V ₃ -V ₄)x
36H	1	1	0	1	1	0	V ₅₄ '	V ₄ +(V ₃ -V ₄)x
37H	1	1	0	1	1	1	V ₅₅ '	V ₄ +(V ₃ -V ₄)x
38H	1	1	1	0	0	0	V ₅₆ '	V ₃
39H	1	1	1	0	0	1	V ₅₇ '	V ₄ +(V ₃ -V ₄)x
3AH	1	1	1	0	1	0	V ₅₈ '	V ₄ +(V ₃ -V ₄)x
3BH	1	1	1	0	1	1	V ₅₉ '	V ₄ +(V ₃ -V ₄)x
3CH	1	1	1	1	0	0	V ₆₀ '	V ₄ +(V ₃ -V ₄)x
3DH	1	1	1	1	0	1	V ₆₁ '	V ₄ +(V ₃ -V ₄)x
3EH	1	1	1	1	1	0	V ₆₂ '	V ₄ +(V ₃ -V ₄)x
3FH	1	1	1	1	1	1	V ₆₃ '	V ₄

r n(Ω)	
r0	800
r1	750
r2	700
r3	650
r4	600
r5	550
r6	550
r7	500
r8	500
r9	400
r10	400
r11	350
r12	350
r13	350
r14	300
r15	300
r16	300
r17	250
r18	250
r19	250
r20	200
r21	200
r22	200
r23	150
r24	150
r25	150
r26	150
r27	100
r28	100
r29	100
r30	100
r31	100
r32	100
r33	100
r34	100
r35	100
r36	100
r37	100
r38	100
r39	100
r40	100
r41	100
r42	100
r43	100
r44	100
r45	100
r46	100
r47	100
r48	100
r49	100
r50	100
r51	100
r52	100
r53	150
r54	150
r55	150
r56	200
r57	200
r58	250
r59	250
r60	300
r61	500
r62	800
rtotal	15850

Figure 5-3. Relationship between Input Data and Output Voltage (2/2)

$$V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1 V$$



Data	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output Voltage		r(Ω)	
00H	0	0	0	0	0	0	V_0''	V_9	r0	800
01H	0	0	0	0	0	1	V_1''	$V_9+(V_8-V_9) \times$	r1	750
02H	0	0	0	0	1	0	V_2''	$V_9+(V_8-V_9) \times$	r2	700
03H	0	0	0	0	1	1	V_3''	$V_9+(V_8-V_9) \times$	r3	650
04H	0	0	0	1	0	0	V_4''	$V_9+(V_8-V_9) \times$	r4	600
05H	0	0	0	1	0	1	V_5''	$V_9+(V_8-V_9) \times$	r5	550
06H	0	0	0	1	1	0	V_6''	$V_9+(V_8-V_9) \times$	r6	550
07H	0	0	0	1	1	1	V_7''	$V_9+(V_8-V_9) \times$	r7	500
08H	0	0	1	0	0	0	V_8''	V_8	r8	500
09H	0	0	1	0	0	1	V_9''	$V_9+(V_8-V_9) \times$	r9	400
0AH	0	0	1	0	1	0	V_{10}''	$V_9+(V_8-V_9) \times$	r10	400
0BH	0	0	1	0	1	1	V_{11}''	$V_9+(V_8-V_9) \times$	r11	350
0CH	0	0	1	1	0	0	V_{12}''	$V_9+(V_8-V_9) \times$	r12	350
0DH	0	0	1	1	0	1	V_{13}''	$V_9+(V_8-V_9) \times$	r13	350
0EH	0	0	1	1	1	0	V_{14}''	$V_9+(V_8-V_9) \times$	r14	300
0FH	0	0	1	1	1	1	V_{15}''	$V_9+(V_8-V_9) \times$	r15	300
10H	0	1	0	0	0	0	V_{16}''	$V_9+(V_8-V_9) \times$	r16	300
11H	0	1	0	0	0	1	V_{17}''	$V_8+(V_7-V_8) \times$	r17	250
12H	0	1	0	0	1	0	V_{18}''	$V_8+(V_7-V_8) \times$	r18	250
13H	0	1	0	0	1	1	V_{19}''	$V_8+(V_7-V_8) \times$	r19	250
14H	0	1	0	1	0	0	V_{20}''	$V_8+(V_7-V_8) \times$	r20	200
15H	0	1	0	1	0	1	V_{21}''	$V_8+(V_7-V_8) \times$	r21	200
16H	0	1	0	1	1	0	V_{22}''	$V_8+(V_7-V_8) \times$	r22	200
17H	0	1	0	1	1	1	V_{23}''	$V_8+(V_7-V_8) \times$	r23	150
18H	0	1	1	0	0	0	V_{24}''	$V_8+(V_7-V_8) \times$	r24	150
19H	0	1	1	0	0	1	V_{25}''	$V_8+(V_7-V_8) \times$	r25	150
1AH	0	1	1	0	1	0	V_{26}''	$V_8+(V_7-V_8) \times$	r26	150
1BH	0	1	1	0	1	1	V_{27}''	$V_8+(V_7-V_8) \times$	r27	100
1CH	0	1	1	1	0	0	V_{28}''	$V_8+(V_7-V_8) \times$	r28	100
1DH	0	1	1	1	0	1	V_{29}''	$V_8+(V_7-V_8) \times$	r29	100
1EH	0	1	1	1	1	0	V_{30}''	$V_8+(V_7-V_8) \times$	r30	100
1FH	0	1	1	1	1	1	V_{31}''	$V_8+(V_7-V_8) \times$	r31	100
20H	1	0	0	0	0	0	V_{32}''	V_7	r32	100
21H	1	0	0	0	0	1	V_{33}''	$V_7+(V_6-V_7) \times$	r33	100
22H	1	0	0	0	1	0	V_{34}''	$V_7+(V_6-V_7) \times$	r34	100
23H	1	0	0	0	1	1	V_{35}''	$V_7+(V_6-V_7) \times$	r35	100
24H	1	0	0	1	0	0	V_{36}''	$V_7+(V_6-V_7) \times$	r36	100
25H	1	0	0	1	0	1	V_{37}''	$V_7+(V_6-V_7) \times$	r37	100
26H	1	0	0	1	1	0	V_{38}''	$V_7+(V_6-V_7) \times$	r38	100
27H	1	0	0	1	1	1	V_{39}''	$V_7+(V_6-V_7) \times$	r39	100
28H	1	0	1	0	0	0	V_{40}''	$V_7+(V_6-V_7) \times$	r40	100
29H	1	0	1	0	0	1	V_{41}''	$V_7+(V_6-V_7) \times$	r41	100
2AH	1	0	1	0	1	0	V_{42}''	$V_7+(V_6-V_7) \times$	r42	100
2BH	1	0	1	0	1	1	V_{43}''	$V_7+(V_6-V_7) \times$	r43	100
2CH	1	0	1	1	0	0	V_{44}''	$V_7+(V_6-V_7) \times$	r44	100
2DH	1	0	1	1	0	1	V_{45}''	$V_7+(V_6-V_7) \times$	r45	100
2EH	1	0	1	1	1	0	V_{46}''	$V_7+(V_6-V_7) \times$	r46	100
2FH	1	0	1	1	1	1	V_{47}''	$V_7+(V_6-V_7) \times$	r47	100
30H	1	1	0	0	0	0	V_{48}''	$V_7+(V_6-V_7) \times$	r48	100
31H	1	1	0	0	0	1	V_{49}''	$V_6+(V_5-V_6) \times$	r49	100
32H	1	1	0	0	1	0	V_{50}''	$V_6+(V_5-V_6) \times$	r50	100
33H	1	1	0	0	1	1	V_{51}''	$V_6+(V_5-V_6) \times$	r51	100
34H	1	1	0	1	0	0	V_{52}''	$V_6+(V_5-V_6) \times$	r52	100
35H	1	1	0	1	0	1	V_{53}''	$V_6+(V_5-V_6) \times$	r53	150
36H	1	1	0	1	1	0	V_{54}''	$V_6+(V_5-V_6) \times$	r54	150
37H	1	1	0	1	1	1	V_{55}''	$V_6+(V_5-V_6) \times$	r55	150
38H	1	1	1	0	0	0	V_{56}''	V_6	r56	200
39H	1	1	1	0	0	1	V_{57}''	$V_6+(V_5-V_6) \times$	r57	200
3AH	1	1	1	0	1	0	V_{58}''	$V_6+(V_5-V_6) \times$	r58	250
3BH	1	1	1	0	1	1	V_{59}''	$V_6+(V_5-V_6) \times$	r59	250
3CH	1	1	1	1	0	0	V_{60}''	$V_6+(V_5-V_6) \times$	r60	300
3DH	1	1	1	1	0	1	V_{61}''	$V_6+(V_5-V_6) \times$	r61	500
3EH	1	1	1	1	1	0	V_{62}''	$V_6+(V_5-V_6) \times$	r62	800
3FH	1	1	1	1	1	1	V_{63}''	V_5	rtotal	15850

6. RELATIONSHIP BETWEEN OUTPUT DATA AND D/A CONVERTER

Data format : 6 bits × 2 RGBs (6 dots)

Input width : 36 bits (2-pixel data)

R,/L = H (Right shift)

Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₈₃	S ₃₈₄
Data	D ₀₀ to D ₀₅	D ₁₀ to D ₁₅	D ₂₀ to D ₂₅	D ₃₀ to D ₃₅	...	D ₄₀ to D ₄₅	D ₅₀ to D ₅₅

R,/L = L (Left shift)

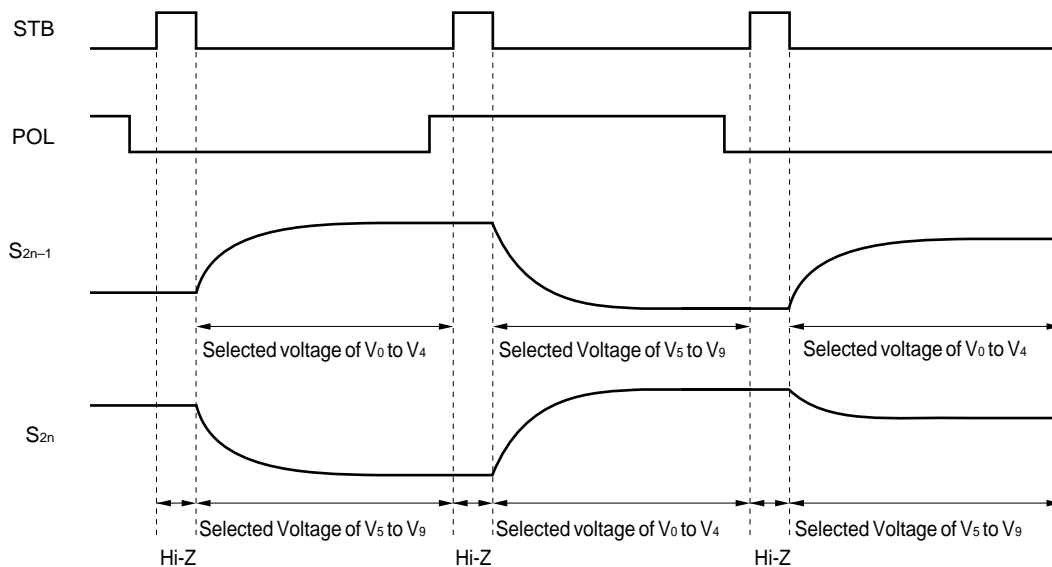
Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₈₃	S ₃₈₄
Data	D ₀₀ to D ₀₅	D ₁₀ to D ₁₅	D ₂₀ to D ₂₅	D ₃₀ to D ₃₅	...	D ₄₀ to D ₄₅	D ₅₀ to D ₅₅

POL	S _{2n-1} ^{Note}	S _{2n} ^{Note}
L	V ₀ to V ₄	V ₅ to V ₉
H	V ₅ to V ₉	V ₀ to V ₄

Note S_{2n-1} (Odd output), S_{2n} (Even output), n = 1,2,...,192

7. RELATIONSHIP BETWEEN STB, POL, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.



8. RELATIONSHIP BETWEEN OUTPUT DATA AND D/A CONVERTER

The μPD16715A is a dot inversion and inverts dots by alternately using a charging output buffer and a discharging output buffer. Therefore, the output voltage of the first line may not be correctly written because the last line's output polarity of frame n (n + 1) and the first line's output polarity are the same (refer to Figure 8-1).

Consequently, polarity inversion and write operation must be performed between frames (vertical blanking period) in order to invert (clear) the polarity of the wiring level of the liquid crystal panel by using the last line output of the previous frame (refer to Figure 8-2).

Figure 8-1. Incase of the output voltage may not be correctly written

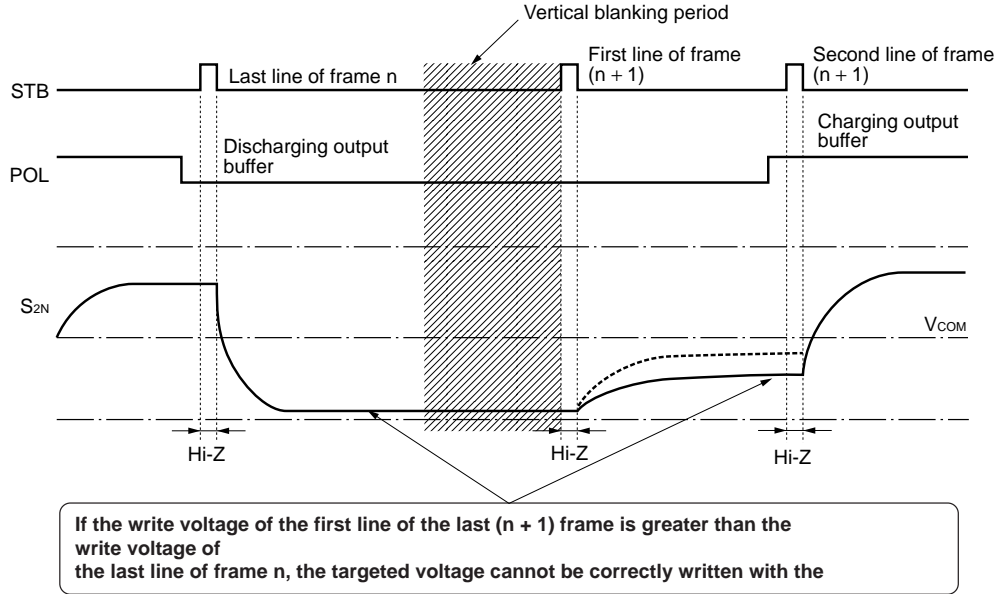
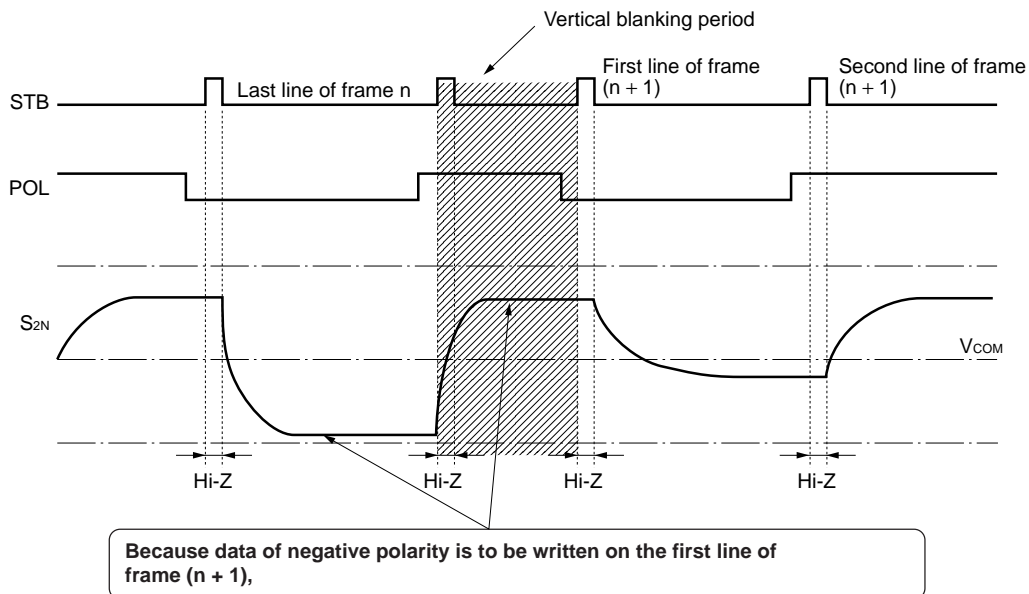


Figure 8-2. Polarity inversion and write operation



5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings ($T_A = 25\text{ }^\circ\text{C}$, $V_{SS1} = V_{SS2} = 0\text{ V}$)

Parameter	Symbol	Ratings	Unit
Logic Part Supply Voltage	V_{DD1}	-0.3 to + 6.5	V
Driver Part Supply Voltage	V_{DD2}	-0.5 to + 15.0	V
Logic Part Input Voltage	V_{I1}	-0.3 to $V_{DD1} + 0.3$	V
Driver Part Input Voltage	V_{I2}	-0.3 to $V_{DD2} + 0.3$	V
Logic Part Output Voltage	V_{O1}	-0.3 to $V_{DD1} + 0.3$	V
Driver Part Output Voltage	V_{O2}	-0.3 to $V_{DD2} + 0.3$	V
Operating Ambient Temperature	T_A	-10 to +75	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +125	$^\circ\text{C}$

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range ($T_A = -10\text{ to }+75\text{ }^\circ\text{C}$, $V_{SS1} = V_{SS2} = 0\text{ V}$)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Supply Voltage	V_{DD1}	3.0	3.3	3.6	V
Driver Supply Voltage	V_{DD2}	9.0	11.0	13.5	V
High-Level Input Voltage	V_{IH}	$0.7 V_{DD1}$		V_{DD1}	V
Low-Level Input Voltage	V_{IL}	0		$0.3 V_{DD1}$	V
γ -Corrected Voltage	V_0 to V_9	$V_{SS2} + 0.1$		$V_{DD2} - 0.1$	V
Driver Part Output Voltage	V_O	$V_{SS2} + 0.1$		$V_{DD2} - 0.1$	V
Clock Frequency	f_{CLK}			55	MHz

Electrical Characteristics (T_A = -10 to +75 °C, V_{DD1} = 3.3 V ± 0.3 V, V_{DD2} = 11.0 V^{+2.5}_{-2.0} V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Input Leak Current	I _{IL}				±1.0	μA	
High-Level Output Voltage	V _{OH}	STHR (STHL), I _{OH} = 0 mA	V _{DD1} - 0.1		V _{DD1}	V	
Low-Level Output Voltage	V _{OL}	STHR (STHL), I _{OL} = 0 mA			0.1	V	
★ γ-Corrected Supply Current	I _γ	V _{DD2} = 13 V, V ₀ to V ₄ = V ₅ to V ₉ = 6.0 V	V ₀ pin, V ₅ pin		0.31	0.8	mA
			V ₄ pin, V ₉ pin	-0.8	-0.31		mA
Driver Output Current	I _{VOH}	V _X = 8.0 V, V _{OUT} = 6.0 V			-0.25	mA	
	I _{VOL}	V _X = 1.0 V, V _{OUT} = 3.0 V	0.25			mA	
Output Voltage Deviation	ΔV _O	Input data			±20	mV	
Average Output Voltage Variation	ΔV _{AV}	Input data		±10		mV	
Output Voltage Range	V _O	Input data	V _{DD2} + 0.1		V _{DD2} - 0.1	V	
Logic Part Dynamic Current Consumption	I _{DD1}	V _{DD1} = 3.6 V, T _A = 25°C		1.5	8	mA	
Driver Part Dynamic Current Consumption	I _{DD2}	V _{DD1} = 3.0 V, V _{DD2} = 13.5 V, No loads, T _A = 25°C		3.5	8	mA	

- Cautions 1.** The output voltage deviation refers to the voltage difference between adjoining output pins when the display data is the same (within the chip).
- 2.** The average output voltage variation refers to the average output voltage difference between chips. The average output voltage refers to the average voltage between chips when the display data is the same.
- 3.** The STB cycle is defined to be 20 μs at f_{CLK} = 33 MHz.
- 4.** The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.
- 5.** Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (8 units).

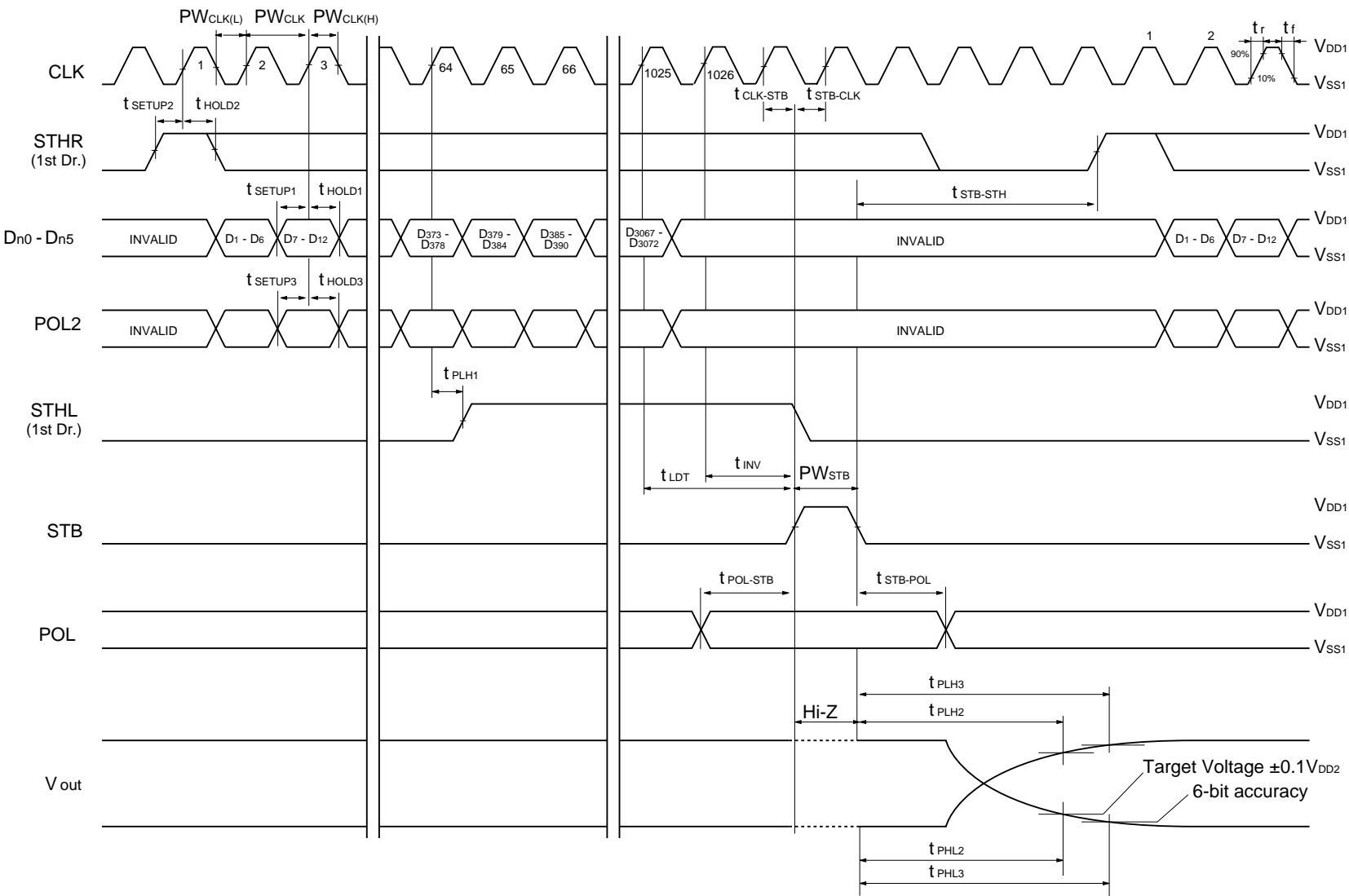
Switching Characteristics (T_A = -10 to +75 °C, V_{DD1} = 3.3 V ± 0.3 V, V_{DD2} = 11.0 V^{+2.5}_{-2.0} V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t _{PLH1}	C _L = 25 pF		9.1	14	ns
Driver Output Delay Time	t _{PLH2}	C _L = 50 pF, R _L = 50 kΩ		5.2	11	μs
	t _{PLH3}			9.9	17	μs
	t _{PHL2}			5.3	11	μs
	t _{PHL3}			10.4	17	μs
Input Capacitance	C _{I1}	STHR (STHL) excluded, T _A = 25°C		5.8	15	pF
	C _{I2}	STHR (STHL), T _A = 25°C		5.7	15	pF

Timing Requirement ($T_A = -10$ to $+75$ °C, $V_{DD1} = 3.3$ V \pm 0.3 V, $V_{SS1} = V_{SS2} = 0$ V, $t_r = t_f = 8.0$ ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW _{CLK}		18			ns
Clock Pulse High Period	PW _{CLK(H)}		5			ns
Clock Pulse Low Period	PW _{CLK(L)}		5			ns
Data Setup Time	t _{SETUP1}		0			ns
Data Hold Time	t _{HOLD1}		8			ns
Start Pulse Setup Time	t _{SETUP2}		4			ns
Start Pulse Hold Time	t _{HOLD2}		5			ns
POL2 Setup Time	t _{SETUP3}		0			ns
POL2 Hold Time	t _{HOLD3}		8			ns
STB Pulse Width	PW _{STB}		500			ns
Data Invalid Period	t _{INV}		1			CLK
Last Data Timing	t _{LDT}		2			CLK
CLK-STB Time	t _{CLK-STB}	CLK \uparrow \rightarrow STB \uparrow	5			ns
STB-CLK Time	t _{STB-CLK}	STB \uparrow \rightarrow CLK \uparrow	5			ns
Time Between STB and Start Pulse	t _{STB-STH}	STB \uparrow \rightarrow STHR(STHL) \uparrow	50			ns
POL-STB Time	t _{POL-STB}	POL \uparrow or \downarrow \rightarrow STB \uparrow	-7			ns
STB-POL Time	t _{STB-POL}	STB \downarrow \rightarrow POL \downarrow or \uparrow	9			ns

★ 9. SWITCHING CHARACTERISTICS WAVEFORM (R/L = H)
 (Unless otherwise specified, the input level is defined to be $V_{IH} = 0.5 V_{DD1}$.)



7. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the μPD16715A.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Type of Surface Mount Device

μPD16715AN-xxx : TCP (TAB package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 seconds: pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm ² : time 3 to 5 seconds. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm ² : time 30 to 40 seconds. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents**NEC Semiconductor Device Reliability / Quality Control System (C10983E)****Quality Grades to NEC's Semiconductor Devices (C11531E)**

- **The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.**
 - No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.
 - NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.
 - Descriptions of circuits, software, and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software, and information in the design of the customer's equipment shall be done under the full responsibility of the customer. NEC Corporation assumes no responsibility for any losses incurred by the customer or third parties arising from the use of these circuits, software, and information.
 - While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.
 - NEC devices are classified into the following three quality grades:
"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
 - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
 - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
 - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.
- The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.