

MONOLITHIC DUAL H BRIDGE DRIVER CIRCUIT

DESCRIPTION

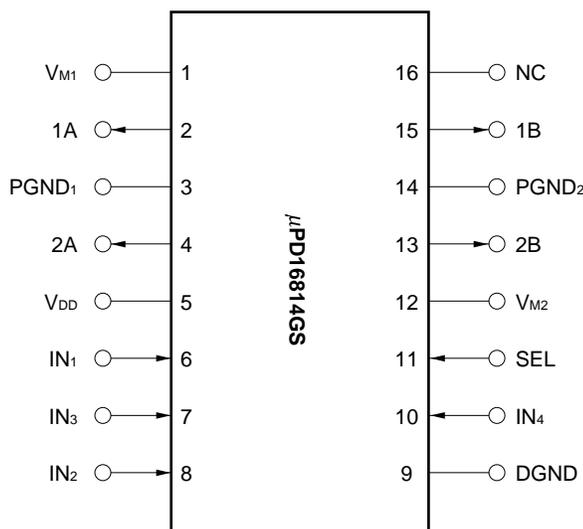
The μ PD16814GS is a monolithic dual H bridge driver circuit employing a power MOS FET for its driver stage. By complementing the P channel and N channel of the output stage, the circuit current is substantially improved as compared with that of the conventional charge pump driver.

Because the dual H bridge driver circuits at the output stage are independent of each other, this IC is ideal as the driver circuit for a 1- to 2-phase excitation bipolar driving stepping motor for the head actuator of an FDD.

FEATURES

- Low ON resistance (sum of ON resistance of top and bottom FETs)
 $R_{ON1} = 2.0 \Omega$ TYP.
- Low current consumption: $I_{DD} = 100 \mu A$ MAX.
- Four input modes independently controlling dual H bridge drivers
- Stop and Brake modes selectable
- Surface-mount mini-mold package: 16-pin plastic SOP (300 mil)

PIN CONFIGURATION (Top View)

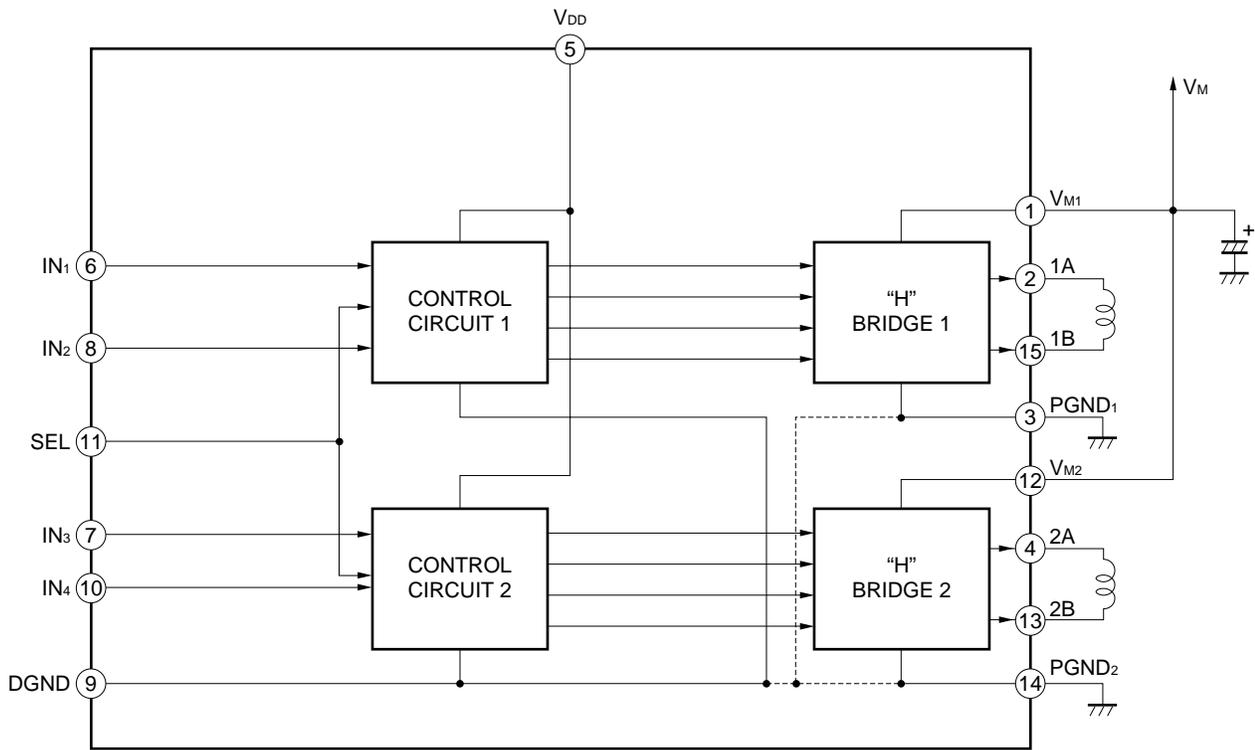


ORDERING INFORMATION

Part Number	Package
μ PD16814GS	16-pin plastic SOP (300 mil)

The information in this document is subject to change without notice.

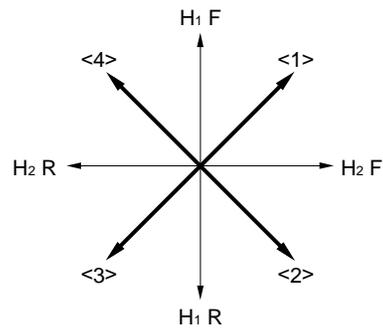
BLOCK DIAGRAM



FUNCTION TABLE

• In Stop mode (SEL = High)

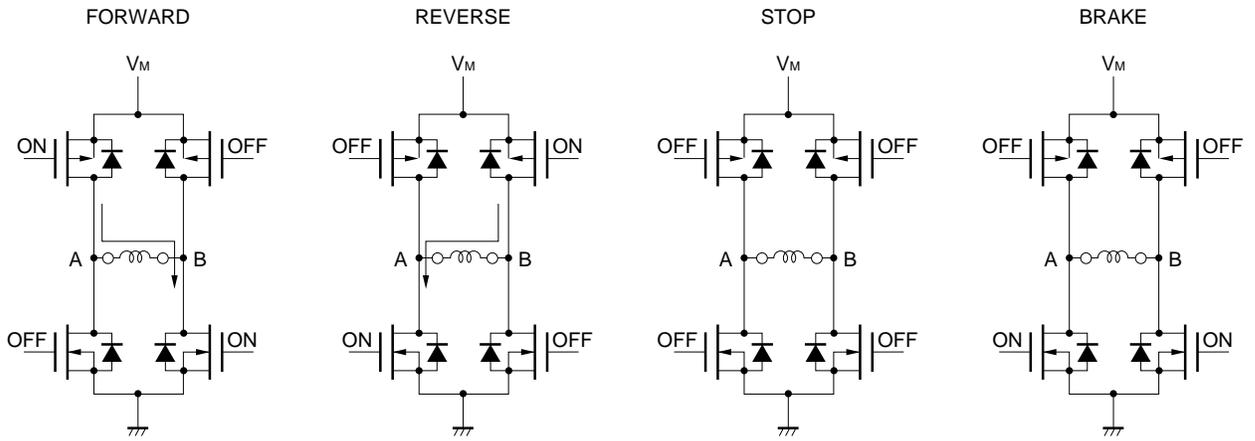
Excitation Direction	IN ₁	IN ₂	IN ₃	IN ₄	H ₁	H ₂
—	L	L	L	L	S	S
H ₂ R	L	L	L	H	S	R
H ₂ F	L	L	H	L	S	F
—	L	L	H	H	S	S
H ₁ R	L	H	L	L	R	S
<3>	L	H	L	H	R	R
<2>	L	H	H	L	R	F
H ₁ R	L	H	H	H	R	S
H ₁ F	H	L	L	L	F	S
<4>	H	L	L	H	F	R
<1>	H	L	H	L	F	F
H ₁ F	H	L	H	H	F	S
—	H	H	L	L	S	S
H ₂ R	H	H	L	H	S	R
H ₂ F	H	H	H	L	S	F
—	H	H	H	H	S	S



• In Brake mode (SEL = Low)

Excitation Direction	IN ₁	IN ₂	IN ₃	IN ₄	H ₁	H ₂
—	L	L	L	L	B	B
H ₂ R	L	L	L	H	B	R
H ₂ F	L	L	H	L	B	F
—	L	L	H	H	B	B
H ₁ R	L	H	L	L	R	B
<3>	L	H	L	H	R	R
<2>	L	H	H	L	R	F
H ₁ R	L	H	H	H	R	B
H ₁ F	H	L	L	L	F	B
<4>	H	L	L	H	F	R
<1>	H	L	H	L	F	F
H ₁ F	H	L	H	H	F	B
—	H	H	L	L	B	B
H ₂ R	H	H	L	H	B	R
H ₂ F	H	H	H	L	B	F
—	H	H	H	H	B	B

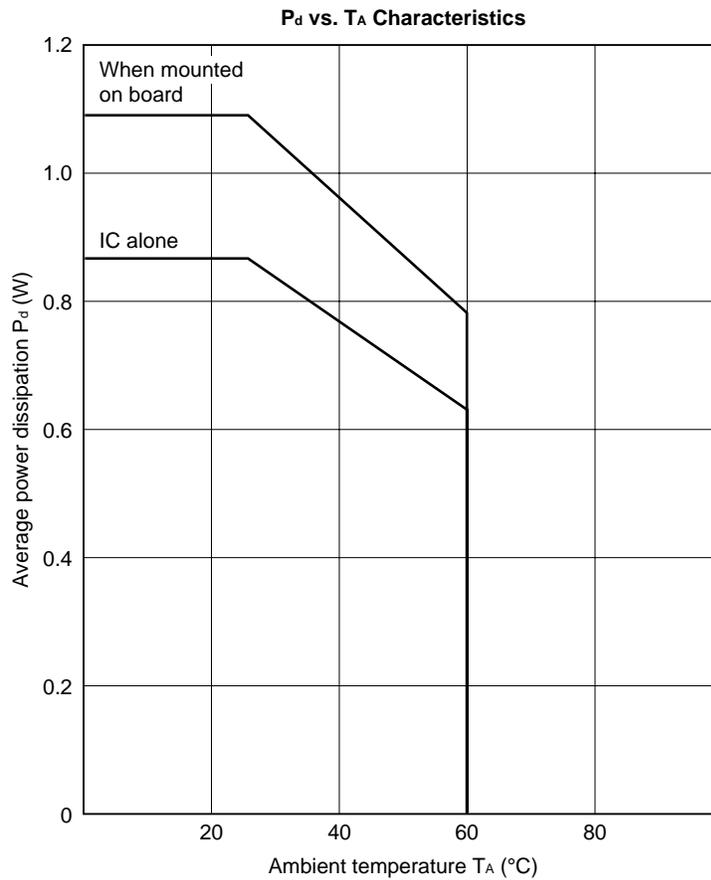
F: Forward R: Reverse S: Stop B: Brake



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Ratings	Unit
Supply voltage (motor block)	V _M	-0.5 to +7	V
Supply voltage (control block)	V _{DD}	-0.5 to +7	V
Power dissipation	P _{d1}	0.862 ^{Note 1}	W
	P _{d2}	1.087 ^{Note 2}	
Instantaneous H bridge driver current	I _{D (pulse)}	±1.0 ^{Note 2,3}	A
Input voltage	V _{IN}	-0.5 to V _{DD} + 0.5	V
Operating temperature	T _A	0 to 60	°C
Junction temperature	T _{J MAX.}	150	°C
Storage temperature	T _{stg}	-55 to +125	°C

- Notes 1.** IC alone.
2. When mounted on board (100 × 100 × 1 mm, glass epoxy)
3. t ≤ 5 ms, Duty ≤ 40%



RECOMMENDED OPERATING CONDITIONS (T_A = 25 °C)

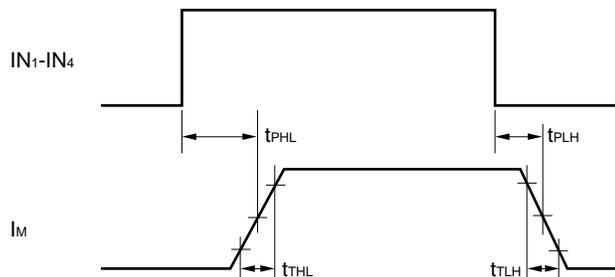
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage (motor block)	V _M	4.0	5.0	6.0	V
Supply voltage (control block)	V _{DD}	4.0	5.0	6.0	V
H bridge drive current ^{Note}	I _{DR}			±415	mA
Operating temperature	T _A	0		60	°C

Note When mounted on board (100 × 100 × 1 mm, glass epoxy)

ELECTRICAL CHARACTERISTICS (Within recommended operating conditions unless otherwise specified)

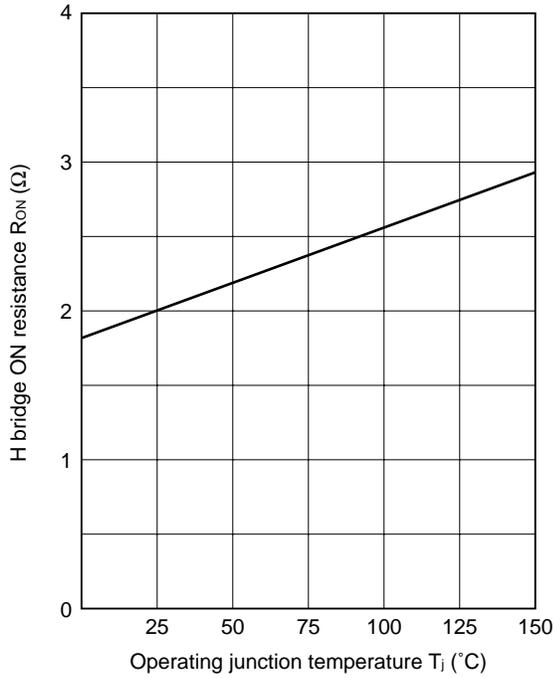
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
V _M pin current with output transistor OFF	I _M	V _M = 6.0 V, V _{DD} = 6.0 V			1.0	μA
V _{DD} pin current	I _{DD}				0.1	mA
Control pin high-level input current	I _{IH}	V _{IN} = V _{DD}			1.0	μA
Control pin low-level input current	I _{IL}	V _{IN} = 0 V			-1.0	μA
Control pin high-level input voltage	V _{IH}		3.0		V _{DD} + 0.3	V
Control pin low-level input voltage	V _{IL}		-0.3		0.8	V
H bridge circuit ON resistance ^{Note 1}	R _{ON1}	V _M = 5 V, V _{DD} = 5 V		2.0	4.0	Ω
R _{ON} relative accuracy	ΔR _{ON}	Excitation direction <2>, <4> ^{Note 2}			±5	%
	ΔR _{ON}	Excitation direction <1>, <3>			±10	
H bridge output circuit propagation delay time	t _{PHL}	V _M = 5 V, V _{DD} = 5 V ^{Note 3} T _A = 25 °C, R _M = 20 Ω		1.8	2.5	μs
H bridge output circuit propagation delay time	t _{PLH}			0.2	0.65	
H bridge output circuit rise time	t _{THL}	V _M = 5 V, V _{DD} = 5 V ^{Note 3} T _A = 25 °C, R _M = 20 Ω		0.2	0.4	μs
H bridge output circuit fall time	t _{TLH}			0.1	0.2	

- Notes**
- Sum of ON resistance of top and bottom transistors
 - For the excitation direction, refer to **FUNCTION TABLE**.
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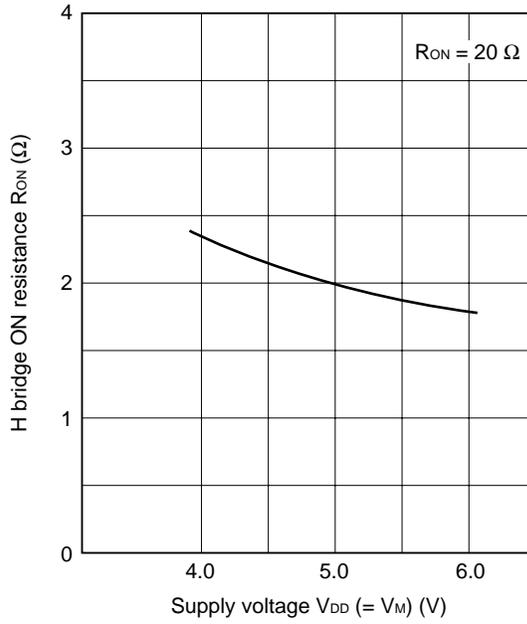


TYPICAL CHARACTERISTICS

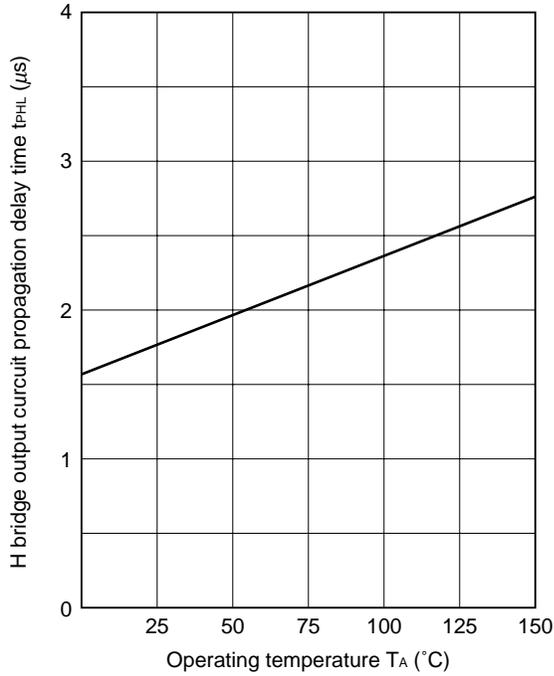
R_{ON} vs. T_J Characteristics



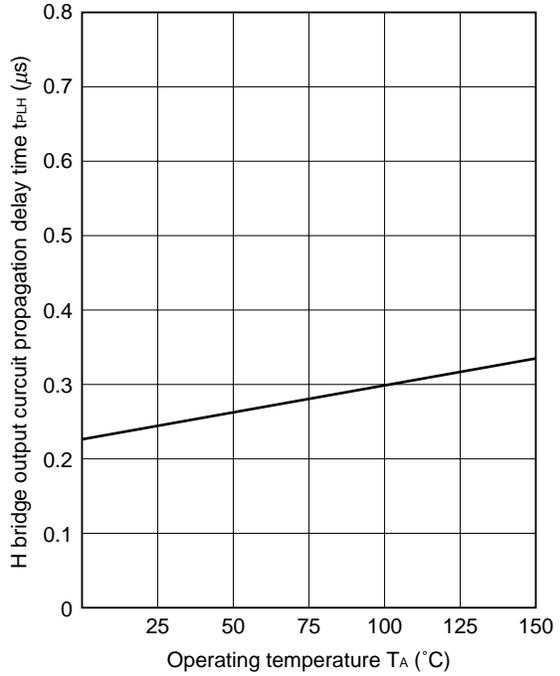
R_{ON} vs. V_{DD} (= V_M) Characteristics



t_{PHL} vs. T_A Characteristics

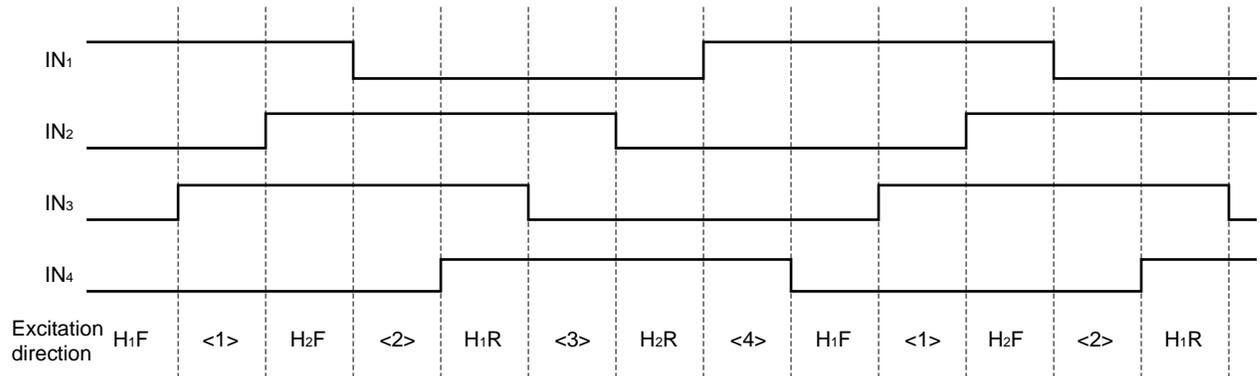


t_{PLH} vs. T_A Characteristics

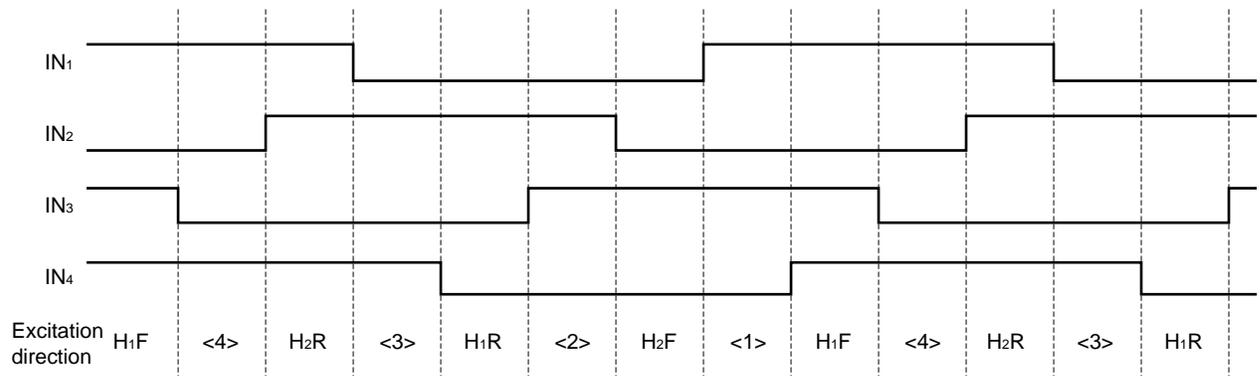


STEPPING MOTOR EXCITATION TIMING CHART

Inner circumference seek



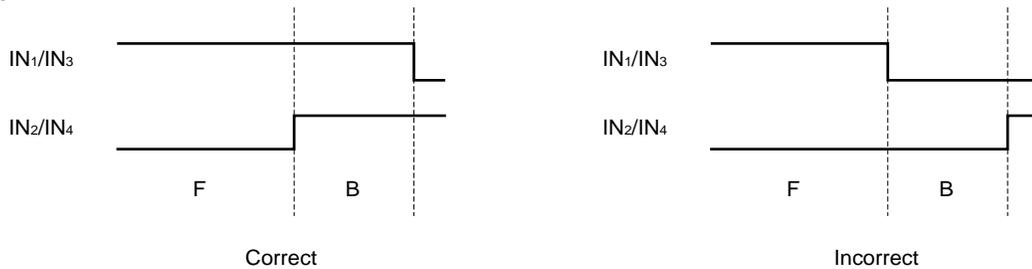
Outer circumference seek



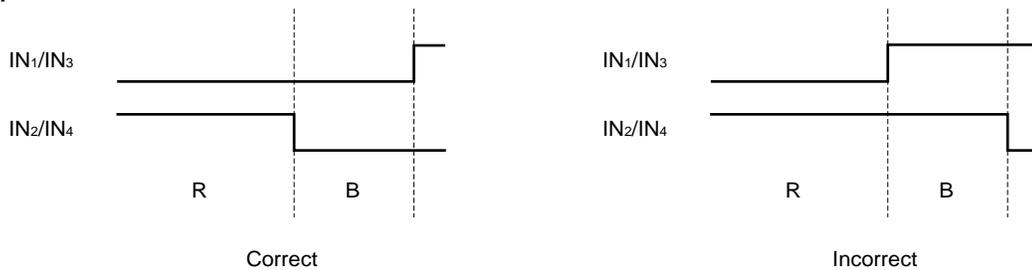
• Input signal wave when SEL = LOW (Brake mode)

To set the H bridge in the Brake mode (refer to **FUNCTION TABLE**), use input signals that set the Brake mode from IN₂ (IN₄).

Example 1 From Forward to Brake



Example 2 From Reverse to Brake



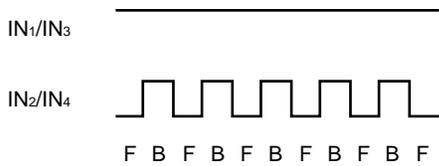
Remark This is because noise may be output due to the configuration of the internal circuit.

NOTES ON PWM DRIVING CONTROL

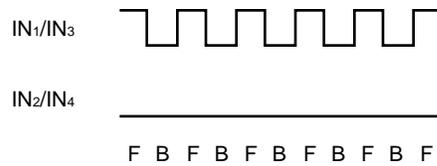
Keep in mind the following points when executing PWM.

- Be sure to input the signals to control PWM driving from IN₂ and IN₄.
- Because the logic of the PWM driving control inputs (IN₂ and IN₄) to create the Brake status is inverted depending on whether the Forward or Reverse mode is used, care must be exercised when PWM driving is controlled at a duty factor other than 50%.

Example 1 PWM driving in Forward mode

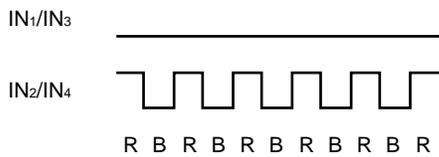


Correct

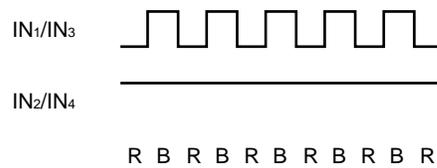


Incorrect

Example 2 PWM driving in Reverse mode



Correct

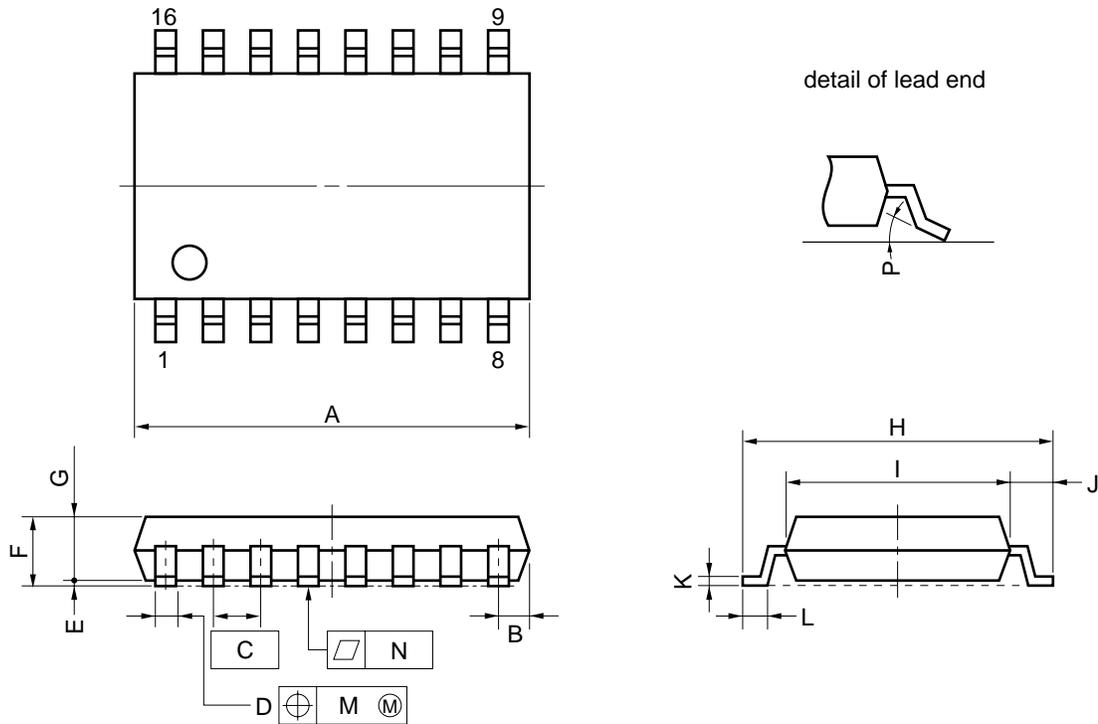


Incorrect

Remark This is because noise may be output due to the configuration of the internal circuit.

PACKAGE DIMENSION

16 PIN PLASTIC SOP (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ^{+0.10} _{-0.05}	0.016 ^{+0.004} _{-0.003}
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7±0.3	0.303±0.012
I	5.6	0.220
J	1.1	0.043
K	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}
L	0.6±0.2	0.024 ^{+0.008} _{-0.009}
M	0.12	0.005
N	0.10	0.004
P	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}

P16GM-50-300B-4

RECOMMENDED SOLDERING CONDITIONS

It is recommended to solder this product under the conditions shown below.

For soldering methods and conditions other than those listed below, consult NEC.

For details of the recommended soldering conditions, refer to Information Document “**Semiconductor Device Mounting Technology Manual**” (C10535E).

Surface Mount Type

Soldering Method	Soldering Condition	Symbol of Recommended Soldering
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds MAX. (210 °C MIN.) Number of times: 2 MAX. <Precautions> (1) Start the second reflow after the device temperature rise due to the first reflow has dropped to room temperature. (2) Do not clean flux with water after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215 °C, Time: 40 seconds MAX. (200 °C MIN.) Number of times: 2 MAX. <Precautions> (1) Start the second reflow after the device temperature rise due to the first reflow has dropped to room temperature. (2) Do not clean flux with water after the first reflow.	VP15-00-2
Wave soldering	Soldering bath temperature: 260 °C MAX., Time: 10 seconds MAX., Number of times: 1 Preheating temperature: 120 °C MAX. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C MAX., Time: 3 seconds MAX. (per side of device)	–

Caution Do not use two or more soldering methods in combination (except partial heating).

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.