NEC

MOS INTEGRATED CIRCUIT

μPD168302

MONOLITHIC 2CH H-BRIDGE DRIVER

DESCRIPTION

The μPD168302 is monolithic dual H-bridge driver LSI which uses power MOS FETs in the output stages. By using the MOS process, this driver has substantially improved the voltage loss of the output stage and power consumption as compared with conventional driver using bipolar transistors.

As the package, a 24-pin plastic TSSOP is adopted to enable the creation of compact, slim application sets.

It is provided with forward/reverse and brake functions and is ideal as a driver for DC motor and stepping motor.

FEATURES

- 2ch H-Bridge circuit employing power MOS FETs
- Charge-pump circuit for low-voltage operation
- Low output FET on resistance: 1.0 Ω TYP. 2.0 Ω MAX. (Sum of upper and lower side)
- Output current: DC current 0.6 A/ch
  Peak current 1.0 A/ch
- Input logic frequency: 100 kHz
- 5 V logic power supply: Minimum operating supply voltage 4.0 V
- 0.9 to 3.6 V power supply for motor drive
- Under voltage locked out circuit: shutdown internal circuit at V_{DD} = 1.7 V TYP.
- 24-pin plastic TSSOP (5.72 mm (225), 0.5 mm pitch)

ORDERING INFORMATION

Part Number	Package
μPD168302MA-6A5	24-pin plastic TSSOP (5.72 mm (225))

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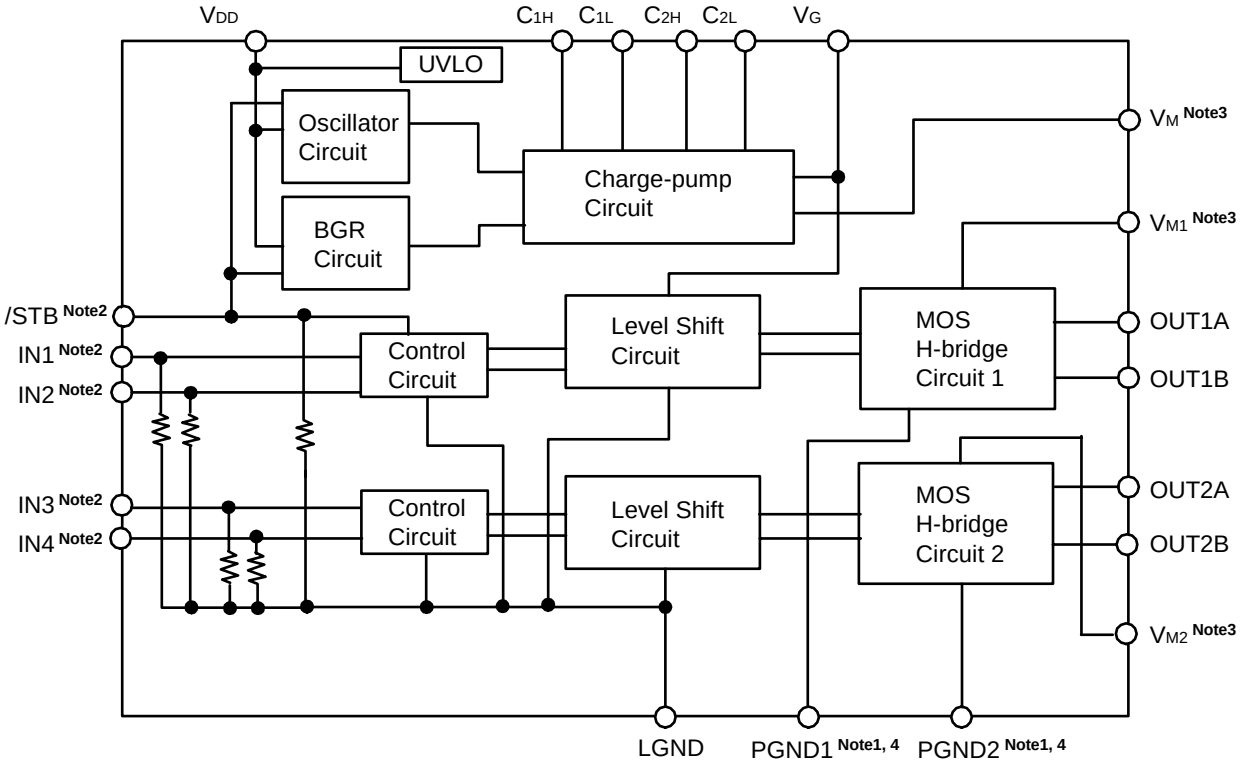
Printed in Japan

1. BLOCK DIAGRAM



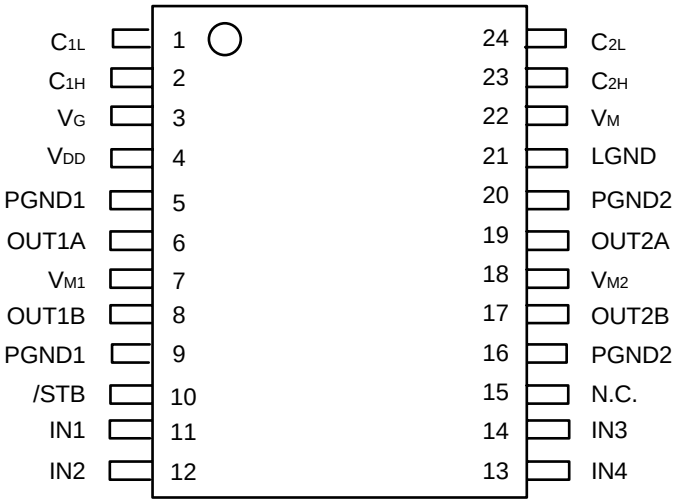
Notes 1. The terminal which has more than one should connect not only one terminal but all terminals.

2. Pull down resistance (50 to 200 kΩ) is connected to the input terminal.

3. It is recommended that V_M terminal is connected to the terminal which either V_{M1} or V_{M2} is higher.

4. It is recommended that the voltage of PGND1 and PGND2 is not lower value than GND.

2. PIN CONNECTION



3. PIN FUNCTIONS

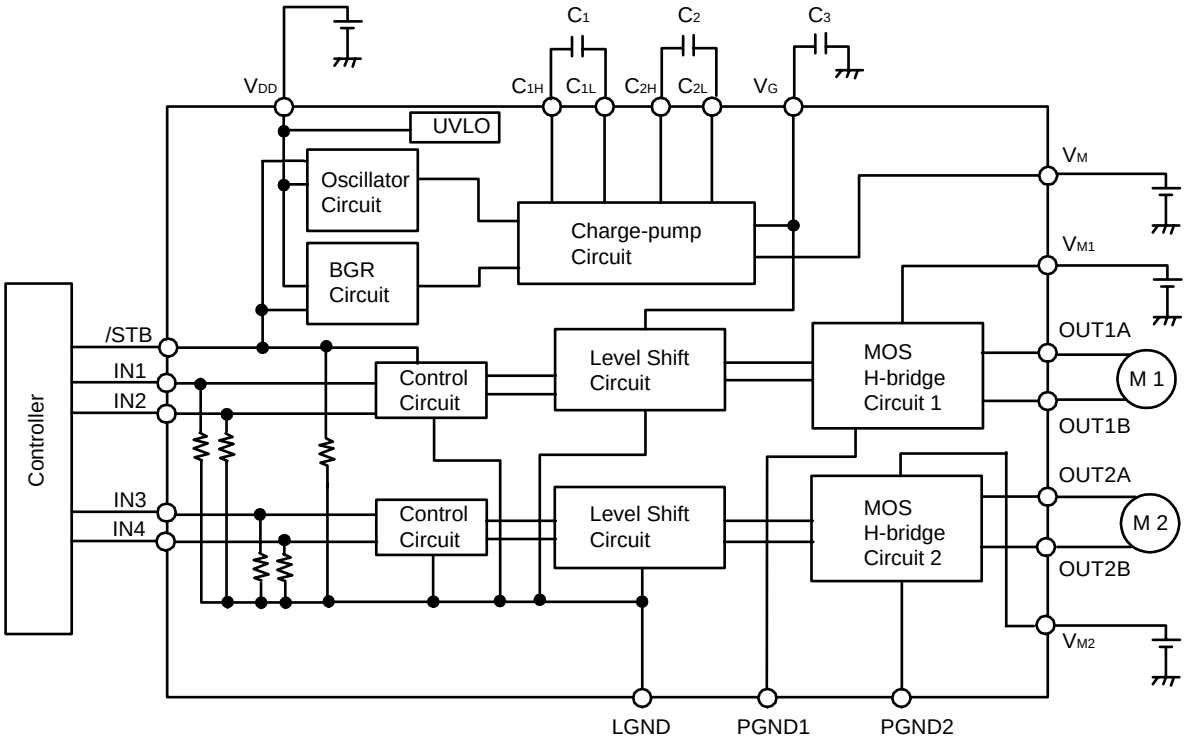
PACKAGE: 24-pin plastic TSSOP (5.72 mm (225), 0.5 mm pitch)

Pin No.	Pin Name	Pin Function
1	C_{1L}	Capacitor connect pin for charge-pump circuit
2	C_{1H}	Capacitor connect pin for charge-pump circuit
3	V_G	Gate voltage pin
4	V_{DD}	Power supply pin for logic circuit
5	PGND1	Power GND pin
6	OUT1A	Output A pin for ch1
7	V_{M1}	Power supply pin for power circuit
8	OUT1B	Output B pin for ch1
9	PGND1	Power GND pin
10	/STB	Standby pin
11	IN1	Input logic 1 pin for ch1
12	IN2	Input logic 2 pin for ch1
13	IN4	Input logic 4 pin for ch2
14	IN3	Input logic 3 pin for ch2
15	N.C.	(No connect)
16	PGND2	Power GND pin
17	OUT2B	Output B pin for ch2
18	V_{M2}	Power supply pin for power circuit
19	OUT2A	Output A pin for ch2
20	PGND2	Power GND pin
21	LGND	Logic GND pin
22	V_M	Power supply pin for power circuit
23	C_{2L}	Capacitor connect pin for charge-pump circuit
24	C_{2H}	Capacitor connect pin for charge-pump circuit

Cautions 1. The terminal which has more than one should connect not only one terminal but terminals.

2. Please recommend connecting unused pins to GND.

4. APPLICATION EXAMPLE



Remark This circuit diagram is an example of connection, and is not a thing aiming at mass production.

5. FUNCTION TABLE

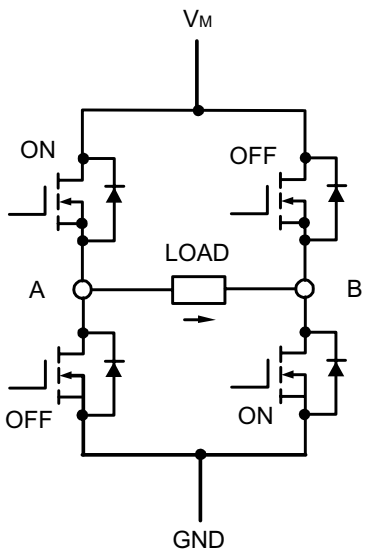
Input			Output		Current direction
IN1	IN2	/STB	OUT1A	OUT1B	
L	L	H	Hi-Z	Hi-Z	Stop
H	L	H	H	L	OUT1A→OUT1B (Forward)
L	H	H	L	H	OUT1B→OUT1A (Reverse)
H	H	H	L	L	Brake (Regeneration mode)
x	x	L	Hi-Z	Hi-Z	All output stop mode (Standby)

Input			Output		Current direction
IN3	IN4	/STB	OUT2A	OUT2B	
L	L	H	Hi-Z	Hi-Z	Stop
H	L	H	H	L	OUT1A→OUT1B (Forward)
L	H	H	L	H	OUT1B→OUT1A (Reverse)
H	H	H	L	L	Brake (Regeneration mode)
x	x	L	Hi-Z	Hi-Z	All output stop mode (Standby)

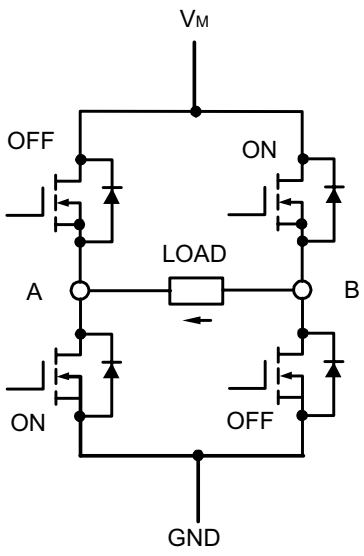
Remark H: High-level, L: Low-level, Hi-Z: High impedance

6. H-BRIDGE OPERATION FIGURE

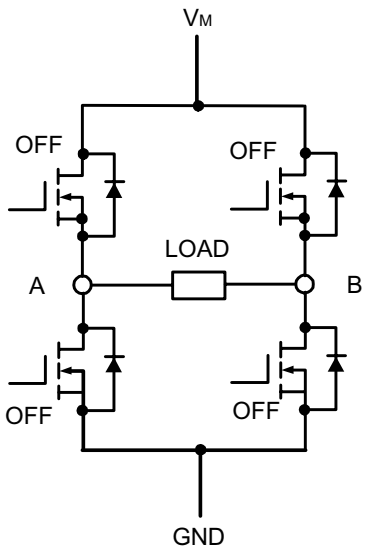
Forward



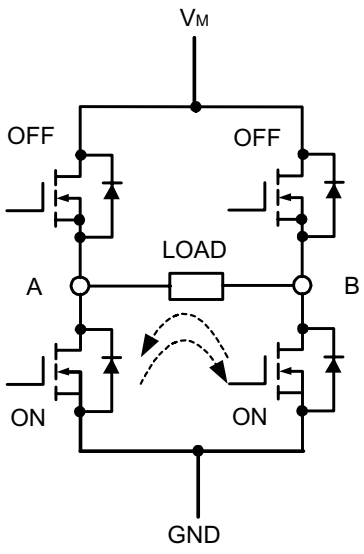
Reverse



Stop



Brake



7. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C. When mounted on a glass epoxy board (100 mm x 100 mm x 1 mm, 15% copper foil))

Parameter	Symbol	Condition	Rating	Unit
Power Supply	V_{DD}	Logic	–0.5 to +6.0	V
	V_M	Motor	–0.5 to +4.0	V
V_G Voltage	V_G		–0.5 to +8.0	V
Input Voltage	V_{IN}		–0.5 to V_{DD} + 0.5	V
Output Voltage	V_{OUT}	Motor	6.2	V
DC Output Current	$I_{D(DC)}$	DC	± 0.6	A/ch
Peak Output Current	$I_{D(pulse)}$	PW < 10 ms, Duty ≤ 20%	± 1.0	A/ch
Power consumption	P_T		0.7	W
Peak junction temperature	$T_{ch(MAX.)}$		150	°C
Storage temperature	T_{stg}		–55 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = 25°C. When mounted on a glass epoxy board (100 mm x 100 mm x 1 mm, 15% copper foil))

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power Supply	V_{DD}	Logic	4.0		5.5	V
	V_M	Motor	0.9		3.6	V
V_G Voltage **Note**	V_G		V_M + 3.5		7.5	V
Input Voltage	V_{IN}		0		V_{DD}	V
DC Output Current	$I_{D(DC)}$	DC	–0.3		+0.3	A/ch
Peak Output Current	$I_{D(pulse)}$	PW < 10 ms, Duty ≤ 20%	–0.7		+0.7	A/ch
Logic input frequency	f_{IN}				100	kHz
Capacitor for charge-pump	C_1 to C_3		0.008	0.01	0.012	μF
Operating temperature	T_A		0		70	°C

Note When using charge-pump circuit, the voltage occurs internally at V_G-pin (V_M + 3.5 V (TYP.)).

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, T_A = 25°C, V_{DD} = 5 V, V_M = 5.5 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
V_{DD} current at standby	$I_{DD(STB)}$	/STB = L			1.0	μA
V_{DD} current at operating	$I_{DD(ACT)}$				1.0	mA
High-level Input current	I_{IH}	$V_{IN} = V_{DD}$			100	μA
Low-level Input current	I_{IL}	V_{IN} = 0 V	–1.0			μA
Input pull-down resistance	R_{IND}		50		200	kΩ
High-level Input voltage	V_{IH}	4.0 V ≤ V_{DD} ≤ 5.5 V	0.7 x V_{DD}			V
Low-level Input voltage	V_{IL}	4.0 V ≤ V_{DD} ≤ 5.5 V			0.3 x V_{DD}	V
On resistance H-Bridge	R_{on}	I_M = 0.3 A, Sum of upper and lower		1.0	2.0	Ω
Output Leak current	$I_{M(off)}$	Per V_M pin All control-pin = L (V_M = Recommenred range MAX.)			1.0	μA
low-voltage detected voltage	V_{DDS}			1.7	2.5	V
turn-ON time at charge-pump	t_{ONC}	$C_1 = C_2 = C_3$ = 0.01 μF			1.0	ms
Output turn-ON time	t_{on}	I_M = 0.3 A, refer to Figure 1, 2	0.1		5.0	μs
Output turn-OFF time	t_{off}		0.1		5.0	μs

Figure 1. Charge-pump circuit operating wave

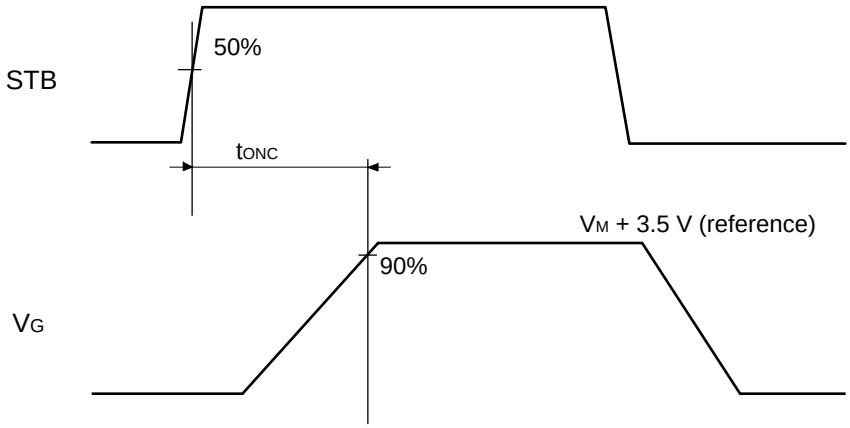
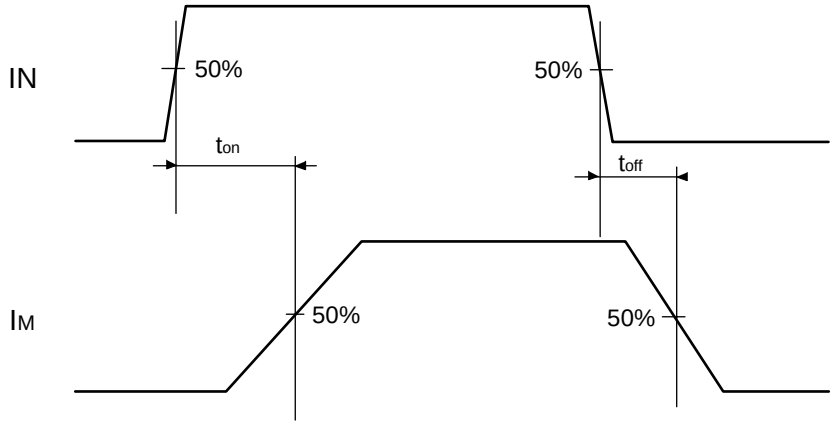
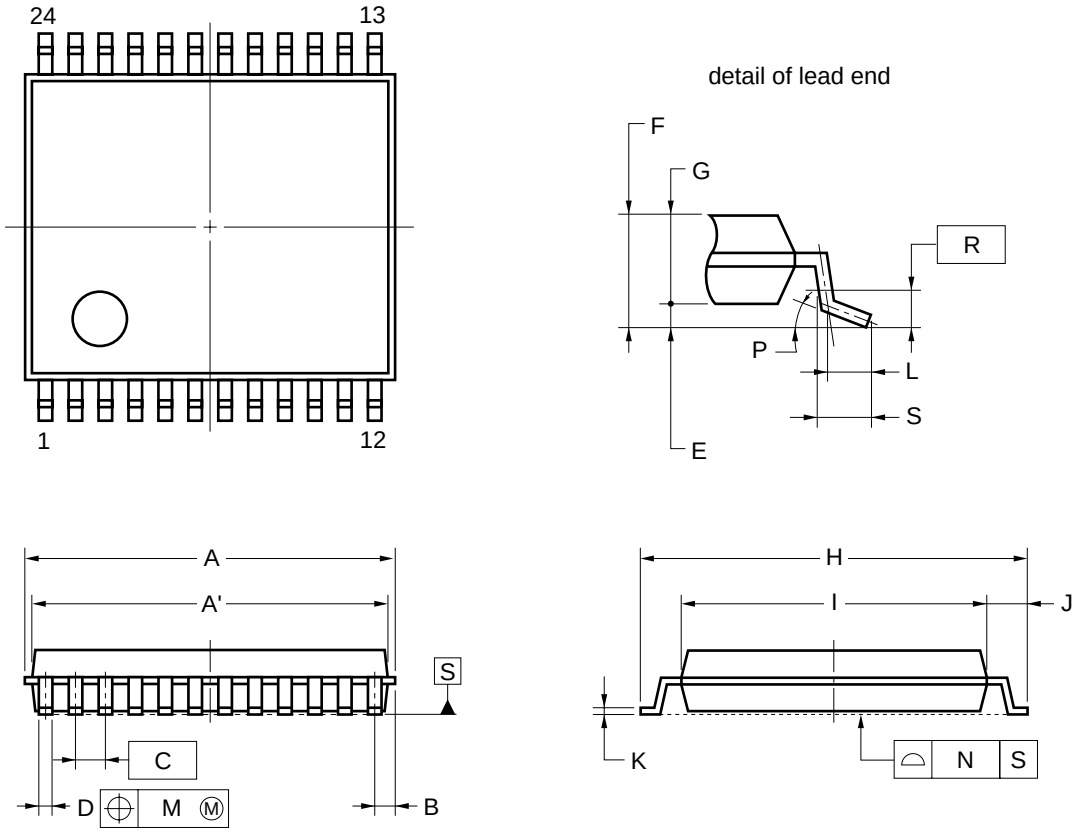


Figure 2. Switching Wave



8. PACKAGE DRAWING

24-PIN PLASTIC TSSOP (5.72 mm (225))



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	6.65±0.10
A'	6.5±0.1
B	0.575
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
H	6.4±0.1
I	4.4±0.1
J	1.0±0.1
K	0.17±0.025
L	0.5
M	0.10
N	0.08
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.6±0.15

P24MA-50-6A5

9. RECOMMENDED SOLDERING CONDITIONS

The μPD168302 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

μPD168302MA-6A5: 24-pin plastic TSSOP (5.72 mm (225))

Soldering Method	Soldering Conditions	Recommended Condition symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds MAX. (at 220°C or higher), Count: Three times or less, Exposure limit: None, Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended	IR60-00-3

Caution Do not use different soldering methods together (except for partial heating).

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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