NEC

MOS INTEGRATED CIRCUIT

μPD16835

MONOLITHIC QUAD H BRIDGE DRIVER CIRCUIT

The μPD16835 is a monolithic quad H bridge driver IC that employs a CMOS control circuit and a MOS FET output circuit. Because it uses MOS FETs in its output stage, this driver IC consumes less power than conventional driver ICs that use bipolar transistors.

Because the μPD16835 controls a motor by inputting serial data, its package has been shrunk and the number of pins reduced. As a result, the performance of the application set can be improved and the size of the set has been reduced.

This IC employs a current-controlled 64-step micro step driving method that drives stepper motor with low vibration.

The μPD16835 is housed in a 38-pin shrink SOP to contribute to the miniaturization of the application set.

This IC can simultaneously drive two stepper motors and is ideal for the mechanisms of camcorders.

FEATURES

- Four H bridge circuits employing power MOS FETs
- Current-controlled 64-step micro step driving
- Motor control by serial data (8 bytes × 8 bits) (original oscillation: 4-MHz input)
  Data is input with the LSB first.
  EVR reference setting voltage: 100 to 250 mV (@V_{REF} = 250 mV) ... 4-bit data input (10-mV step)
  Chopping frequency: 32 to 124 kHz ... 5-bit data input (4-kHz step)
  Original oscillation division or internal oscillation selectable
  Number of pulses in 1 V_D: 0 to 252 pulses ... 6 bits + 2-bit data input (4 pulses/step)
  Step cycle: 0.25 to 8,191.75 μs ... 15-bit data input (0.25-μs step)
- 3-V power supply. Minimum operating voltage: 2.7 V (MIN.)
- Low current consumption I_{DD}: 3 mA (MAX.), $I_{DD\ (reset)}$: 100 μA (MAX.), I_{MO}: 1 μA (MAX.)
- 38-pin shrink SOP (300 mil)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		-0.5 to +6.0	V
	V_M		-0.5 to +11.2	V
Input voltage	V_{IN}		-0.5 to V_{DD} + 0.5	V
Reference voltage	V_{REF}		500	mV
H bridge drive current**Note 1**	$I_{M\ (DC)}$	DC	±150	mA/phase
Instantaneous H bridge drive current**Note 1**	$I_{M\ (pulse)}$	PW ≤ 10 ms, Duty ≤ 5%	±300	mA/phase
Power consumption**Note 2**	P_T		1.0	W
Peak junction temperature	$T_{CH\ (MAX)}$		150	°C
Storage temperature	T_{stg}		-55 to +150	°C

Notes 1. Permissible current per phase with the IC mounted on a PCB.

2. When the IC is mounted on a glass epoxy PCB (10 cm × 10 cm × 1 mm).

The information in this document is subject to change without notice.

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RECOMMENDED OPERATING RANGE

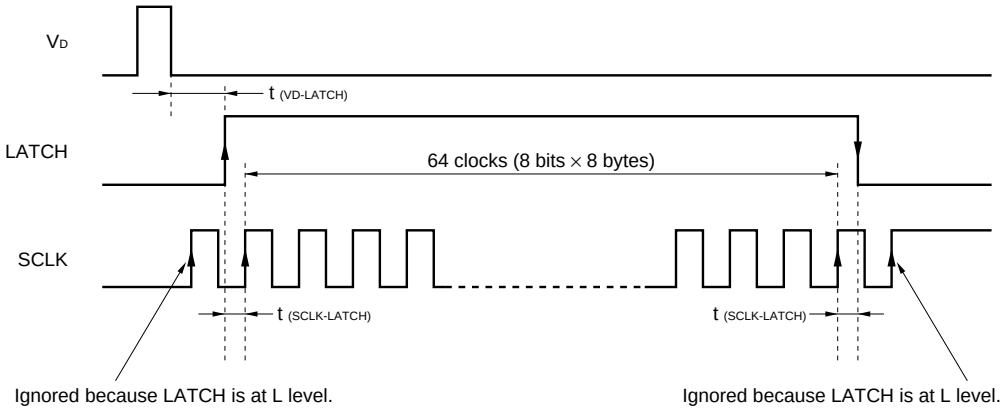
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	2.7		5.5	V
	V_M	4.8		11	V
Input voltage	V_{IN}	0		V_{DD}	V
Reference voltage	V_{REF}	225	250	275	mV
EXP pin input voltage	V_{EXPIN}			V_{DD}	V
EXP pin input current	I_{EXPIN}			100	μA
H bridge drive current	$I_{M\ (DC)}$	-100		+100	mA
H bridge drive current	$I_{M\ (pulse)}$ **Note 1**	-200		+200	mA
Clock frequency (OSC_{IN})	f_{CLK} **Note 2**	3.9	4	4.2	MHz
Clock frequency amplitude	V_{fCLK} **Note 2**	$0.7V_{DD}$		V_{DD}	V
Serial clock frequency (SCLK)	f_{SCLK}			5.0	MHz
Video sync signal width	$PW_{(VD)}$ **Note 3**	250			ns
LATCH signal wait time	$t_{(VD\text{-}LATCH)}$ **Note 4**	400			ns
SCLK wait time	$t_{(SCLK\text{-}LATCH)}$ **Note 4**	400			ns
SDATA setup time	t_{setup} **Note 4**	80			ns
SDATA hold time	t_{hold} **Note 4**	80			ns
Chopping frequency	f_{osc} **Note 3**	32		124	kHz
Reset signal pulse width	f_{RST}	100			μs
Operating temperature	T_A	-10		+70	°C
Peak junction temperature	$T_{CH\ (MAX)}$			125	°C

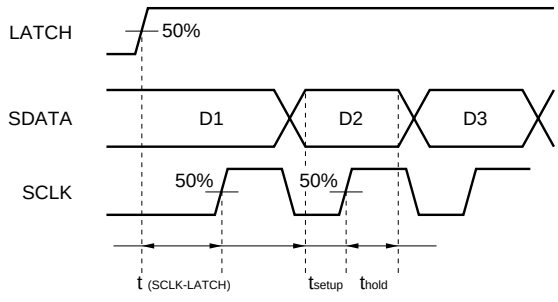
Notes 1. PW ≤ 10 ms, duty ≤ 5%

2. C_{OSC} = 33 pF, V_{REF} = 250 mV

3. f_{CLK} = 4 MHz

4. Serial data delay (see the figure below.)





ELECTRICAL CHARACTERISTICS

DC Characteristics (Unless otherwise specified, V_{DD} = 3.3 V, V_M = 6.0 V, V_{REF} = 250 mV, T_A = 25°C, f_{CLK} = 4 MHz, C_{OSC} = 33 pF, C_{FIL} = 1,000 pF, EVR = 100 mV (0000))

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Off V_M pin current	$I_{MO\ (RESET)}$	No load, reset period			1.0	μA
V_{DD} pin current	I_{DD}	Output open			3.0	mA
V_{DD} pin current	$I_{DD\ (RESET)}$	Reset period			100	μA
High-level input voltage	V_{IH}	LATCH, SCLK, SDATA, V_D, RESET, OSC_{IN}	0.7*V_{DD}			V
Low-level input voltage	V_{IL}				0.3*V_{DD}	V
Input hysteresis voltage	V_H			300		mV
Monitor output voltage 1 (EXTOUT α, β)	$V_{OM\alpha\ (H)}$, $V_{OM\beta\ (H)}$	5th byte	0.9*V_{DD}			V
	$V_{OM\alpha\ (L)}$, $V_{OM\beta\ (L)}$	5th byte			0.1*V_{DD}	V
Monitor output voltage 2 (EXP 0 to 4: open drain)	$V_{OEXP\ (H)}$	Pull up (V_{DD})			V_{DD}	V
	$V_{OEXP\ (L)}$	I_{OEXP} = 100 μA			0.1*V_{DD}	V
High-level input current	I_{IH}	V_{IN} = V_{DD}			0.06	mA
Low-level input current	I_{IL}	V_{IN} = 0	-1.0			μA
Reset pin high-level input current	$I_{IH\ (RST)}$	V_{RST} = V_{DD}			1.0	μA
Reset pin low-level input current	$I_{IL\ (RST)}$	V_{RST} = 0	-1.0			μA
Input pull-down resistor	R_{IND}	LATCH, SCLK, SDATA, V_D	50		200	kΩ
H bridge ON resistance**Note 1**	R_{ON}	I_M = 100 mA		3.5	5.0	Ω
Chopping frequency (internal oscillation: C_{OSC} = 100 pF)	$f_{OSC\ (1)}$	DATA: 00000 (4th byte)		0		kHz
	$f_{OSC\ (2)}$	DATA: 11111 (4th byte)	100	124	150	
Step frequency	f_{STEP}	Minimum step		4		kHz
V_D delay**Note 2**	Δt_{VD}				250	ns
Sine wave peak output current**Note 3**	I_M	L = 25 mH/R = 100 Ω (1 kHz) EVR = 200 mV (1010) R_S = 6.8 Ω, f_{OSC} = 64 kHz		52		mA
FIL pin voltage**Note 4**	V_{EVR}	EVR = 200 mV (1010)	370	400	430	mV
FIL pin step voltage**Note 4**	$V_{EVRSTEP}$	Minimum step		20		mV

AC Characteristics (Unless otherwise specified, V_{DD} = 3.3 V, V_M = 6.0 V, T_A = 25°C, f_{CLK} = 4 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
H bridge output circuit turn on time	t_{ONH}	I_M = 100 mA**Note 5**		1.0	2.0	μs
H bridge output circuit turn off time	t_{OFFH}	I_M = 100 mA**Note 5**		1.0	2.0	μs

Notes 1. Total of ON resistance at top and bottom of output H bridge

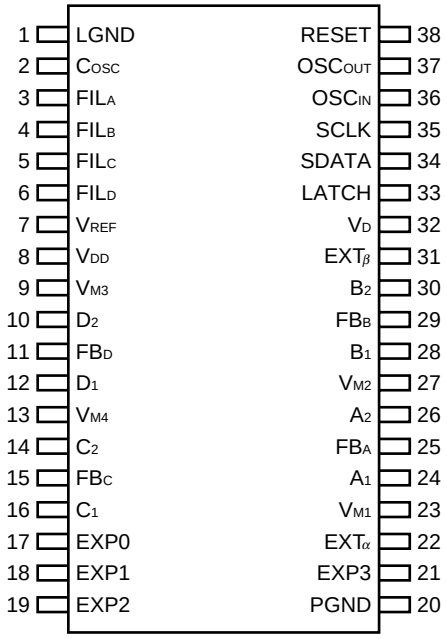
2. By OSC_{IN} and V_D sync circuit

3. FB pin is monitored.

4. FIL pin is monitored. A voltage about twice that of the EVR value is output to the FIL pin.

5. 10% to 90% of the pulse peak value without filter capacitor (C_{FIL})

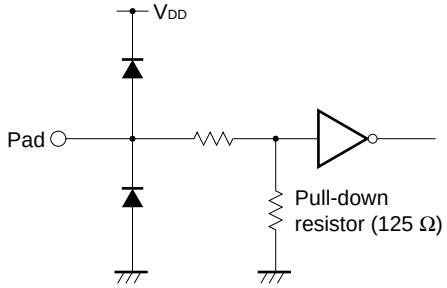
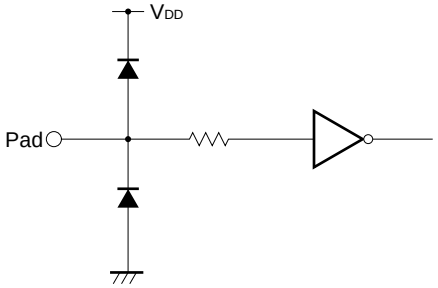
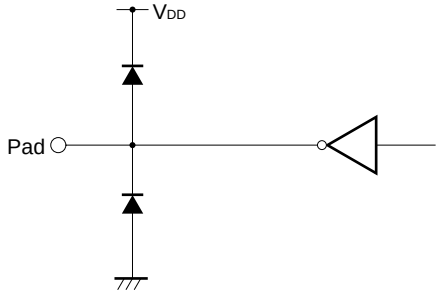
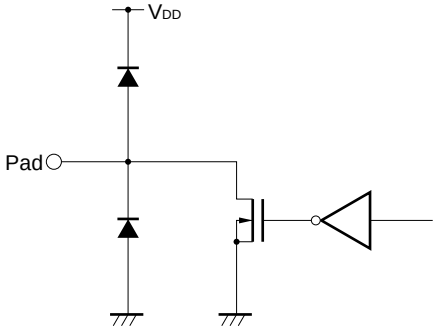
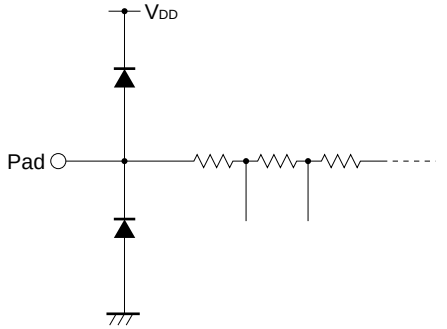
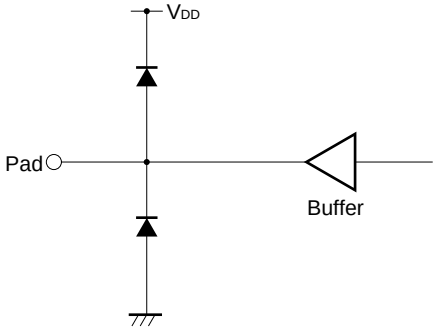
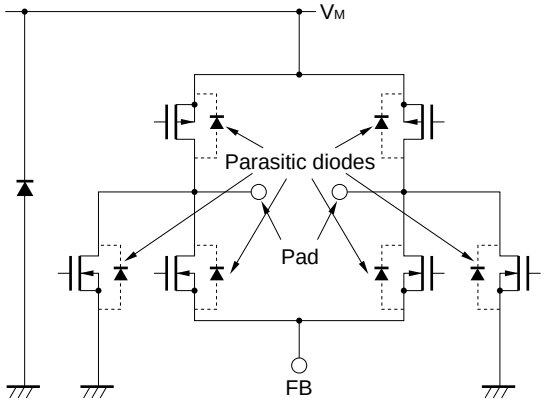
PIN CONFIGURATION



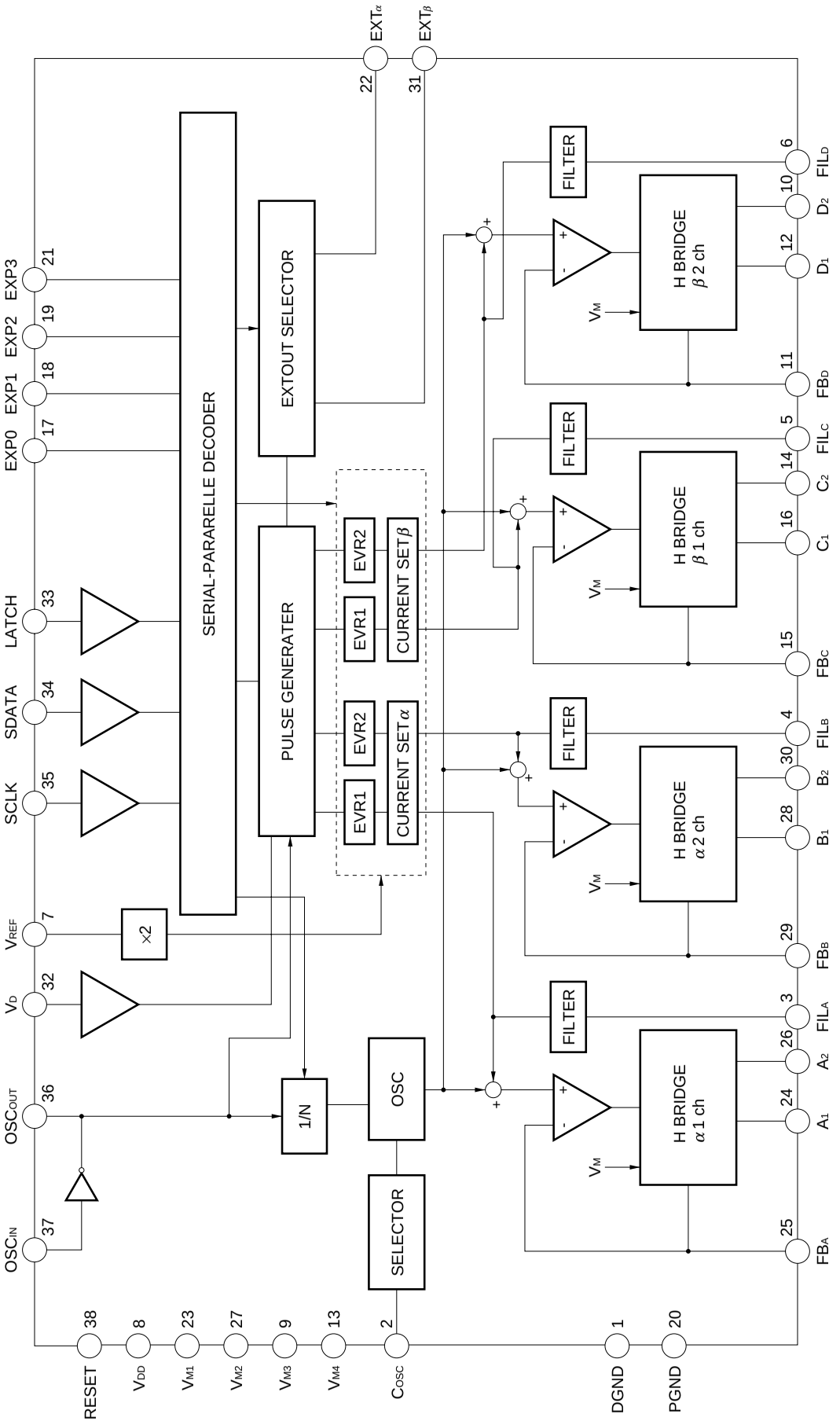
PIN FUNCTION

No.	Name	Function
1	LGND	Control circuit GND pin
2	C_{OSC}	Chopping capacitor connection pin
3	FIL_A	α 1-ch filter capacitor connection pin (1,000 pF TYP.)
4	FIL_B	α 2-ch filter capacitor connection pin (1,000 pF TYP.)
5	FIL_C	β 1-ch filter capacitor connection pin (1,000 pF TYP.)
6	FIL_D	β 2-ch filter capacitor connection pin (1,000 pF TYP.)
7	V_{REF}	Reference voltage input pin (250 mV TYP.)
8	V_{DD}	Control circuit supply voltage input pin
9	V_{M3}	Output circuit supply voltage input pin
10	D_2	β 2-ch output pin
11	FB_D	β 2-ch sense resistor connection pin
12	D_1	β 2-ch output pin
13	V_{M4}	Output circuit supply voltage connection pin
14	C_2	β 1-ch output pin
15	FB_C	β 1-ch sense resistor connection pin
16	C_1	β 1-ch output pin
17	EXP0	Output monitor pin (open-drain)
18	EXP1	Output monitor pin (open-drain)
19	EXP2	Output monitor pin (open-drain)
20	PGND	Power circuit GND pin
21	EXP3	Output monitor pin (open-drain)
22	EXT_α	Logic circuit monitor pin
23	V_{M1}	Output circuit supply voltage input pin
24	A_1	α 1-ch output pin
25	FB_A	α 1-ch sense resistor connection pin
26	A_2	α 1-ch output pin
27	V_{M2}	Output circuit supply voltage input pin
28	B_1	α 2-ch output pin
29	FB_B	α 2-ch sense resistor connection pin
30	B_2	α 2-ch output pin
31	EXT_β	Logic circuit monitor pin
32	V_D	Video sync signal input pin
33	LATCH	Latch signal input pin
34	SDATA	Serial data input pin
35	SCLK	Serial clock input pin
36	OSC_{IN}	Original oscillation input pin (4 MHz TYP.)
37	OSC_{OUT}	Original oscillation output pin
38	RESET	Reset signal output pin

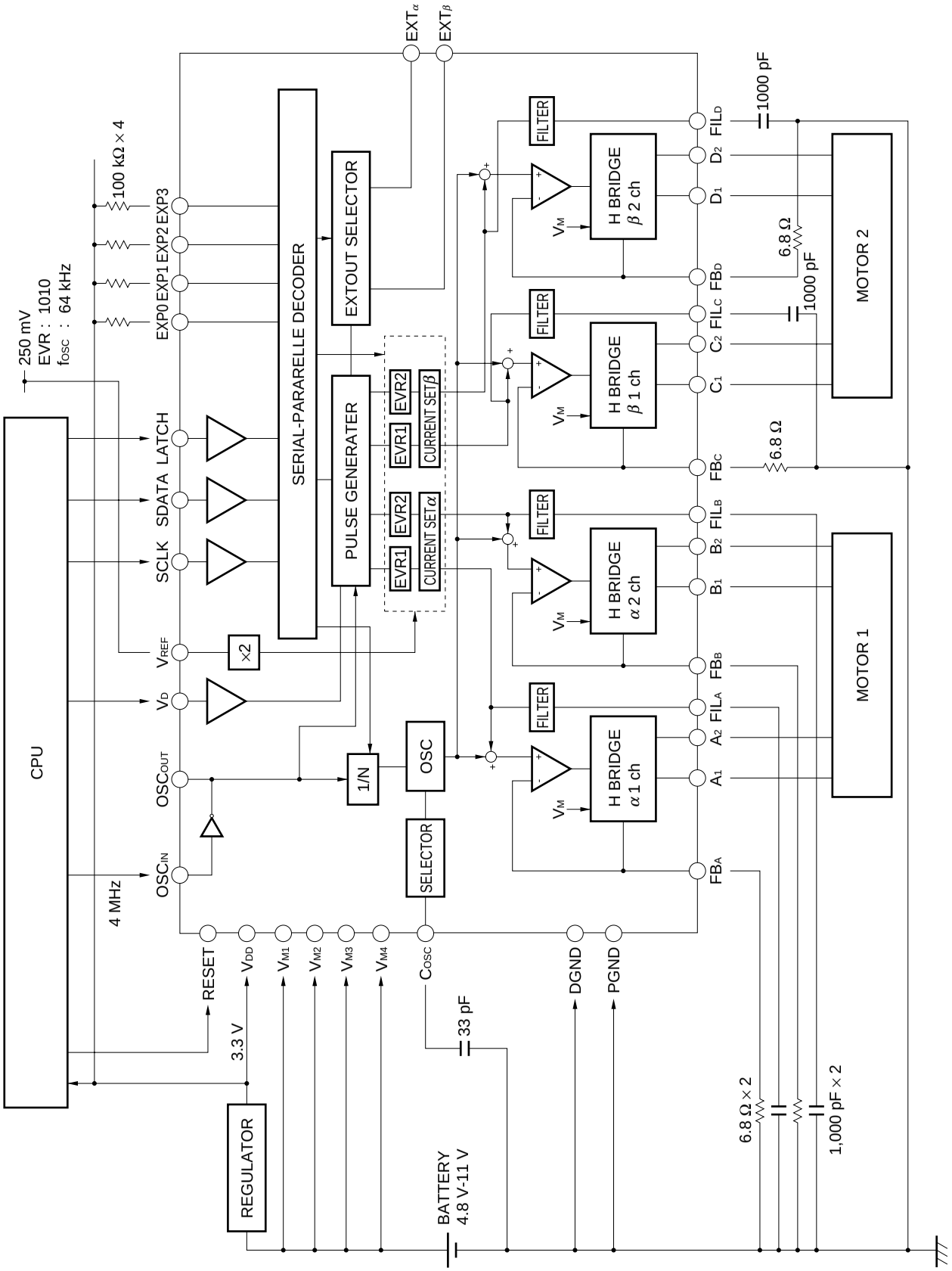
I/O PIN EQUIVALENT CIRCUIT

Pin name	Equivalent circuit	Pin name	Equivalent circuit
V_{DD} LATCH SDATA SCLK		OSC_{IN} RESET	
OSC_{OUT} EXT_{α} EXT_{β}		EXP0 EXP1 EXP2 EXP3	
V_{REF}		FIL_A FIL_B FIL_C FIL_D	
A_1, A_2 B_1, B_2 C_1, C_2 D_1, D_2			

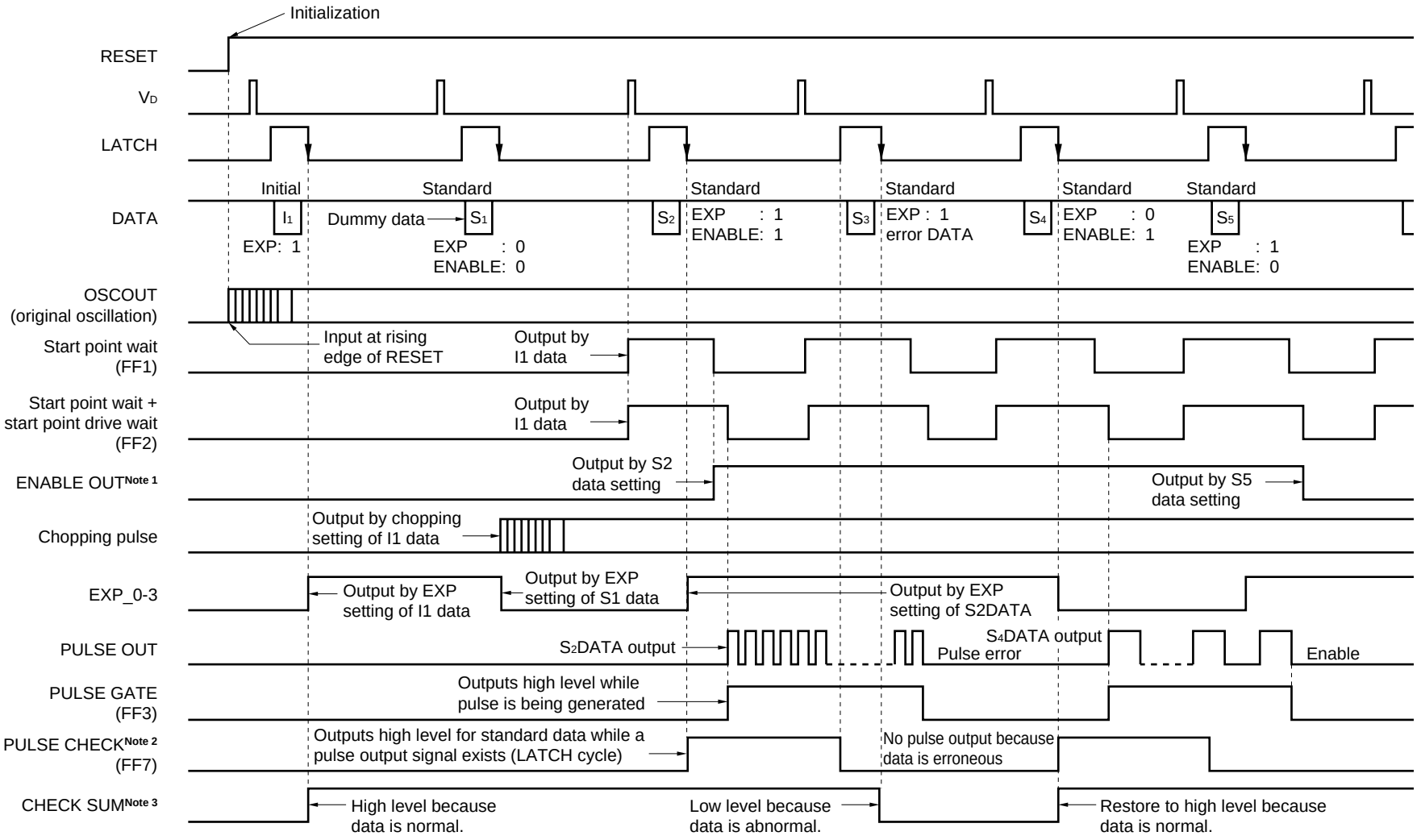
BLOCK DIAGRAM



EXAMPLE OF STANDARD CONNECTION



TIMING CHART (1)

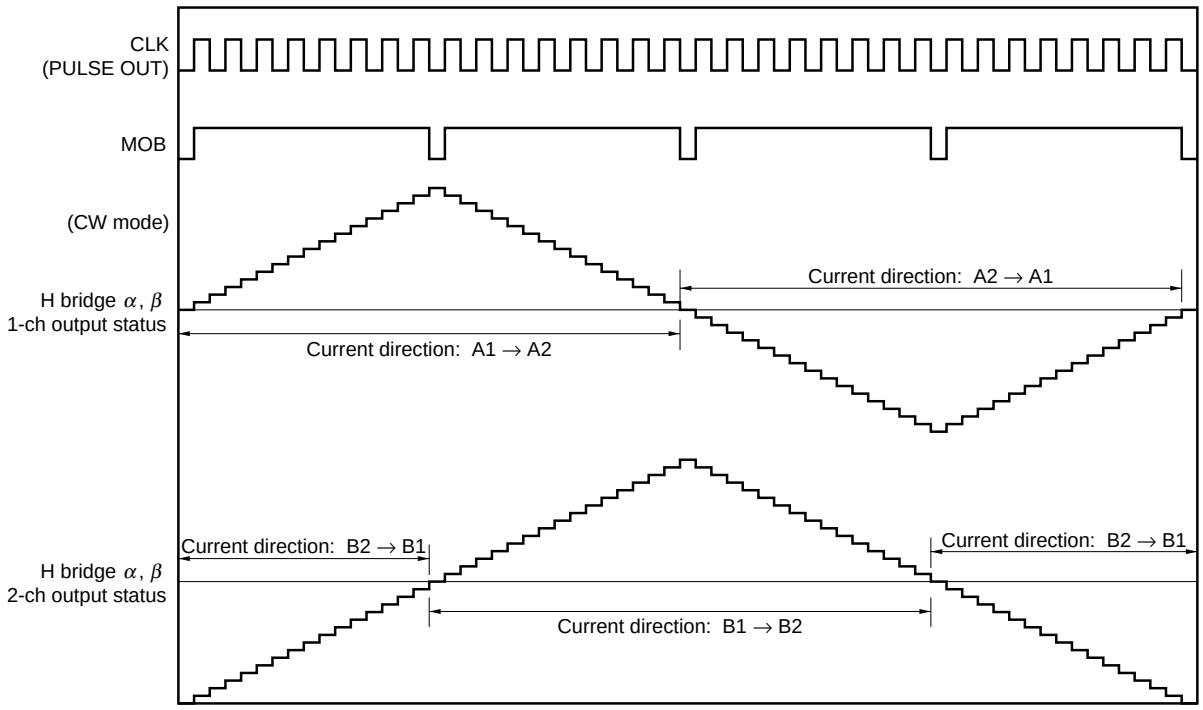


Notes 1. ENABLE is set at the falling edge of FF1 when the level changes from low to high, and at the falling edge of FF2 when the level changes from high to low.

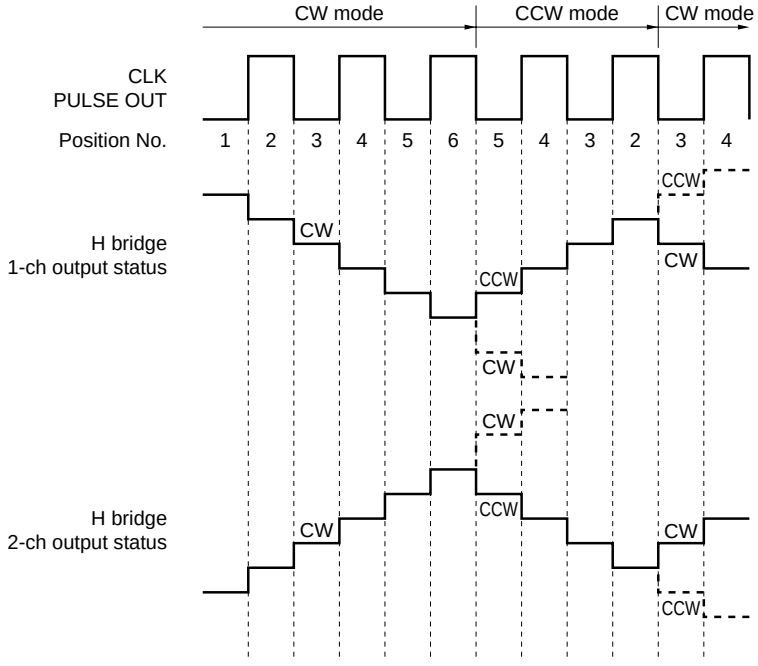
2. FF7 is an output signal that is used to check for the presence or absence of a pulse in the standard data, is updated at the falling edge of LATCH and reset once at the rising edge of LATCH. If CHECK SUM is other than "00h", FF7 goes low, inhibiting pulse output, even if a pulse is generated.

3. CHECK SUM output is updated at the falling edge of LATCH.

TIMING CHART (2)



(Expanded view)



Note In CW mode : Position No. is incremented.
In CCW mode : Position No. is decremented.

Remarks 1. The current value of the actual wave is approximated to the value shown on the next page.

2. The C_1, C_2, D_1, and D_2 pins of β channel correspond to the A_1, A_2, B_1, and B_2 pins of α channel.

3. The CW mode is set if the D7 bit of the second and fifth bytes of the standard data is “0”.

4. The CCW mode is set if the D7 bit of the second and fifth bytes of the standard data is “1”.

RELATION BETWEEN ROTATION ANGLE, PHASE CURRENT, AND VECTOR QUANTITY (64-DIVISION MICRO STEP)

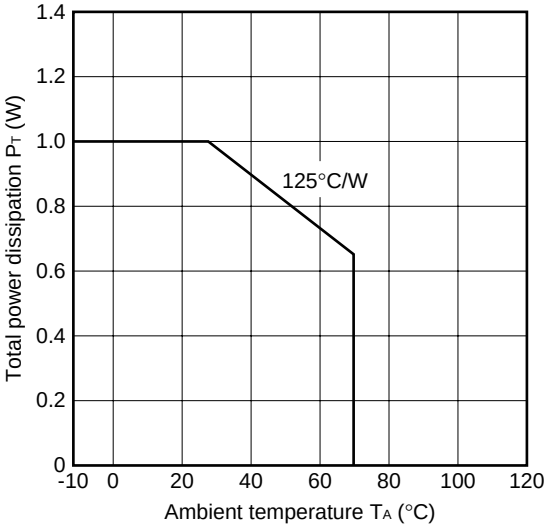
(Values of μPD16835 for reference)

Step	Rotation angle (θ)	A phase current			B phase current			Vector quantity
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	TYP.
θ0	0	-	0	-	-	100	-	100
θ1	5.6	2.5	9.8	17.0	-	100	-	100.48
θ2	11.3	12.4	19.5	26.5	93.2	98.1	103	100
θ3	16.9	22.1	29.1	36.1	90.7	95.7	100.7	100.02
θ4	22.5	31.3	38.3	45.3	87.4	92.4	97.4	100.02
θ5	28.1	40.1	47.1	54.1	83.2	88.2	93.2	99.99
θ6	33.8	48.6	55.6	62.6	78.1	83.1	88.1	99.98
θ7	39.4	58.4	63.4	68.4	72.3	77.3	82.3	99.97
θ8	45	65.7	70.7	75.7	65.7	70.7	75.7	99.98
θ9	50.6	72.3	77.3	82.3	58.4	63.4	68.4	99.97
θ10	56.3	78.1	83.1	88.1	48.6	55.6	62.6	99.98
θ11	61.9	83.2	88.2	93.2	40.1	47.1	54.1	99.99
θ12	67.5	87.4	92.4	97.4	31.3	38.3	45.3	100.02
θ13	73.1	90.7	95.7	100.7	22.1	29.1	36.1	100.02
θ14	78.8	93.2	98.1	103	12.4	19.5	26.5	100
θ15	84.4	-	100	-	2.5	9.8	17.0	100.48
θ16	90	-	100	-	-	0	-	100

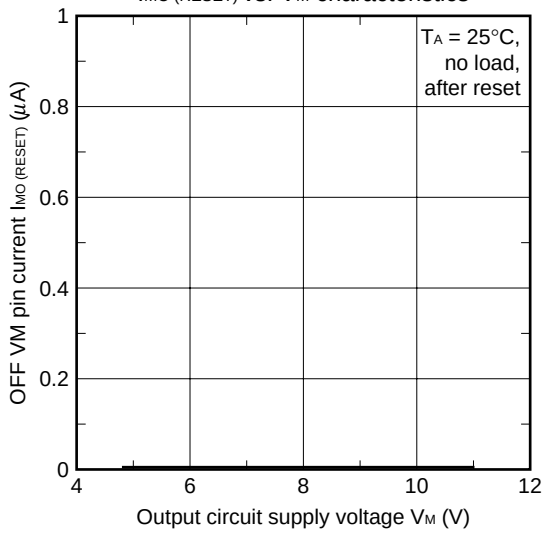
Remark These data do not indicate guaranteed values.

STANDARD CHARACTERISTIC CURVES

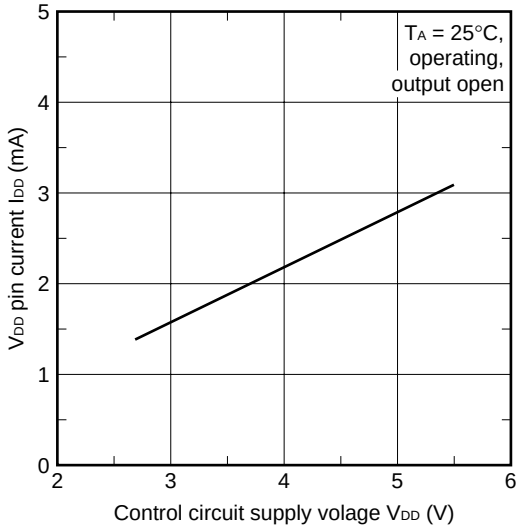
P_T vs. T_A characteristics



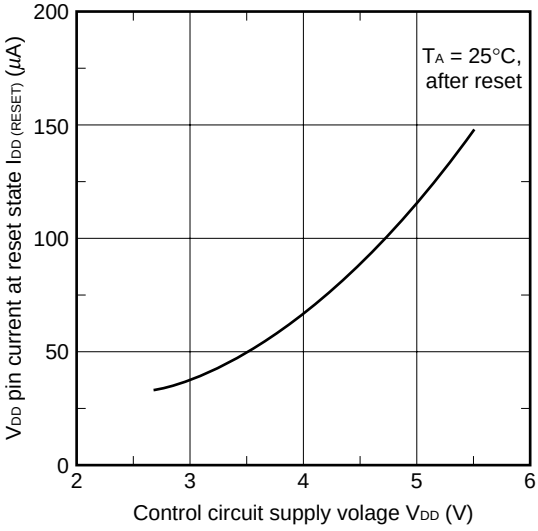
$I_{MO\ (RESET)}$ vs. V_M characteristics



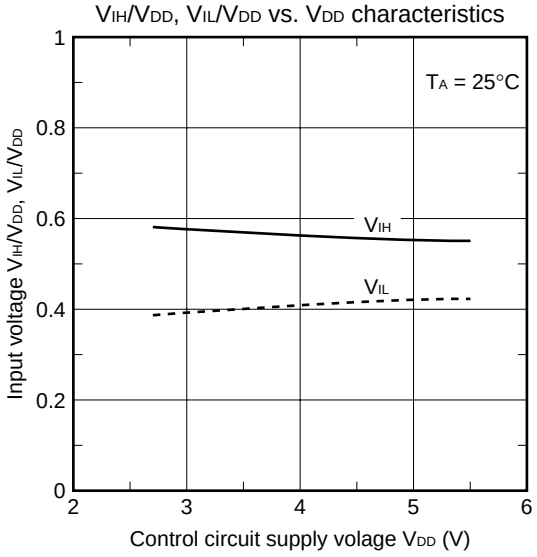
I_{DD} vs. V_{DD} characteristics



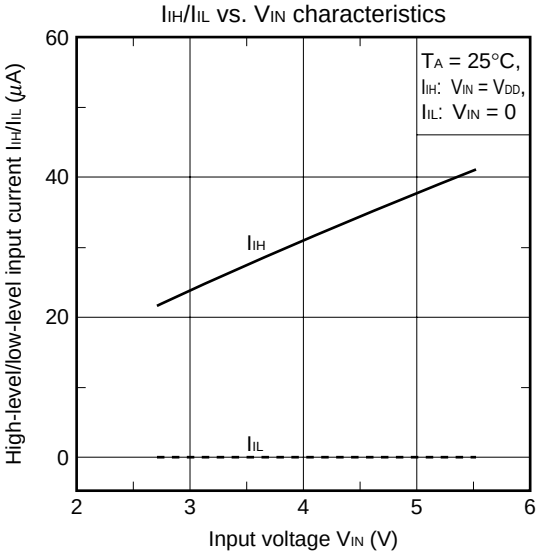
$I_{DD\ (RESET)}$ vs. V_{DD} characteristics



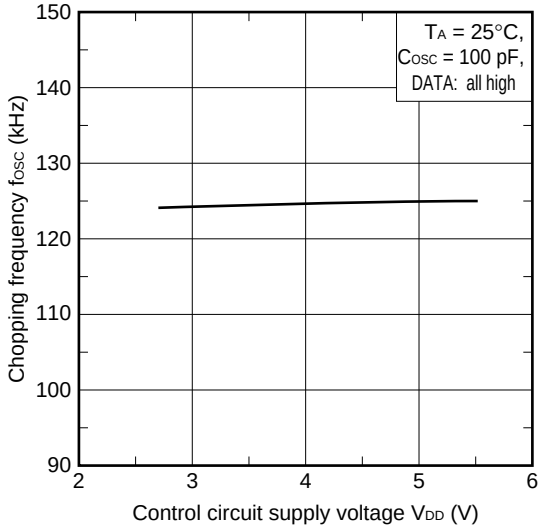
V_{IH}/V_{DD}, V_{IL}/V_{DD} vs. V_{DD} characteristics



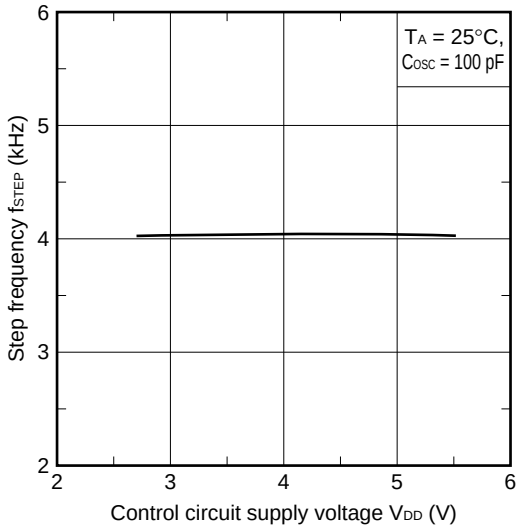
I_{IH}/I_{IL} vs. V_{IN} characteristics



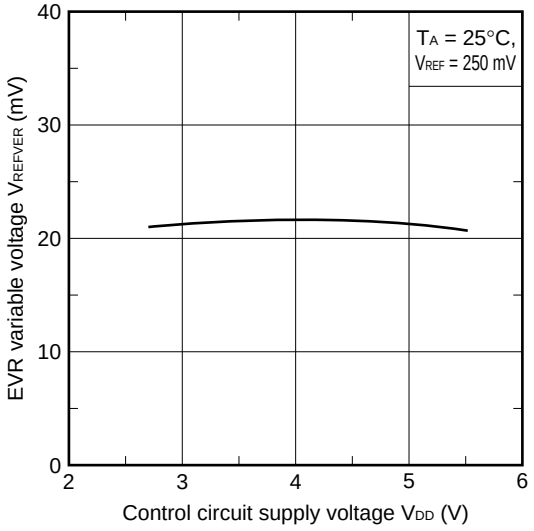
fOSC vs. VDD characteristics



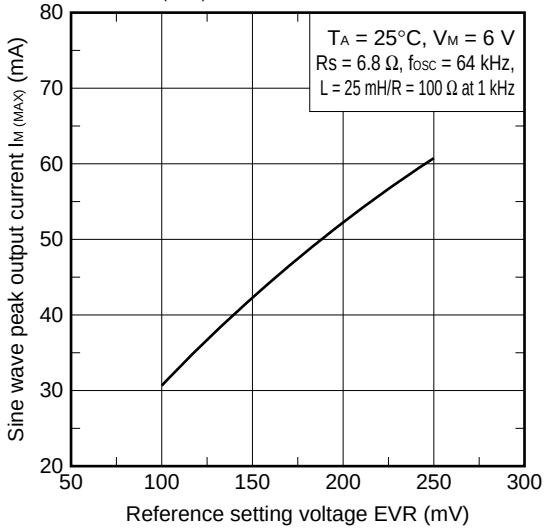
fSTEP vs. VDD characteristics



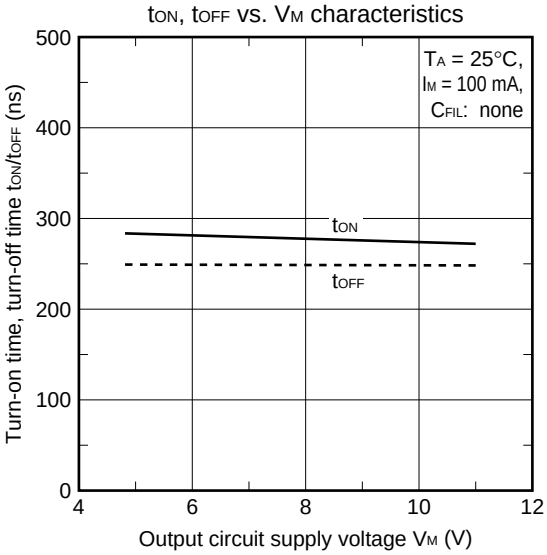
VREFVER vs. VDD characteristics



IM (MAX) vs. EVR characteristics



tON, tOFF vs. VM characteristics



I/F CIRCUIT DATA CONFIGURATION (f_{CLK} = 4-MHz EXTERNAL CLOCK INPUT)

Input data consists of serial data (8 bytes × 8 bits).
Input serial data with the LSB first, from the first byte to eighth byte.

(1) Initial data

<1st byte>

Bit	Data	Function	Setting
D7	1	HEADER DATA2	DATA selection
D6	1	HEADER DATA1	
D5	1	HEADER DATA0	
D4	0	-	-
D3	1 or 0	EXP_3	Z or L
D2	1 or 0	EXP_2	Z or L
D1	1 or 0	EXP_1	Z or L
D0	1 or 0	EXP_0	Z or L

Z: High impedance, L: Low level (current sink)

<2nd byte>

Bit	Data	Function	Setting
D7	8-bit data input[Note]	First Point Wait	Start point wait 256 μs to 65.28 ms Setting (1 to 255) Δt = 256 μs
D6			
D5			
D4			
D3			
D2			
D1			
D0			

Note Input other than “0”.

<3rd byte>

Bit	Data	Function	Setting
D7	8-bit data input[Note]	First Point Magnetize Wait	Start point drive wait 256 μs to 65.28 ms Setting (1 to 255) Δt = 256 μs
D6			
D5			
D4			
D3			
D2			
D1			
D0			

Note Input other than “0”.

(2) Standard data

<1st byte>

Bit	Data	Function	Setting
D7	0	HEADER DATA2	DATA selection
D6	0	HEADER DATA1	
D5	0	HEADER DATA0	
D4	0	-	-
D3	1 or 0	EXP_3	Z or L
D2	1 or 0	EXP_2	Z or L
D1	1 or 0	EXP_1	Z or L
D0	1 or 0	EXP_0	Z or L

Z: High impedance, L: Low level (current sink)

<2nd byte>

Bit	Data	Function	Setting
D7	1 or 0	α ROTATION	α ch CCW/CW
D6	1 or 0	α ENABLE	α ch ON/OFF
D5	6-bit data input	α Pulse Number	α ch Number of pulses in 1 V Setting (0 to 63) Δn = 4 pulses[Note]
D4			
D3			
D2			
D1			
D0			

Note The number of pulses can be varied in 4-pulse steps.

<3rd byte>

Bit	Data	Function	Setting
D7	15-bit data Low-order 8-bit data input	α Pulse Width	α ch pulse cycle 0.25 to 8,191.75 μs Setting (1 to 32,767) Δt = 0.25 μs
D6			
D5			
D4			
D3			
D2			
D1			
D0			

<4th byte>

Bit	Data	Function	Setting
D7	1 or 0	OSCSEL	Internal/external
D6	0	-	-
D5	0	-	-
D4	5-bit data input	Chopping Frequency	Chopping frequency: 32 to 124 kHz Setting (8 to 31)Note Δf = 4 kHz
D3			
D2			
D1			
D0			

Note The frequency is 0 kHz if 0 to 7 is input.

<4th byte>

Bit	Data	Function	Setting
D7	1 or 0	Current Set α	set2/set1
D6	15-bit data High-order 8-bit data input	α Pulse Width	α ch pulse cycle: 0.25 to 8,191.75 μs Setting (1 to 32,767) Δt = 0.25 μs
D5			
D4			
D3			
D2			
D1			
D0			

<5th byte>

Bit	Data	EXT_α	EXT_β
D7	0	-	-
D6	Note 5	ENABLE α Note 1	ENABLE β Note 1
D5	Note 5	ROTATION α Note 2	ROTATION β Note 2
D4	Note 5	Pulse Out α	Pulse Out β
D3	Note 5	FF7 α	FF7 β
D2	Note 5	FF3 α	FF3 β
D1	Note 5	ChecksumNote 3	FF2 β
D0	Note 5	ChoppingNote 4	FF1 β

Notes 1. H level: Conducts, L level: Stops

2. H level: Reverse (CCW),
L level: Forward (CW)

3. H level: Normal data input,
L level: Abnormal data input

4. Not output in internal oscillation mode.

5. Select one of D0 to D6 and input "1".
If two or more of D0 to D6 are selected, they are positively ORed for output.

<5th byte>

Bit	Data	Function	Setting
D7	1 or 0	β ROTATION	β ch CCW/CW
D6	1 or 0	β ENABLE	β ch ON/OFF
D5	6-bit data input	β Pulse Number	β ch Number of pulses in 1 V Setting (1 to 63) Δn = 4 pulsesNote
D4			
D3			
D2			
D1			
D0			

Note The number of pulses can be varied in 4-pulse steps.

<6th byte>

Bit	Data	Function	Setting
D7	4-bit data input	α ch Current Set2	α ch Output current setting 2 EVR: 100 to 250 mV Setting (0 to 15)Note
D6			
D5			
D4			
D3	4-bit data input	α ch Current Set1	α ch Output current setting 1 EVR: 100 to 250 mV Setting (0 to 15)Note
D2			
D1			
D0			

Note A voltage of about double EVR is output to the FIL pin.

<6th byte>

Bit	Data	Function	Setting
D7	15-bit data Low-order 8-bit data input	β Pulse Width	β ch pulse cycle: 0.25 to 8,191.75 μs Setting (1 to 32,767) Δt = 0.25 μs
D6			
D5			
D4			
D3			
D2			
D1			
D0			

<7th byte>

Bit	Data	Function	Setting
D7	4-bit data input	β ch Current Set2	β ch Output current setting 2 EVR: 100 to 250 mV Setting (0 to 15)Note
D6			
D5			
D4			
D3	4-bit data input	β ch Current Set1	β ch Output current setting 1 EVR: 100 to 250 mV Setting (0 to 15)Note
D2			
D1			
D0			

Note A voltage of about double EVR is output to the FIL pin.

<7th byte>

Bit	Data	Function	Setting
D7	1 or 0	Current Set β	set2/set1
D6	15-bit data High-order 7-bit data input	β Pulse Width	β ch pulse cycle: 0.25 to 8,191.75 μs Setting (1 to 32,767) Δt = 0.25 μs
D5			
D4			
D3			
D2			
D1			
D0			

<8th byte>

Bit	Data	Function	Setting
D7	1 or 0	Checksum	ChecksumNote
D6	1 or 0		
D5	1 or 0		
D4	1 or 0		
D3	1 or 0		
D2	1 or 0		
D1	1 or 0		
D0	1 or 0		

Note Data is input so that the sum of the first through the eighth bytes is 00h.

<8th byte>

Bit	Data	Function	Setting
D7	1 or 0	Checksum	ChecksumNote
D6	1 or 0		
D5	1 or 0		
D4	1 or 0		
D3	1 or 0		
D2	1 or 0		
D1	1 or 0		
D0	1 or 0		

Note Data is input so that the sum of the first through the eighth bytes is 00h.

DATA CONFIGURATION

Data can be input in either of two ways. Initial data can be input when the power is first applied, or standard data can be input during normal operation. Input serial data with the LSB first, i.e., starting from the D0 bit (LSB) of the first byte. Therefore, the D7 bit of the eighth byte is the most significant bit (MSB).

When inputting initial data, set a start-point wait time that specifies the delay from power application to pulse output, and the start-point drive wait time. At the same time, also set a chopping frequency and a reference voltage (EVR) that determines the output current of each channel. Because the μPD16835 has an EXT pin for monitoring the internal operations, the parameter to be monitored can be selected by initial data.

When inputting standard data, input the rotation direction of each channel, the number of pulses, and the data for the pulse cycle.

Initial data or standard data is selected by using bits D5 to D7 of the first byte (see **Table 1**).

Table 1. Data Selection Mode (1st byte)

D7	D6	D5	Data type
1	1	1	Initial data
0	0	0	Standard data

If the high-order three bits are high, the initial data is selected; if they are low, the standard data is selected. Data other than (0, 0, 0) and (1, 1, 1) must not be input.

Input the serial data during start-point wait time.

Details of Data Configuration

How to input initial data and standard data is described below.

(1) Initial data input

<First byte>

The first byte specifies the type of data (initial data or standard data) and determines the presence or absence of the EXP pin output. Bits D5 to D7 of this byte specify the type of data as shown in Table 1, while bits D0 to D3 select the EXP output (open drain).

Table 2. First Byte Data Configuration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	1	1	1	0	0 or 1	0 or 1	0 or 1	0 or 1

The EXP pin goes low (current sink) when the input data is “0”, and high (high-impedance state) when the input data is “1”. Pull this pin up to V_{DD} for use.
Input “0” to bit D4.

<Second byte>

The second byte specifies the delay between data being read and data being output. This delay is called the start-up wait time, and the motor can be driven from that point at which the start-up wait time is “0”. This time is counted at the rising edge of V_D. The start-up wait time can be set to 65.28 ms (when a 4-MHz clock is input), and can be fine-tuned by means of 8-bit division (256-μs step: with 4-MHz clock). The start-up wait time is set to 65.28 ms when all the bits of the second byte are set to “1”. Always input data other than “0” to this byte because the start-up wait time is necessary for latching data. If “0” is input to this byte, data cannot be updated. Transfer standard data during the start-up wait time.

<Third byte>

The third byte specifies the delay between the start-point wait time being cleared and the output pulse being generated. This time is called the start-up drive wait time, and the output pulse is generated from the point at which the start-up drive wait time reaches "0". The start-up drive wait time is counted at the falling edge of the start-up wait time. The start-up drive wait time can be set to 65.28 ms (with 4-MHz clock) and can be fine-tuned by means of 8-bit division (256-μs step: with 4-MHz clock). The start-up drive wait time is set to 65.28 ms when all the bits of the third byte are "1". Always input data other than "0" to this byte because the start-up drive wait time is necessary for latching data. If "0" is input to this byte, data cannot be updated.

<Fourth byte>

The fourth byte selects a chopping frequency by using 5-bit data. It also selects whether the chopping frequency is created by dividing the original oscillation (external clock) or whether the internal oscillator is used. The chopping frequency is selected by bits D0 to D4. Bit D7 specifies the method used to create the chopping frequency. When this bit is "0", the original oscillation (external clock input to OSC_{IN}) is used; when it is "1", the internal oscillator is used. Bits D5 and D6 are fixed to "0". The chopping signal is output after the initial data has been input and the first standard data has been latched (see Timing Chart).

Table 3. Fourth Byte Data Configuration (Initial data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0	0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

The chopping frequency is set to 0 kHz and to a value in the range of 32 to 124 kHz (in 4-kHz steps), as follows. Although the chopping frequency is set by 5 bits of data, it is internally configured using 7-bit data (with the low-order 2 bits fixed to 0).

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0	0	0	0	0	0	0

f_{OSC} = 0 kHz

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0	0	0	0	1	1	1

f_{OSC} = 0 kHz

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0	0	0	1	0	0	0

f_{OSC} = 32 kHz

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0	0	0	1	0	0	1

f_{OSC} = 36 kHz

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0	0	1	1	1	1	1

f_{OSC} = 124 kHz

<Fifth byte>

The fifth byte selects a parameter to be output to the EXTOUT pin (logic operation monitor pin). Input data to bits D0 to D6 of this byte. Bit D7 is fixed to "0". There are two EXTOUT pins. EXTOUT α indicates the operating status of α ch, and EXTOUT β indicates that of β ch. The relationship between each bit and each EXTOUT pin is as shown in Table 4.

Table 4. Fifth Byte Data Configuration (Initial data)

Bit	Data	EXTOUT α	EXTOUT β
D7	0	Not used	Not used
D6	0 or 1	ENABLE α	ENABLE β
D5	0 or 1	ROTATION α	ROTATION β
D4	0 or 1	PULSEOUT α	PULSEOUT β
D3	0 or 1	FF7 α	FF7 β
D2	0 or 1	FF3 α	FF3 β
D1	0 or 1	CHECKSUM	FF2 β
D0	0 or 1	CHOPPING	FF1 β

The checksum bit is cleared to "0" in the event of an error. Normally, it is "1".

If two or more signals that output signals to EXTOUT α and EXTOUT β are selected, they are positively ORed for output.

The CHOPPING signal is not output in internal oscillation mode.

The meanings of the symbols listed in Table 4 are as follows:

ENABLE: Output setting (H: Conducts, L: Stops)

ROTATION: Rotation direction (H: Reverse (CCW), L: Forward (CW))

PULSEOUT: Output pulse signal

FF7: Presence/absence of pulse in LATCH cycle (Outputs H level if output pulse information exists in standard data.)

FF3: Pulse gate (output while pulse exists)

FF2: Outputs H level during start-up wait time + start-up drive wait time

FF1: Outputs H level during start-up wait time

CHECKSUM: Checksum output (H: when normal data is transmitted, L: when abnormal data is transmitted)

CHOPPING: Chopping wave output (in original oscillation mode only)

<Sixth byte>

The sixth byte sets the peak output current value of α ch. The output current is determined by the EVR reference voltage.

The 250-mV (TYP.) voltage input from an external source to the V_{REF} pin is internally doubled and input to a 4-bit D/A converter. By dividing this voltage by 4-bit data, an EVR reference voltage can be set inside the IC within the range of 200 to 500 mV, in units of 20 mV.

The μPD16835 can set two values of the EVR reference voltage in advance. This is done by using bits D0 to D3 or D4 to D7. Which of the two EVR reference voltage values is to be used is specified by the CURRENT_SET bit in the standard data.

If all the bits of the sixth byte are "0", the EVR reference voltage of 200 mV is selected; if they are "1", the EVR reference voltage of 500 mV is selected.

Table 5. Sixth Byte Data Configuration (Initial data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

Bits D4 to D7: Reference voltage 2 ($EVR_{\alpha 2}$)

Bits D0 to D3: Reference voltage 1 ($EVR_{\alpha 1}$)

<Seventh byte>

The seventh byte specifies the peak output current value of β ch. The output current is determined by the EVR reference voltage.

The 250-mV (TYP.) voltage input from an external source to the V_{REF} pin is internally doubled and input to a 4-bit D/A converter. By dividing this voltage by 4-bit data, an EVR reference voltage can be set inside the IC within a range of 200 to 500 mV, in units of 20 mV.

The μPD16835 can set two values of the EVR reference voltage in advance. This is done using bits D0 to D3 or D4 to D7. Which of the two EVR reference voltage values is to be used is specified by the CURRENT_SET bit in the standard data.

If all the bits of the seventh byte are "0", the EVR reference voltage of 200 mV is selected; if they are "1", the EVR reference voltage of 500 mV is selected.

Table 6. Seventh Byte Data Configuration (Initial data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

Bits D4 to D7: Reference voltage 2 ($EVR_{\beta 2}$)

Bits D0 to D3: Reference voltage 1 ($EVR_{\beta 1}$)

<Eighth byte>

The eighth byte is checksum data. Normally, the sum of the 8-byte data is 00h.

If the sum is not 00h because data transmission is abnormal, the stepping operation is inhibited and the checksum output pin (EXT pin) is kept "L".

(2) Standard data input

<First byte>

The first byte specifies the type of data and whether the EXP pin output is used, such as when the initial data is input.

Table 7. First Byte Data Configuration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	1	1	1	0	0 or 1	0 or 1	0 or 1	0 or 1

The EXP pin goes low (current sink) when the input data is “0”, and high (high-impedance state) when the input data is “1”. Input “0” to bit D4.

<Second byte>

The second byte specifies the rotation direction of the α channel, enables output of the α channel, and the number of pulses (252 pulses MAX.) during the $1V_D$ period (in 1 cycle of FF2) of the α channel.

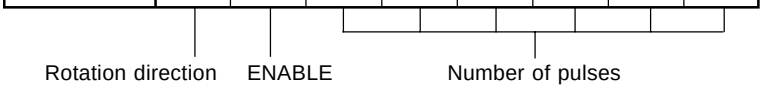
Bit D7 is used to specify the rotation direction. The rotation is in the forward direction (CW mode) when this bit is “0”; it is in the reverse direction (CCW mode) when the bit is “1”.

Bit D6 is used to enable the output of the α channel. The α channel enters the high-impedance state when this bit is “0”; it is in conduction mode when the bit is “1”.

The number of pulses is set by bits D0 to D5. It is set by 6 bits in terms of software. However, the actual circuit uses an 8-bit counter with the low-order two bits fixed to “0”. Therefore, the number of pulses that is actually generated during start-up wait time + start-up drive wait (FF2) cycle is the number of pulses input $\times$ 4. The number of pulses can be set to a value in the range of 0 to 252, in units of four pulses.

Table 8. Second Byte Data Configuration (Standard data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1



<Third and fourth bytes>

The third and fourth bytes select the pulse cycle of the α channel and which of the two reference voltages, created in the initial mode, is to be used (CURRENT SET α).

The pulse cycle is specified using 15 bits: bits D0 (least significant bit) to D7 of the third byte, and bits D0 to D6 (most significant bit) of the fourth byte. The pulse cycle can be set to a value in the range of 0.25 to 8,191.75 μs in units of 0.25 μs (with a 4-MHz clock).

CURRENT SET α is specified by bit D7 of the fourth byte. When this bit is "0", reference voltage 1 ($EVR_{\alpha 1}$) is selected; when it is "1", reference voltage 2 ($EVR_{\alpha 2}$) is selected. For further information, refer to the description of the sixth byte of the initial data.

Table 9. Fourth Byte Data Configuration (Standard data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

CURRENT SET α — Most significant bit

Table 10. Third Byte Data Configuration (Standard data)

D7	D6	D5	D4	D3	D2	D1	D0
0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

Least significant bit

(Reference) Sixth Byte Data Configuration for Initial Data

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

Bits D4 to D7: Reference voltage 2 ($EVR_{\alpha 2}$)

Bits D0 to D3: Reference voltage 1 ($EVR_{\alpha 1}$)

<Fifth byte>

The fifth byte specifies the rotation direction of the β channel, enables output of the β channel, and the number of pulses (252 pulses MAX.) during the $1V_D$ period (in one cycle of FF2) of the β channel.

Bit D7 is used to specify the rotation direction. The rotation is in the forward direction (CW mode) when this bit is "0"; it is in the reverse direction (CCW mode) when the bit is "1".

Bit D6 is used to enable the output of the β channel. The β channel goes into a high-impedance state when this bit is "0"; it is in the conduction mode when the bit is "1".

The number of pulses is set by bits D0 to D5. It is set by six bits in terms of software. However, the actual circuit uses an 8-bit decoder with the low-order two bits fixed to "0". Therefore, the number of pulses that is actually generated during start-up wait time + start-up drive wait (FF2) cycle is the number of pulses input $\times$ 4. The number of pulses can be set in a range of 0 to 252 and in units of four pulses.

Table 11. Fifth Byte Data Configuration (Standard data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

Rotation direction — ENABLE — Number of pulses

<Sixth and seventh bytes>

The sixth and seventh bytes select the pulse cycle of the β channel and which of the two reference voltages, created in the initial mode, is to be used (CURRENT SET β).

The pulse cycle is specified using 15 bits: bits D0 (least significant bit) to D7 of the sixth byte, and bits D0 to D6 (most significant bit) of the seventh byte. The pulse cycle can be set to a value in the range of 0.25 to 8,191.75 μs in units of 0.25 μs (with a 4-MHz clock).

CURRENT SET β is specified by bit D7 of the seventh byte. When this bit is "0", reference voltage 1 ($EVR_{\beta 1}$) is selected; when it is "1", reference voltage 2 ($EVR_{\beta 2}$) is selected. For further information, refer to the description of the seventh byte of the initial data.

Table 12. Seventh Byte Data Configuration (Standard data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

CURRENT SET β — Most significant bit

Table 13. Sixth Byte Data Configuration (Standard data)

D7	D6	D5	D4	D3	D2	D1	D0
0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

Least significant bit

(Reference) Seventh Byte Data Configuration for Initial Data

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

Bits D4 to D7: Reference voltage 2 ($EVR_{\beta 2}$)

Bits D0 to D3: Reference voltage 1 ($EVR_{\beta 1}$)

<Eighth byte>

The eighth byte is checksum data. Normally, the sum of the 8-byte data is 00h.

If the sum is not 00h because data transmission is abnormal, the stepping operation is inhibited and the checksum output pin (EXT pin) is held at "L".

Data Update Timing

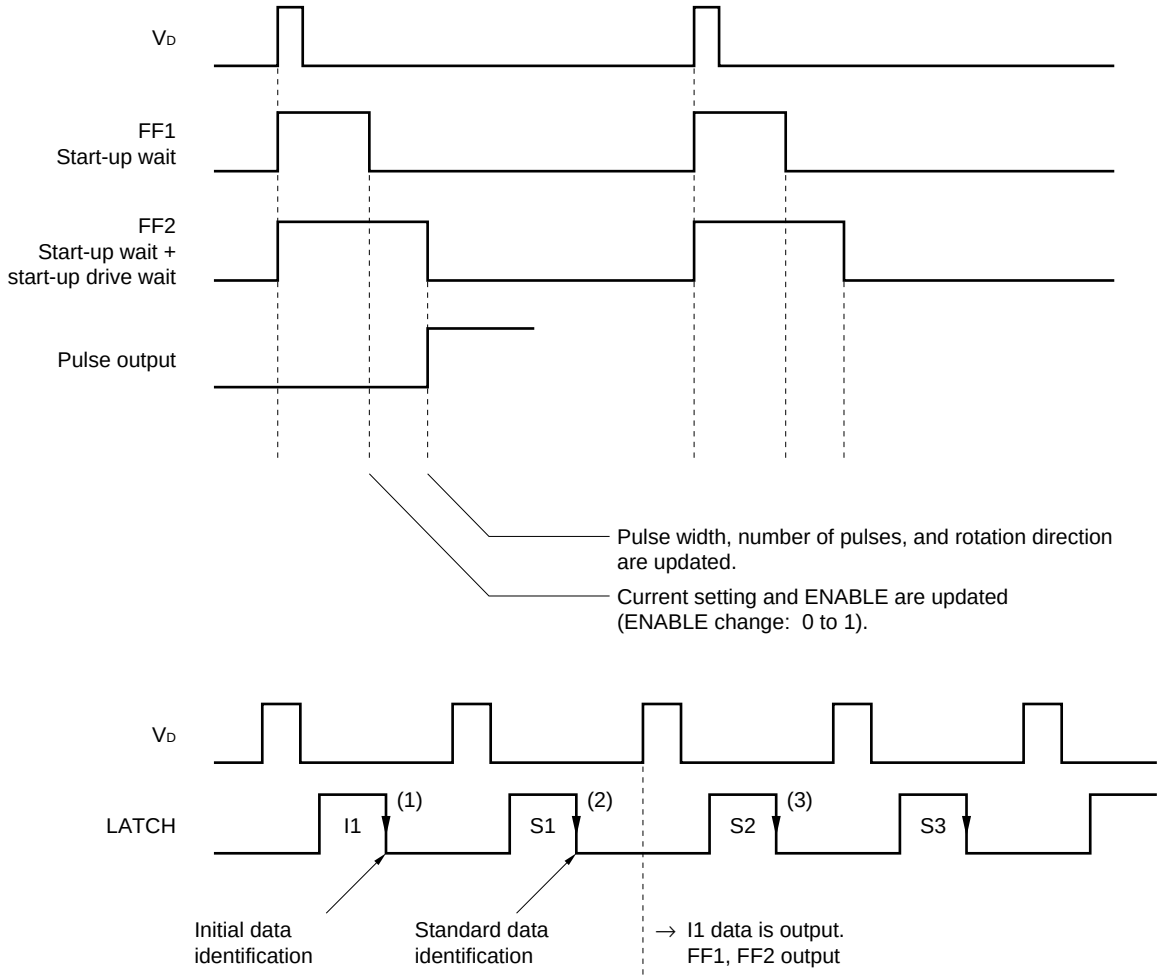
The standard data (pulse width, number of pulses, rotation direction, current setting, and ENABLE) of this product are set and updated at the following latch timing.

Table 14. Data Update Timing

ENABLE change	1 → 1	0 → 1	1 → 0	0 → 0
Pulse width	FF2 ↓	FF2 ↓	FF2 ↓	-
Number of pulses	FF2 ↓	FF2 ↓	FF2 ↓	-
Rotation direction	FF2 ↓	FF2 ↓	FF2 ↓	-
Current setting	FF2 ↓	FF1 ↓	FF2 ↓	-
ENABLE	FF2 ↓	FF1 ↓	FF2 ↓	-

The timing at which data is to be updated differs, as shown in Table 14, depending on the enabled status.

For example, suppose the enable signal is currently "0" (output high-impedance) and "1" (output conduction) is input by the next data. In this case, the pulse width, number of pulses, and rotation direction signals are updated at FF2 (upon the completion of start-up wait), and the current setting and ENABLE signals are updated at FF1 (upon completion of start-up drive wait).



	(1)	(2)	(3)
Pulse width	Internal data retained. Output reset	Not output	Updated to S2 data at FF2
Rotation direction	Internal output retained	Not output	
Number of pulses	Internal data retained. Output reset	Not output	
Current setting	Internal output retained	Not output	Updated to S2 data at either FF1 or FF2 by enable data of (2)
ENABLE	Internal output retained	Not output	

The initial mode of this product is as follows.
The IC operation can be initialized as follows:

(1) Turns ON V_{DD}.
(2) Make RESET input “L”.
(3) Input serial initial data.

In initial mode, the operating status of the IC is as shown in Table 15.

Table 15. Operations in Initial Mode

Item	Specifications
Current consumption	100 μA
OSC	Oscillation stops. Input of external clock is inhibited.
V_D	Input inhibited.
FF1 to FF7	“L” level
PULSE OUT	“L” level
EXP0 to EXP3	Undefined in the case of (1) above. Previous value is retained in the case of (2) above. Can be updated by serial data in the case of (3) above.
Serial operation	Can be accessed after initialization in the case of (1) above. Can be accessed after RESET has gone “H” in the case of (2) above. Can be accessed in the case of (3) above.

Step pulse output is inhibited and FF7 is made “L” if the following conditions are satisfied.

(1) If the set number of pulses (2nd/5th: standard data) is 00h.
(2) If the checksum value is other than 00h.
(3) If the start-up wait time is set to $1V_D$ or longer.
(4) If the start-up wait time + start-up drive wait time is set to $1V_D$ or longer.
(5) If start-up wait is completed earlier than LATCH (↓).
(6) If V_D is not input.

HINTS ON CORRECT USE

(1) With this product, input the data for start-up wait and start-up drive wait.
Because the standard data are set or updated by these wait times, if the start-up wait time and start-up drive wait time are not input, the data are not updated.

(2) The start-up wait time must be longer than LATCH.

(3) If the rising of the start-up drive wait time is the same as the falling of the last output pulse, a count error occurs, and the IC may malfunction.

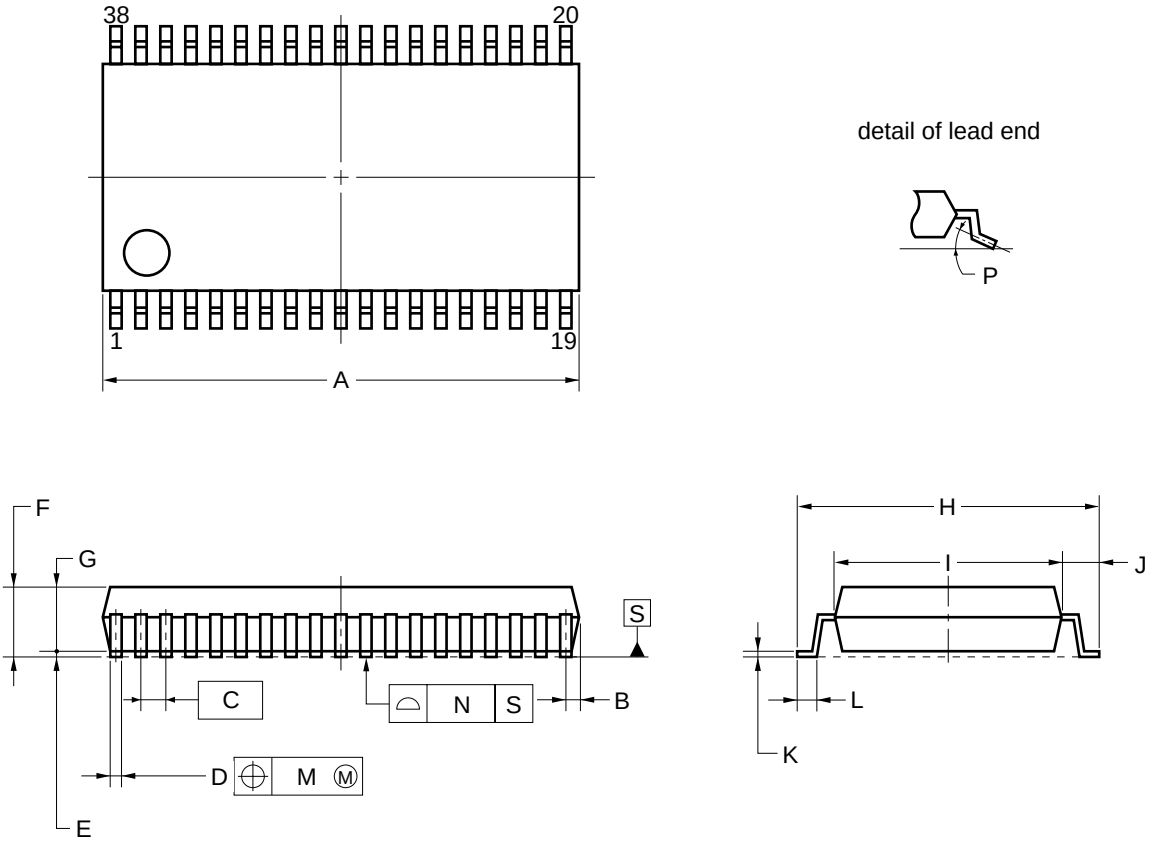
(4) Input the initial data in a manner that it does not straddle the video sync signal (V_D).
If it does, the initial data is not latched.

(5) Transmit the standard data during the start-up wait time (FF1). If it is input at any other time, the data may not be transmitted correctly.

(6) If the LGND potential is undefined, the data may not be input correctly. Keep the LGND potential to the minimum level. It is recommended that LGND and PGND be divided for connection (single ground) to prevent the leakage of noise from the output circuit.

PACKAGE

38 PIN PLASTIC SHRINK SOP (300 mil)



NOTE

1. Controlling dimension —— millimeter.

2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$12.45^{+0.26}_{-0.2}$	$0.490^{+0.011}_{-0.008}$
B	0.51 MAX.	0.020 MAX.
C	0.65 (T.P.)	0.026 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	$0.013^{+0.003}_{-0.004}$
E	0.125±0.075	0.005±0.003
F	2.0 MAX.	0.079 MAX.
G	1.7±0.1	0.067±0.004
H	8.1±0.3	0.319±0.012
I	6.1±0.2	0.240±0.008
J	1.0 ± 0.2	$0.039^{+0.009}_{-0.008}$
K	$0.17^{+0.08}_{-0.07}$	$0.007^{+0.003}_{-0.004}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	0.10	0.004
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P38GS-65-300B-2

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following conditions.

For details of the soldering method and when soldering under conditions other than those given below, contact NEC.

- For details of the recommended soldering conditions, refer to the **Semiconductor Device Mounting Technology Manual**.

Soldering method	Soldering conditions	Symbol indicating recommended soldering
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds MAX. (at 210°C MIN.), Number of times: 3 MAX., Number of days: None[Note], Flux: Rosin-based flux with low chlorine content (chlorine 0.2 Wt% MAX.) is recommended.	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 seconds MAX. (at 200°C MIN.), Number of times: 3 MAX., Number of days: None[Note], Flux: Rosin-based flux with low chlorine content (chlorine 0.2 Wt% MAX.) is recommended.	VP-15-00-3
Wave soldering	Package peak temperature: 260°C, Time: 10 seconds MAX., Preheating temperature: 120°C MAX., Number of times: 1, Flux: Rosin-based flux with low chlorine content (chlorine 0.2 Wt% MAX.) is recommended.	WS60-00-1

Note Number of days the device can be stored after the dry pack has been opened, at conditions of 25°C, 65% RH.

Caution Do not use two or more soldering methods in combination.

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