MOS INTEGRATED CIRCUIT
μPD1705C-014

PLL FREQUENCY SYNTHESIZER AND CONTROLLER FOR VHF, UHF AND CATV

The μPD1705C-014 is a CMOS LSI developed for television receivers of PLL frequency synthesizer system designed to U.S.A. and Canada. PLL and controller are contained on a single chip. This LSI, with the prescaler μPB568C, μPB568HA, μPB568G, constitues a high performance PLL television receiver system. Since PLL section uses pulse swallowing system, fine tuning can be easily done with a high precision. Furthermore, it is provided with functions of remote control.

FEATURES

- PLL and controller are packed in one chip.
- Multifarious station selection modes
  - 10-key direct selection
  - Auto-search type up/down selection
  - Skip-memory type up/down selection
- High precision fine tuning capable by the use of pulse swallowing method.
  (40 kHz per step over ±2.2 MHz range)
- Channel search function
- CATV station can be selected. (TRADITIONAL and H.R.C. options)
- Built-in remote control decoder (μPD6121G-002 and μPC1373HA are used.)
- Provided with the function to channel number BCD output for CRT display interface
- CMOS structure with low power consumption
- 5 V ±10 % single power supply

ORDERING INFORMATION

Order Code	Package
μPD1705C-014	42-Pin Plastic DIP (600 mil)

FUNCTIONS

Receiving band, Channel number, Receiving frequency and Intermediate frequency

RECEIVING BAND		CHANNEL NUMBER	RECEIVING FREQUENCY (video carrier frequency)		INTERMEDIATE FREQUENCY
			TRADITIONAL	H.R.C.	
TV	VL	2 to 6	55.25 to 83.25 MHz		45.75 MHz
	VH	7 to 13	175.25 to 221.25		
	UB	14 to 83	471.25 to 885.25		
CATV	VL	2 to 6	55.25 to 83.25	54.0 to 78.0	
	MB	A-5 to I	91.25 to 169.25	90.0 to 168.0	
	VH	7 to 13	175.25 to 211.25	174.0 to 210.0	
	SB	J to W	217.25 to 295.25	216.0 to 294.0	
	HIPB	AA to WW	301.25 to 433.25	300.0 to 432.0	

Channel selection

(1) Direct selection by 10-key operation

(2) Channel up/down selection

Auto search selection

Skip memory selection

Manual fine tuning (MFT)

40 kHz per step, maximum range of ±2.2 MHz

125 ms per cycle

Auto fine tuning (AFT)

40 kHz per step, maximum range of ±2.2 MHz

Detection at every 10 ms.

Remote control functions

Built-in remote control reception functions

Connections to μPD6121G-002 (for transmitter) and μPC1373HA (receiver preamplifier) possible

Display

3-digits dynamic display (approx. 300 Hz)

2-digits plus TV/CATV display

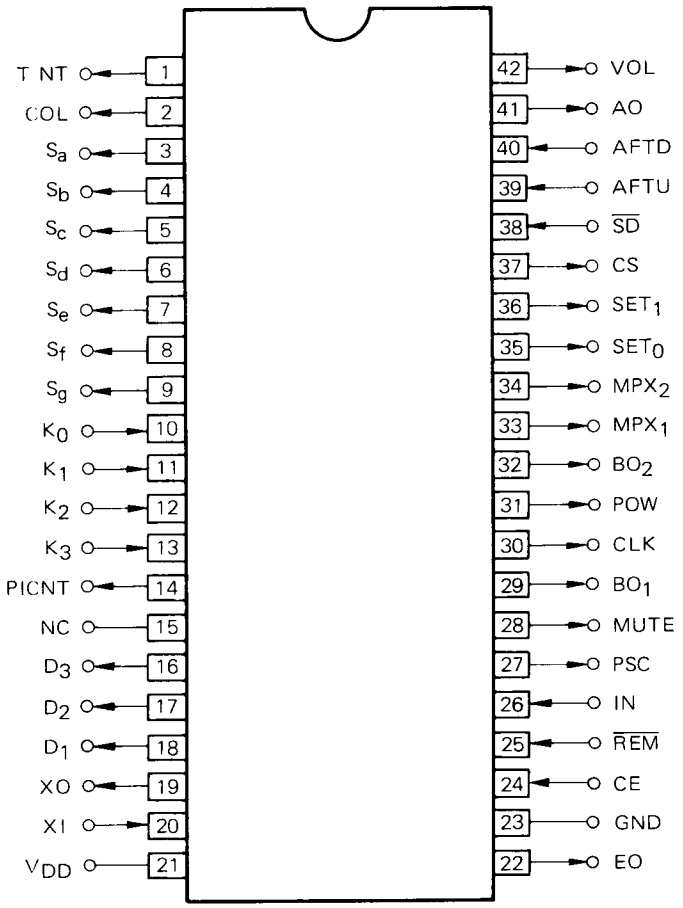
BCD output for CRT display interface

Connection to MM58146 via μPD4015BC possible

Comparative frequency

f_r = 5 kHz

PIN CONFIGURATION (Top View)



NC: No Connection

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME	DESCRIPTION	OUTPUT TYPE
1	TINT	Tint	Output pin of variable duty pulses to tint control. Output passed to DC attenuator via an external low-pass filter.	CMOS Push-pull
2	COL	Color	Output pin of variable duty pulses to color control. Input passed to DC attenuator via an external low-pass filter.	CMOS Push-pull
3 to 9	S_a to S_g	Segment Output	7-segment display output pins — also used as output for key matrix. High voltage endurance (−30 V). Active high.	P-ch Open drain
10 to 13	K_0 to K_3	Key-return Signal Input	Input of key matrix return signal.	Input
14	PICMT	Picture muting	Active high signal output pin used to eliminate picture noise during up/down channel selection.	CMOS Push-pull
16 to 18	D_3 to D_1	Digit Output	Output of active high display digit signal.	CMOS Push-pull
19 20	XO XI	X'tal	4.5 MHz crystal resonator is connected here. Built-in feedback resistance.	CMOS Push-pull (XO) Input (XI)
21	V_{DD}	Power supply	+5 V ±10 % power supply The V_{DD} rise time must be less than 500 ms. The device may not be correctly initialized if the rise time is very long.	—
22	EO	Phase detector output	Phase detector charge pump output for supply of channel selection voltage to tuner varactor via low-pass filter.	CMOS 3-state
23	GND	Ground	Connect to the ground of system.	—
24	CE	Chip Enable	High . . . . Normal operation Low . . . . Memory hold (display OFF, PLL functions dissabled.) Low level signals of less than 134 μs are not accepted.	Input
25	$\overline{REM}$	Remote control signal input	Input pin for remote control signal connected to the μPC1373HA preamplifier output. Active low.	Input
26	IN	Local oscillator input	Input of tuner oscillator signal passed via the μPB568 prescalar. Because of the built-in AC amplifier, use a capacitor to eliminate DC components.	Input Internal self-bias
27	PSC	Pulse swallowing control	Pulse swallow control pin to be connected to the PSC pin of the μPB568 prescalar.	CMOS Push-pull
28	MUTE	Mute Output	Output pin of active high signal used to eliminate noise if the PLL lock is upset.	CMOS Push-pull
29 32	BO_1 BO_2	Band	Signal output pin of tuner band selector. The output formats of this signal is given below.	N-ch Open drain

	VL	MB,VH	SB	UB	HIPB
BO_1	L	H	H	L	L
BO_2	H	H	L	L	L

PIN NO.	SYMBOL	NAME	DESCRIPTION	OUTPUT TYPE
30	CLK	Clock output	Serial output clock pin of BCD channel number.	P-ch Open drain
31	POW	Power	Power output pin for controlling power supply.	P-ch Open drain
33 34	MPX_1 MPX_2	Audio multiplex selector output	Output pin of audio multiplex mode selector.	P-ch Open drain
35 36	SET_0 SET_1	Skip memory data output	Skip data output pin (for data passed to external skip memory ER0082). Active low.	P-ch Open drain
37	CS	Chip select	Output pin for skip memory data reading pulse, and may also be used for output of recall signal to CRT display interface (MM58146).	CMOS push-pull (I/O)
38	$\overline{SD}$	Station Detector	Stop signal input pin used in skip memory and auto search channel selection operations. Active low. During auto search operations, this pin must be switched to low level within 100 ms after the PLL is locked.	CMOS Push-pull (I/O)
39 40	AFTU AFTD	AFT input	Input pin for AFT signal. The AFT signal is split into two values by the μPC393C comparator before being applied to this input pin.	CMOS Push-pull (I/O)
41	AO	Address output	BCD channel number serial pin used to pass address outputs to the skip memory and data outputs to the CRT display interface via an external shift register (μPD4015BC).	P-ch Open drain
42	VOL	Volume	Output pin for volume control variable duty pulse. This output is applied to the DC attenuator via an external low-pass filter.	CMOS Push-pull

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1. KEY MATRIX

1.1 CONFIGURATION OF KEY MATRIX

Input / Output pin	K_3 (13)	K_2 (12)	K_1 (11)	K_0 (10)
S_a (3)	0	1	2	3
S_b (4)	4	5	6	7
S_c (5)	8	9	FTU	FTD
S_d (6)	CHU	VOLU	COLU	TINTU
S_e (7)	CHD	VOLD	COLD	TINTD
S_f (8)	ERASE	WRITE	SHIFT	POWER
S_g (9)	CATV/TV	AFT	CHLOCK	SELECT
D_3 (16)				
D_2 (17)	–	–	–	

Momentary switch

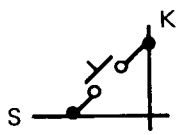
Alternate switch

Diode matrix

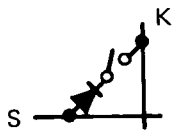
– Open

1.2 SWITCH CONNECTION

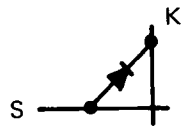
Momentary switch



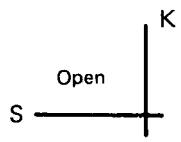
Alternate switch



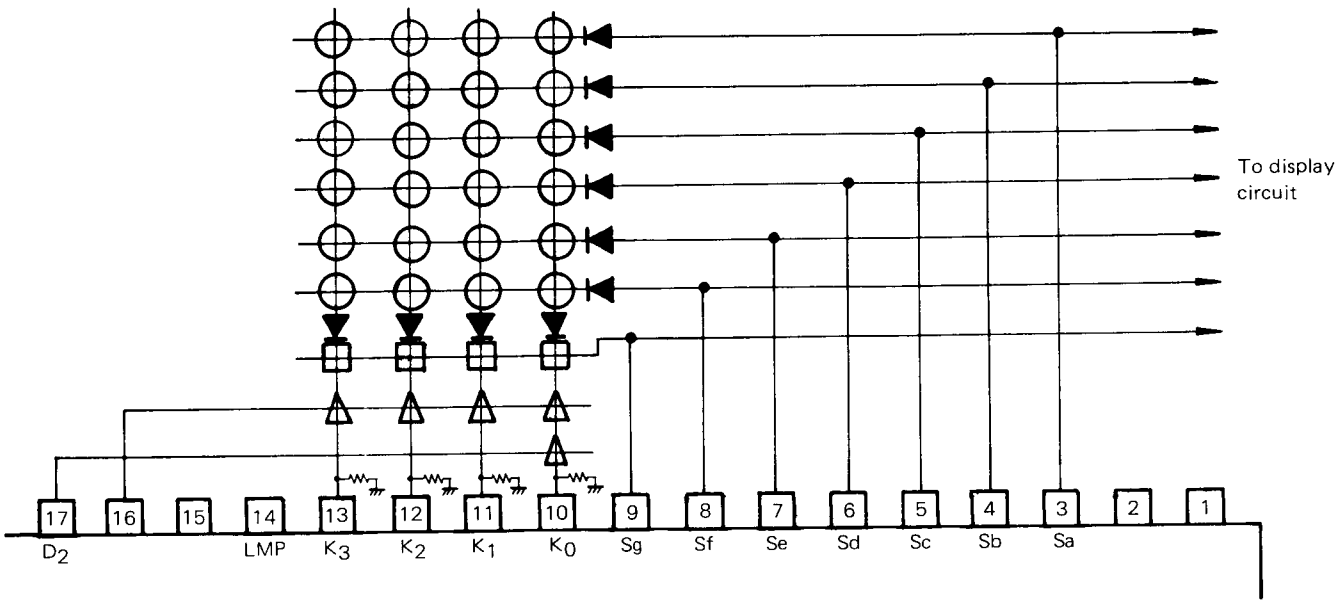
Diode matrix

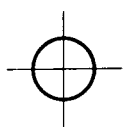


or

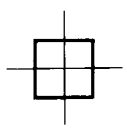


1.3 KEY MATRIX CONNECTION

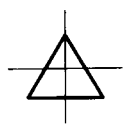




Momentary switch



Alternate switch



Diode matrix

1.4 DESCRIPTION OF KEY MATRIX

Momentary switch

SYMBOL	DESCRIPTION
0 1 2 3 4 5 6 7 8 9	Keys used in direct channel selection where the required channel is specified by 2-digits input. (For example, and 8 are keyed in to select channel 8, and 1 and 2 are keyed in to select channel 12.) Note that the display reverts to the original state if the second key is not pressed within 3 to 4 seconds after pressing the first key (2 to 9). The display is also reverted to the previous channel display if a non-existent channel is selected.
FTU	Fine tuning key used only in manual mode. The tuned frequency is increased by a single 40 kHz step when this key is pressed and released again within 500 ms. If press for more than 500 ms, the tuned frequency is increased in 40 kHz steps at each 125 ms interval. If the upper limit (+2.2 MHz) is reached, the frequency returns to the lower limit (−2.2 MHz) before continuing to increase. This fined tuned status is cancelled if another channel is selected.
FTD	Except for decreased the tuned frequency, this key is the same as the FTU key.
CHU	When the CHU key is pressed during skip memory mode (MEM/AT switch: OFF), the next highest channel is selected irrespective of any input signal being spplied to the SD pin when the SELECT switch is on. And if the CHU key remains depressed, the next highest channel is selected successively at 600 ms intervals until the key is released. If the SELECT switch is off, the next highest channel is selected successively until the channel where stop data os stpred os reached (while reading the skip memory contents). The same automatic operation is executed (with each new channel selected at a rate of one channel per 600 ms) if the CHU key remains depressed. If the CHU key is pressed during auto search mode (MEM/AT switch: ON), the next highest channels are selected successively until a broadcasting channel is reached. If the key remains depressed, this automatic operation is continued after waiting 600 ms at that broadcasting channel.
CHD	Except for selecting the next lowest channel, this key is the same as the CHU key.
VOLU	Volume control key. The volume is increased at a rate of one step every 100 ms until the key is released again. With a total of 64 steps (duty ratio: 0/67 and 3/67 to 65/67), the volume can be adjusted gradually.
VOLD	Except for decreasing the volume, this key is the same as the VOLU key.

SYMBOL	DESCRIPTION
COLU COLD	Color adjustment key. Operation is basically the same as the VOLU and VOLD keys.
TINTU TINTD	Tint adjustment key. Operation is basically the same as the VOLU amd VOLD keys.
ERASE	The key used in writing skip data (1) into the skip memory. (Valid only when the SELECT switch is on.) When this key is pressed with the SELECT switch on, the currently selected channel is erased, and is skipped during subsequent up/down channel selection operations. Muting status is switched on when this key is pressed.
WRITE	The key used in writing skip data (0) into the skip memory. (Valid only when the SELECT switch is on.) When this key is pressed with the SELECT switch on, the currently selected channel is stored in memory, and is selected during subsequent up/down channel selection operations. Muting status is switched on when this key is pressed.
SHIFT	Audio multiplex mode selector key. The audio multiplex selector outputs (MPX1 and MPX2) are switched in cyclic fashion each time this key is pressed.
POWER	Power supply control key. The power output is inverted each time the POWER key is pressed. When the power is switched on, the muting is released and the last channel is selected. When the power is switched off, the display is cleared and all other keys (apart from the POWER key) are disabled.

	→	→
MPX_1 (33)	1	1	0
MPX_2 (34)	1	0	1

Alternate Switch

SYMBOL	DESCRIPTION
CATV/TV	CATV is selected when the band selector switch is on, and TV is selected when off. When CATV is selected, channels 2 to 36 (VFH channels 2 to 13 and CATV channels 14 to 36) can be received in 105 channel mode (CHNSEL: OFF), and channels 2 to 64 (VFH channels 2 to 13 and CATV channels 14 to 64) can be received in 133 channel mode (CHNSEL: ON). And when TV is selected, channels 2 to 83 (VFH channels 2 to 13 and UHF channels 14 to 83) can be received. Note that all modes are initialized at channel 2 when the switch is pressed.
AFT	Tuning mode selector switch. AFT mode operations are executed in accordance with an externally supplied AFT signal when the switch is on. The [FTU] and [FTD] keys are disabled in this case.
CH LOCK	Misoperation prevention key. The ten numerical keys (0 to 9) and the [CHU] and [CHD] keys are disabled when this key is on, thereby preventing the operator from changing the selected channel. Channels can be freely selected when this switch is off.
SELECT	The [ERASE] and [WRITE] keys are enabled when the skip memory write/erase switch is on. Note that the muting, volume control, and shift keys are disabled in this case. Conversely, the [ERASE] and [WRITE] keys are disabled when the SELECT switch is off, and station select operations comply with the memory contents during channel up/down selection.

Initial Diode Switch

<table>
<tr><th>SYMBOL</th><th>DESCRIPTION</th></tr>
<tr><td>CHNSEL</td><td>Setting of the number of channels which may be received. 133 channel mode is selected when CHNSEL is on, and 105 channel mode is selected when off. The number of channels which may be selected in each mode is given below.
<table>
<tr><th>STATUS</th><th>CHANNELS RECEIVED</th></tr>
<tr><td>1</td><td>VHF : 2 ch to 13 ch
UHF : 14 ch to 83 ch
CATV : 14 ch to 64 ch
(A ch to W ch
AA ch to WW ch
A-1 ch to A-5 ch)</td></tr>
<tr><td>0</td><td>VHF : 2 ch to 13 ch
UHF : 14 ch to 83 ch
CATV : 14 ch to 36 ch
(A ch to W ch)</td></tr>
</table></td></tr>
<tr><td>MEM/AT</td><td>Channel up/down selection mode setting. Auto search mode is selected when MEM/AT is on, and skip memory mode is selected when off.</td></tr>
<tr><td>VOLIN$_1$
VOLIN$_2$</td><td>Volume level initialization. Four different initial volume levels can be selected by the following connections.
<table>
<tr><th colspan="2">STATUS</th><th rowspan="2">INITIAL VOLUME LEVEL</th></tr>
<tr><th>VOLIN$_2$</th><th>VOLIN$_1$</th></tr>
<tr><td>0</td><td>0</td><td>25 %</td></tr>
<tr><td>0</td><td>1</td><td>37 %</td></tr>
<tr><td>1</td><td>0</td><td>50 %</td></tr>
<tr><td>1</td><td>1</td><td>61 %</td></tr>
</table></td></tr>
<tr><td>TRADHRC</td><td>CATV reception mode setting. TRADITIONAL mode is selected when TRADHRC is on, and H.R.C. mode is selected when off.</td></tr>
</table>

Note: In this table, "1" or "on" denotes diode shorted, and "0" or "off" denotes diode open.

2. CATV CHANNEL NUMBERS

The correspondence of the CATV channels to actually keyed-in channel numbers as well as displayed channel numbers is shown in the following table.

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W
14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36

AA	BB	CC	DD	EE	FF	GG	HH	II	JJ	KK	LL	MM	NN	OO	PP	QQ	RR	SS	TT	UU	VV	WW
37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59

A-1	A-2	A-3	A-4	A-5
60	61	62	63	64

3. REMOTE CONTROL FUNCTION

The μPD1705C-014 is equipped with built-in remote control functions to enable remote control operations in combination with μPD6121G-002 (for transmitter) and μPC1373HA (reception preamplifier).

The remote control functions available in this combination

- Direct channel selection by 10-key operation
- Channel up/down channel selection (auto search and skip memory)
- Power on/off
- Muting on/off
- Volume up/down (in 64 steps) . . . . . initialized levels of 25 %, 37 %, 50 %, or 61 %
- Color up/down (in 64 steps) . . . . . initialized level of 50 %
- Tint up/down (in 64 steps) . . . . . initialized level of 50 %
- Shift function (see section on SHIFT key)
- Recall function . . . . . Output of display timing signal to CRT display interface
- Initialization function . . . . . Color and tint initialization (50 %)

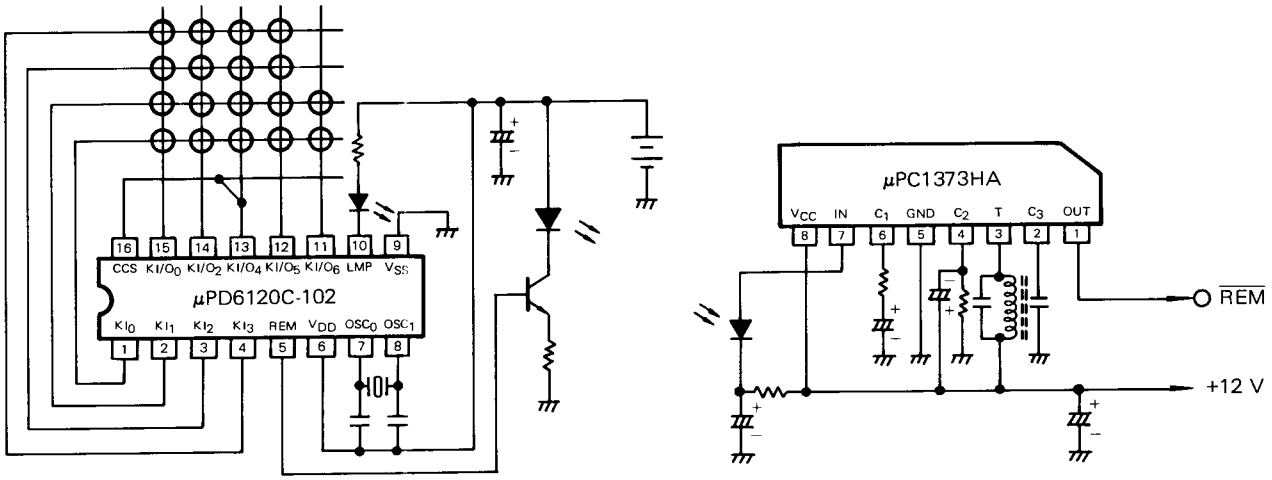
Note: The transmitter custom codes used are C_0 to C_7 = 00100000. No other codes can be used.

Remote Control Transmitter (μPD6121G-002) Key Configuration

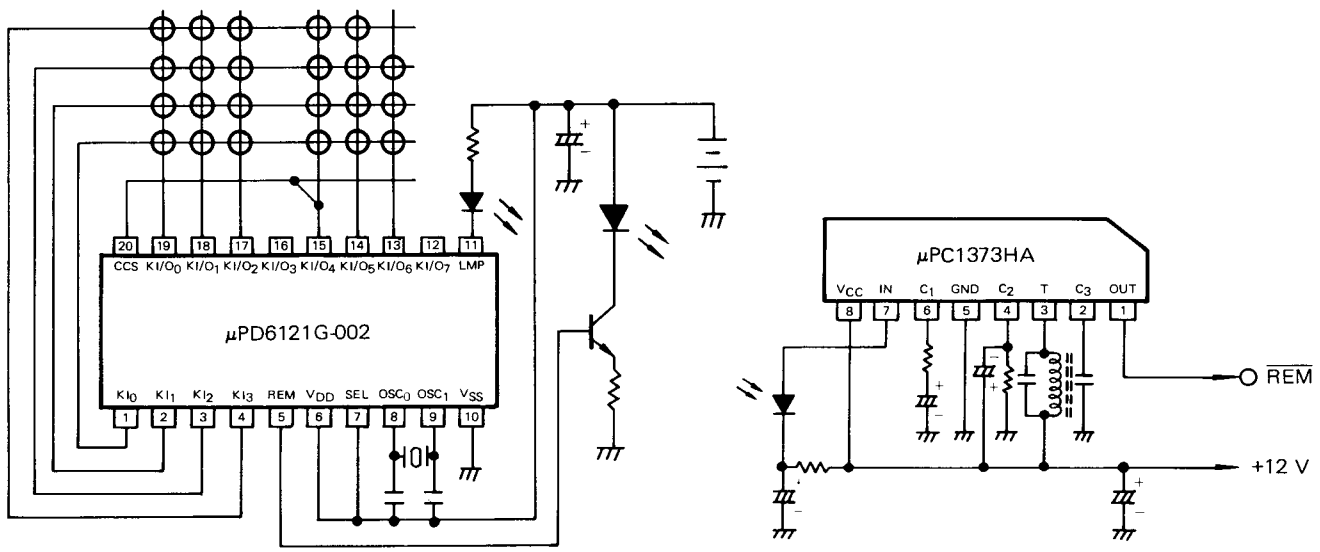
	KI_0	KI_1	KI_2	KI_3
KI/O_0	CHU	CHD	VULU	VOLD
KI/O_1	COLU	COLD	TINTU	TINTD
KI/O_2	POWER	MUTE	SHIFT	RECALL
KI/O_4	0	1	2	3
KI/O_5	4	5	6	7
KI/O_6	8	9	INITIAL	–

Remote Control Connection Diagrams

- When μPD6120C-102 is used.



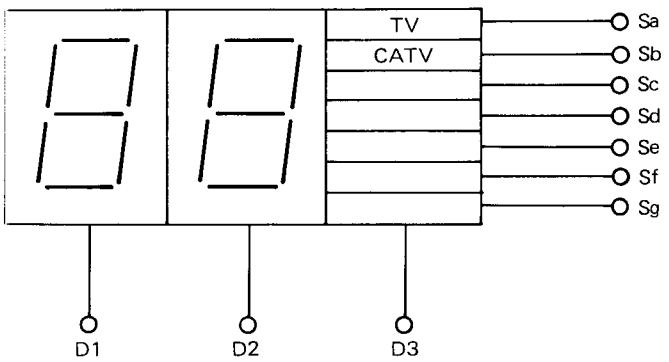
- When μPD6121G-002 is used.



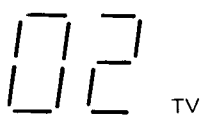
Note: Color and tint cannot be controlled if μPD6120C-102 is used.

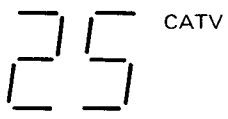
4. DISPLAY

The display format is a 7-segment 3-digit dynamic display. (Repetition frequency: approximately 300 Hz, duty ratio: approximately 30 %). The display connections are shown in the following diagram.



Display examples





Note: No display when power is off.

5. FINE TUNING FUNCTION

The μPD1705C-014 is equipped with high precision fine tuning functions designed to cope with frequency displacements occurring at the broadcasting station. These functions enable easy correction of reception frequency displacements. Fine tuning may be manual mode (MFT) or automatic (AFT).

(1) Manual fine tuning (MFT)

The [FTU] and [FTD] keys are used in manual fine tuning. The fine tuned status is reset if another channel is selected. The [FTU] and [FTD] keys are enabled only when the AFT switch is off (manual mode).

Frequencies are fine tuned in 40 kHz steps at each 125 ms interval, and can be changed by up to ±2.2 MHz.

(2) Auto fine tuning (AFT)

Auto fine tuning is only enabled when the AUT/MAN switch is on (auto mode). Auto tuning is operated by an externally applied AFT signal with the tuning responding to all changes in that AFT signal. Note that AFT is disabled during channel selection. Frequencies are fine tuned in 40 kHz steps at each 8 ms interval, and can be changed by up to ±2.2 MHz.

AFT is activated by signals applied to the AFTU and AFTD pins. The reception frequency is increased when a high level signal is applied to the AFTU pin, and decreased when a high level signal is applied to the AFTD pin. AFT is stopped when low level signals are applied to both the AFTU and AFTD pins.

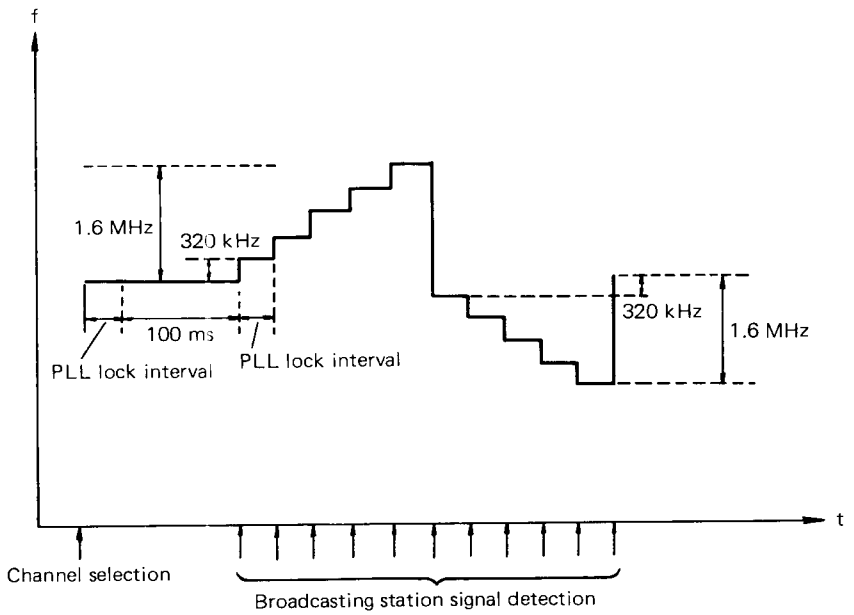
Note: Both MFT and AFT proceed in cyclic fashion with the frequency being returned to the lower (upper) limit when the upper (lower) limit is reached.

6. AUTO SEARCH FUNCTION

When μPD1705C-014 is used in auto search mode, the processor automatically checks for the presence of a broadcasting station at each successive channel.

If an input signal cannot be detected at the specified frequency due to frequency variation at the broadcasting station, the reception frequency can be changed in 320 kHz steps (up to a maximum of ±1.6 MHz) (channel search function).

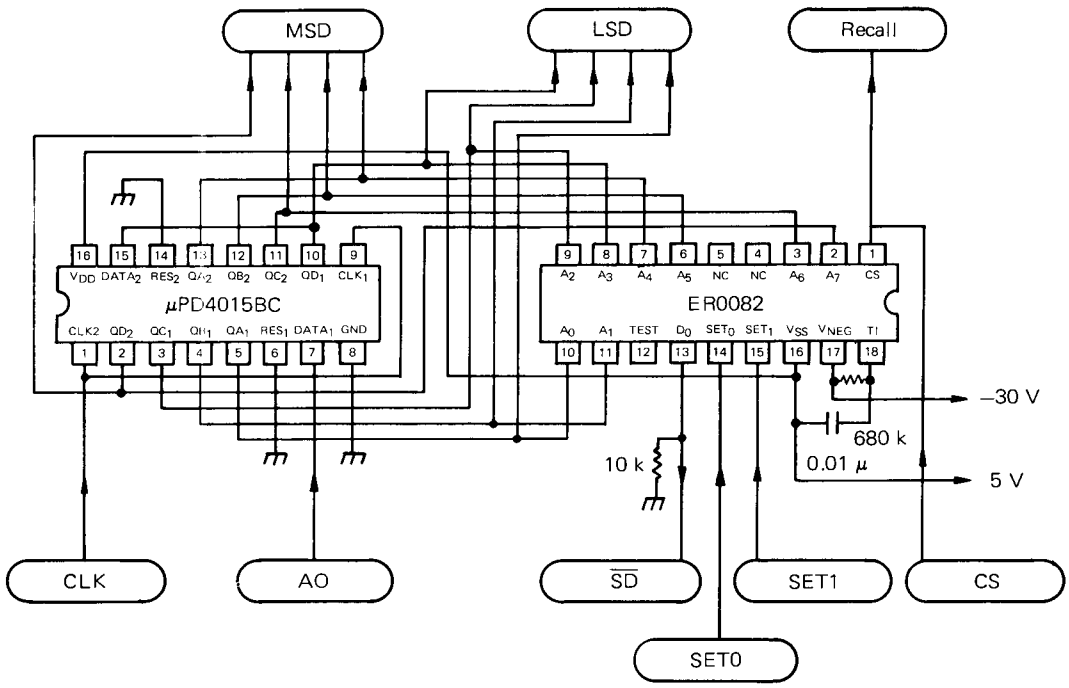
If the reception frequency is detected during this operation, the search is stopped at that frequency. And if no signal is detected at all, the processor proceeds to search for the next channel. The search process within a single channel range is outlined in the following diagram.



7. THE SKIP MEMORY FUNCTION AND CRT DISPLAY

The connections for using μPD1705C-014 in skip memory mode are outlined in the following diagram. Since address data passed to memory is passed serially from the AO pin (pin 41) synchronized with the clock output from the CLK pin (pin 30), this is converted to 8-bits parallel data by μPD4015BC and connected to ER0082.

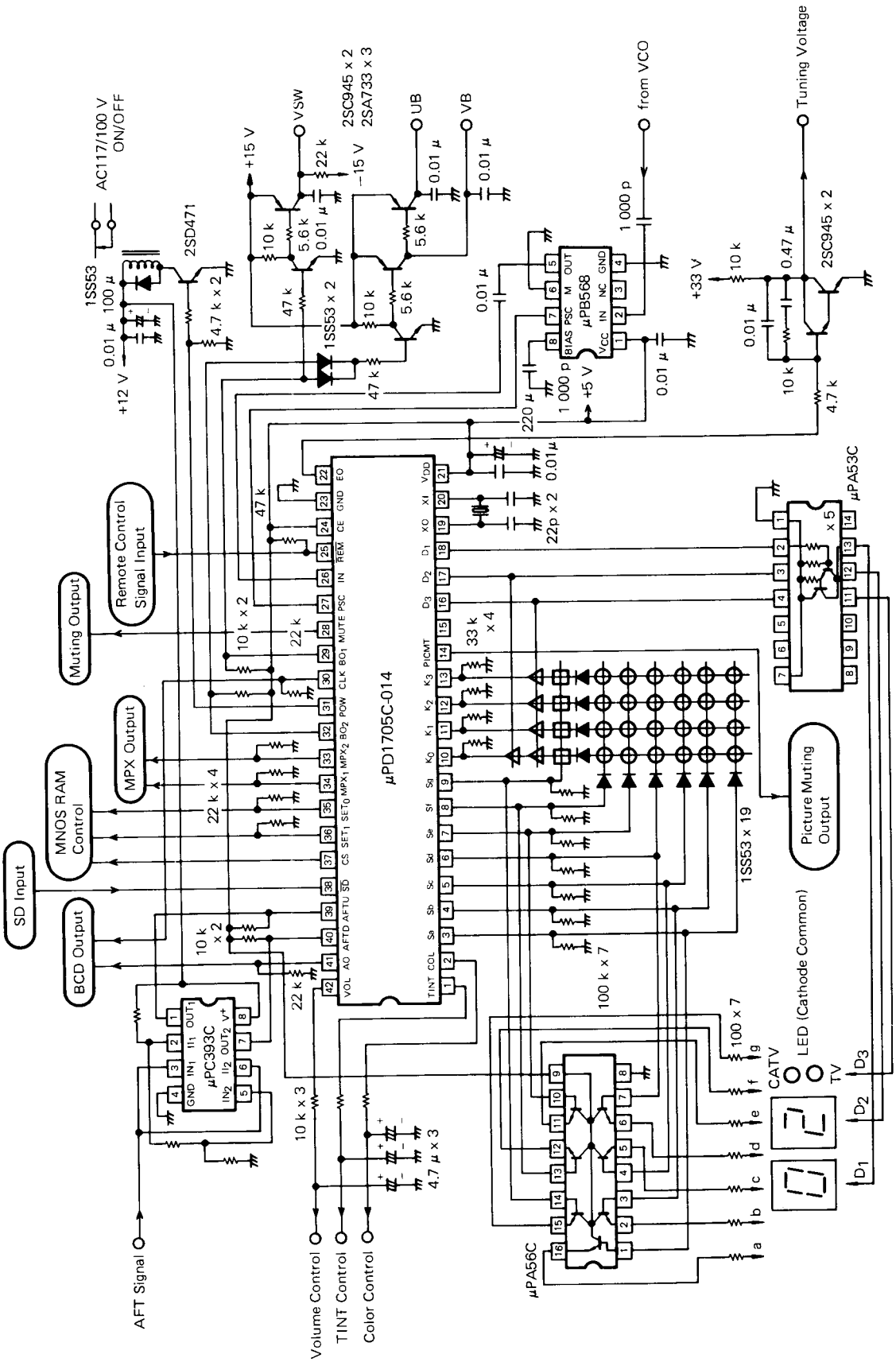
This 8-bit data can also be used as the BCD channel number output for CRT displays. In this case, the 8-bits output and the display timing output (Recall) are connected to the CRT display interface.



OUTPUT PATTERN

NUMERAL	BCD OUTPUT
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1
Blank	1 1 1 1

8. APPLICATION CIRCUIT (105 channels)



The practical circuits and circuit constants shown in this manual have not be designed for mass production (where deviation between parts and temperature characteristics must also be considered). These circuits and circuit constants can only be used after careful consideration has been given.

9. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}	−0.3 to +6.0	V
Input Voltage	V_I	−0.3 to +V_{DD}	V
Output Voltage	V_O	−0.3 to +V_{DD}	V
Output Current	I_O	10	mA
Operating Temperature	T_{opt}	−35 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Output Breakdown Voltage	V_{BDS1}	Sa to Sg pins (between drain source voltage) −35	V
Output Breakdown Voltage	V_{BDS2}	MPX_1, MPX_2, SET_1, SET_0 pins (between drain source voltage) −15	V
Output Breakdown Voltage	V_{BDS3}	BO_1, BO_2 pins (between drain source voltage) +15	V

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
Output Breakdown Voltage	V_{BDS1}			−30	V	Sa to Sg pin (between drain source voltage) I_{OFF} = −5 μA
Output Breakdown Voltage	V_{BDS2}			−11	V	MPX1, MPX2, SET0, SET1 pins (between drain source voltage) I_{OFF} = −10 μA
Output Breakdown Voltage	V_{BDS3}			13	V	BO_1, BO_2 pins (between drain source voltage) I_{OFF} = 5 μA
Supply Voltage Rise Time	T_{rise}			500	ms	V_{DD} = 0 → 4.5 V

DC CHARACTERISTICS (V_{DD} = +4.5 to +5.5 V, T_a = −35 to +75 °C)

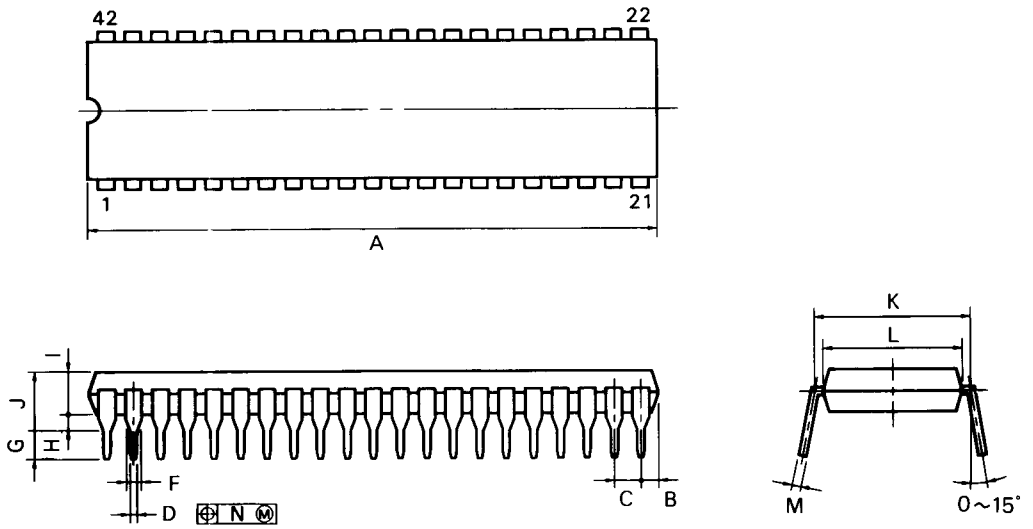
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High Level Input Voltage	V_{IH1}	0.8V_{DD}		V_{DD}	V	$\overline{REM}$ pin
High Level Input Voltage	V_{IH2}	0.7V_{DD}		V_{DD}	V	AFTU, AFTD, $\overline{SD}$, CE pins
High Level Input Voltage	V_{IH3}	0.6V_{DD}		V_{DD}	V	K_0 to K_3 pins
Low Level Input Voltage	V_{IL1}	0		0.3V_{DD}	V	AFTU, AFTD, $\overline{SD}$, CE pins
Low Level Input Voltage	V_{IL2}	0		0.2V_{DD}	V	K_0 to K_3, $\overline{REM}$ pins
High Level Output Voltage	V_{OH1}	4.0			V	EO, VOL, COL, TINT pins. I_{OH} = −0.5 mA
High Level Output Voltage	V_{OH2}	4.0			V	D_1 to D_5, MUTE, PSC, CS pins. I_{OH} = −0.2 mA
High Level Output Voltage	V_{OH3}	3.0			V	Sa to Sg pins. I_{OH} = −0.5 mA
High Level Output Voltage	V_{OH4}	2.5			V	MPX_1, MPX_2, SET_0, SET_1, CLK, POW, AO pins. I_{OH} = −2.0 mA
Low Level Output Voltage	V_{OL1}			0.5	V	EO, VOL, COL, TINT, CS pins. I_{OL} = 0.5 mA
Low Level Output Voltage	V_{OL2}			0.5	V	D_1 to D_5, MUTE, PSC pins. I_{OL} = 0.2 mA
Low Level Output Voltage	V_{OL3}			2.0	V	BO_1, BO_2 pins. I_{OL} = 2.0 mA
High Level Input Current	$+I_{IH1}$	10	40	100	μA	K_0 to K_3 pins. $V_{IN} = V_{DD}$ = 5 V
High Level Input Current	$+I_{IH2}$		300		μA	XI pin (when pulled down). $V_{IN} = V_{DD}$ = 5.0 V
Low Level Input Current	$-I_{IL}$		300		μA	IN pin (when pulled up), V_{IN} = 0, V_{DD} = 5 V
High Level Input Leakage Current	$+I_{LIH}$			10	μA	CE, $\overline{REM}$, AFTU, AFTD, $\overline{SD}$ pins. $V_{IN} = V_{DD}$ = 5.0 V
Low Level Input Leakage Current	$-I_{LIL}$			10	μA	CE, $\overline{REM}$, AFTU, AFTD, $\overline{SD}$, K_0 to K_3 pins. V_{IN} = 0 V
Output Leakage Current	I_L		10^{-3}	1	μA	EO pin. $V_O = V_{DD}$, V_O = 0 V
Operating Current	I_{DD1}		3		mA	Normal operation (excluding display current)
Operating Current	I_{DD2}		0.6		mA	CE pin = 0, V_{DD} = 5 V
Oscillation Stop Current	V_{DDS}		3.2	3.8	V	

AC CHARACTERISTICS (V_{DD} = +4.5 to +5.5, T_a = −35 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Operating Frequency	fin	0.5		8.8	MHz	IN pin, V_{IN} = 0.7 Vp-p (MIN.), DC cut

10. PACKAGE DIMENSION (Unit: mm)

42-pin plastic DIP (600 mil)



P42C-100-600A,B

NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	55.88 MAX.	2.200 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	$3.6^{\pm 0.3}$	$0.142^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01