

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P107 is a tiny microcontroller composed of a ROM with 1K-byte capacity, a RAM with 16-word capacity and 11 I/O ports. It is a product developed by replacing the on-chip mask ROM of the μPD17107 with the one-time PROM.

The μPD17P107CX, which is writable only once, and the μPD17P107GS are available. They are convenient for evaluating or producing in small quantities the μPD17107.

Very efficient programming is possible due to the μPD17000 architecture incorporating the general-purpose register system, which allows the data memory to be manipulated directly, being adopted in the CPU. Every instruction is composed of 1 word of 16-bit length.

FEATURES

- μPD17107 compatible
- Program memory (one-time PROM): 1K byte (512 words × 16 bits)
- Data memory (RAM): 16 words × 4 bits
- I/O ports: 11 ports (N-ch open-drain output 3 ports)
- Instruction execution time: 128 μs (62.5 kHz) to 8 μs (1 MHz)
- Instruction types: 24 types (all 1-word instructions)
- Stack levels: 1 level
- Standby function available (by STOP, HALT instruction)
- Data memory data retainable at low voltage (MIN. 2.0 V)
- With on-chip system clock oscillator (only resistor externally provided)
- Operating supply voltage: 2.5 to 6.0 V (at 250 kHz)
4.5 to 6.0 V (at 1 MHz)

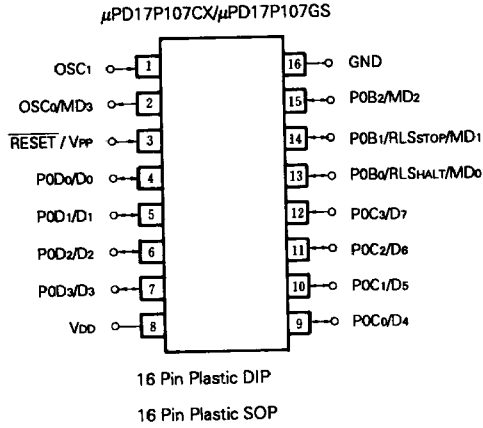
APPLICATIONS

- Electronic control of home electric appliances, TOY, etc.

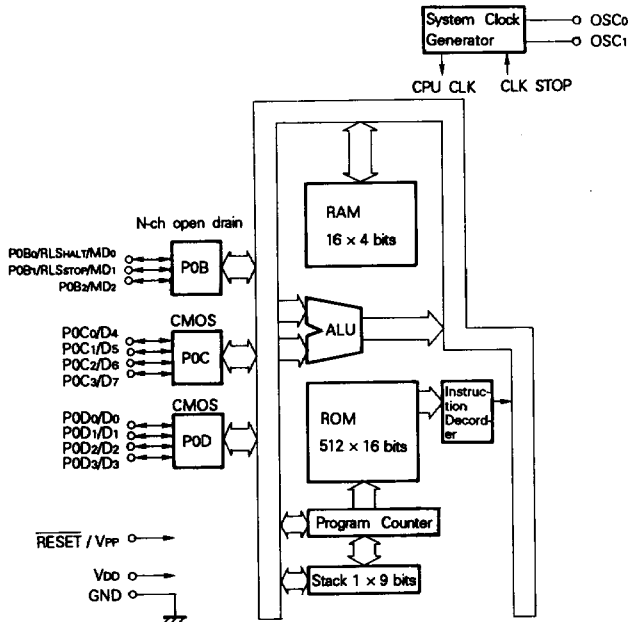
ORDERING INFORMATION

Order Code	Package
μPD17P107CX	16-pin plastic DIP (300 mil)
μPD17P107GS	16-pin plastic SOP (300 mil)

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



PIN FUNCTIONS

PIN FUNCTION LIST

- Port pins

Pin Name	Input/ Output	Dual-Function Pin		Function	Program Memory Write/Verify Mode	Reset
		RLSHALT	MD ₀			
P0B ₀	Input/ Output	RLSHALT	MD ₀	• N-ch open-drain 4-bit input/ output port (Port 0B)	Mode setting pin	High imped- ance (input mode)
P0B ₁		RLSSTOP	MD ₁			
P0B ₂		MD ₂				
P0C ₀	Input/ Output	D ₄		• CMOS (push-pull) 4-bit input/output port (Port 0C)	8-bit data input/ output pin (high-order 4 bits)	High imped- ance (input mode)
P0C ₁		D ₅				
P0C ₂		D ₆				
P0C ₃		D ₇				
P0D ₀	Input/ output	D ₀		• CMOS (push-pull) 4-bit input/output port (Port 0D)	8-bit data input/ output pin (low- order 4 bits)	High imped- ance (input mode)
P0D ₁		D ₁				
P0D ₂		D ₂				
P0D ₃		D ₃				

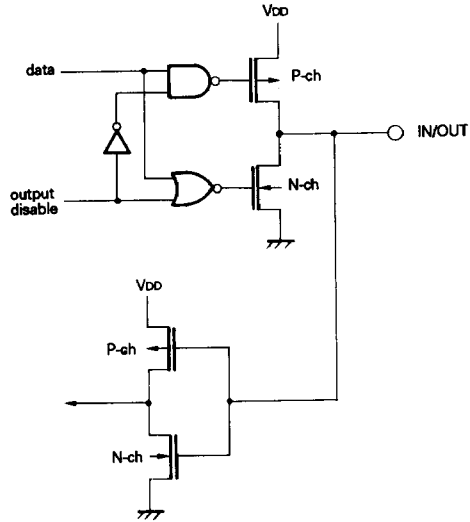
- Other than port pins

Pin Name	Input Output	Dual- Function Pin	Function	Program Memory Write/Verify Mode
RESET	Input	V _{PP}	System reset input pin	Voltage impression pin (+12.5 V)
V _{DD}			Positive power pin	Positive power pin (+6.0 V)
GND			GND pin	GND pin
OSC ₁			System clock oscillation resonator connection pin	Program memory address update
OSC ₀		MD ₃	System clock oscillation resonator connection pin	Mode setting pin

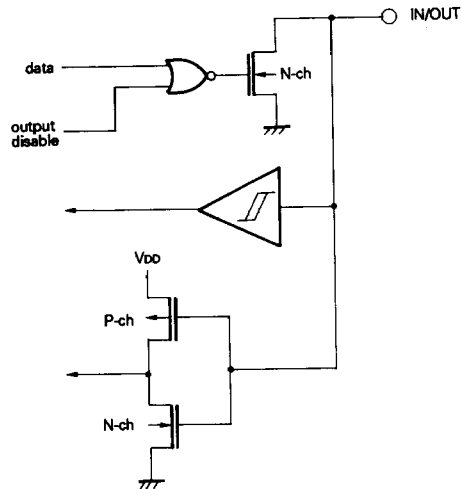
PIN INPUT/OUTPUT CIRCUITS

The μPD17P107 pin input/output circuit diagrams are shown below.

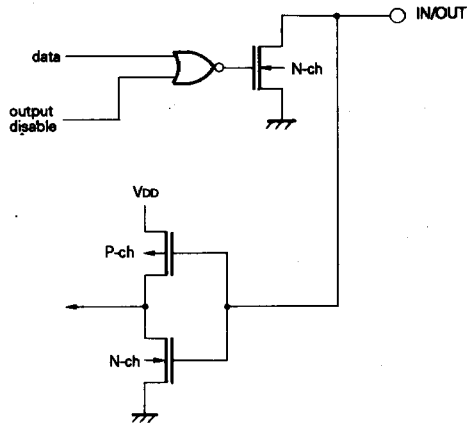
(1) P0C, P0D



(2) P0B₀, P0B₁

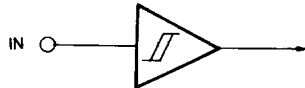


(3) P0Bz



2

(4) $\overline{\text{RESET}}$



μ PD17P107

9. DIFFERENCES BETWEEN μ PD17P107 AND μ PD17107

The μ PD17P107 is a product developed by replacing the program memory of the μ PD17107 with the on-chip mask ROM with the one-time PROM. These 2 models have the same CPU functions and on-chip hardware with the only difference being the program memory and the mask option. Table 9-1 shows the differences between the μ PD17P107 and μ PD17107.

Table 9-1 Differences between μ PD17P107 and μ PD17107

Item	μ PD17P107	μ PD17107
ROM	One-time PROM 512 \times 16 bits	Mask ROM 512 \times 16 bits
P0B ₀ to P0B ₂ pin pull-up resistor	Not available	Mask option
RESET pin pull-up resistor	Not available	Mask option
Connection pin	V _{PP} pin, run mode selection pin available	V _{PP} pin, run mode selection pin not available
Input power	2.5 to 6.0 V (at 250 kHz) 4.5 to 6.0 V (at 1 MHz)	
Package	16-pin DIP 16-pin SOP	

10. ONE-TIME PROM (PROGRAM MEMORY) WRITE AND VERIFY

The μPD17P107's on-chip program memory is a 512 × 16-bit one-time PROM.

To write/verify this one-time PROM, the pins shown in the table below are used. No address input is available. Instead, a system to update the address by the clock input via the OSC₁ pin is adopted.

Pin Name	Function
V _{PP}	Voltage impression pin at program memory write/verify
OSC ₁	Address updating clock input pin at program memory write/verify
MD ₀ to MD ₃	Input pin at program memory write/verify. Used as run mode selection pin.
D ₀ to D ₇	8-bit data input/output pin at program memory write/verify

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10.1 RUN MODE AT PROGRAM MEMORY WRITE/VERIFY

The μPD17P107 assumes the program memory write/verify mode if +6 V is impressed to the V_{DD} pin and +12.5 V is impressed to the V_{PP} pin after the reset status (V_{DD} = 5 V, RESET = 0 V) assumed for a certain period of time. In that mode, the following run mode is entered according to the MD₀ to MD₃ pin setting. All the remaining pins are at the GND potential by the pull-down resistor.

Run Mode Setting						Run Mode
V _{PP}	V _{DD}	MD ₀	MD ₁	MD ₂	MD ₃	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	x	H	H	Program inhibit mode

x: L or H

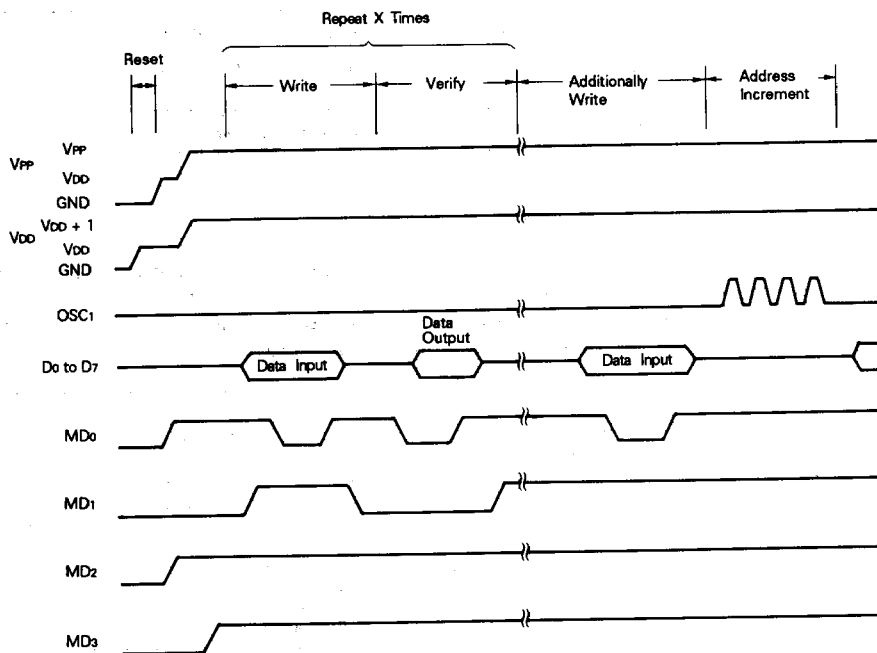
10.2 PROGRAM MEMORY WRITING PROCEDURE

The program memory writing procedure is shown below. High-speed write is possible.

- (1) Pull down the pins not to be used to GND via the resistor. The OSC₁ pin at the low level.
- (2) Supply 5 V to the V_{DD} pin. The V_{PP} pin at the low level.
- (3) Wait 10 μs and then supply 5 V to the V_{PP} pin.
- (4) Set the mode setting pin to the program memory address 0 clear mode.
- (5) Supply 6 V to V_{DD} and 12.5 V to V_{PP}.
- (6) Assume the program inhibit mode.
- (7) Write data in the 1-ms write mode.
- (8) Assume the program inhibit mode.
- (9) Assume the verify mode. If written, go to (10). If not, repeat (7) to (9).

- (10) Additionally write (number of times written in (7) to (9): X) \times 1 ms.
- (11) Assume the program inhibit mode.
- (12) Update (+1) the program memory address by inputting a pulse to the OSC₁ pin 4 times.
- (13) Repeat (7) to (12) up to the last address.
- (14) Assume the program memory address 0 clear mode.
- (15) Change the V_{DD}, V_{PP} pin voltage to 5 V.
- (16) Power off.

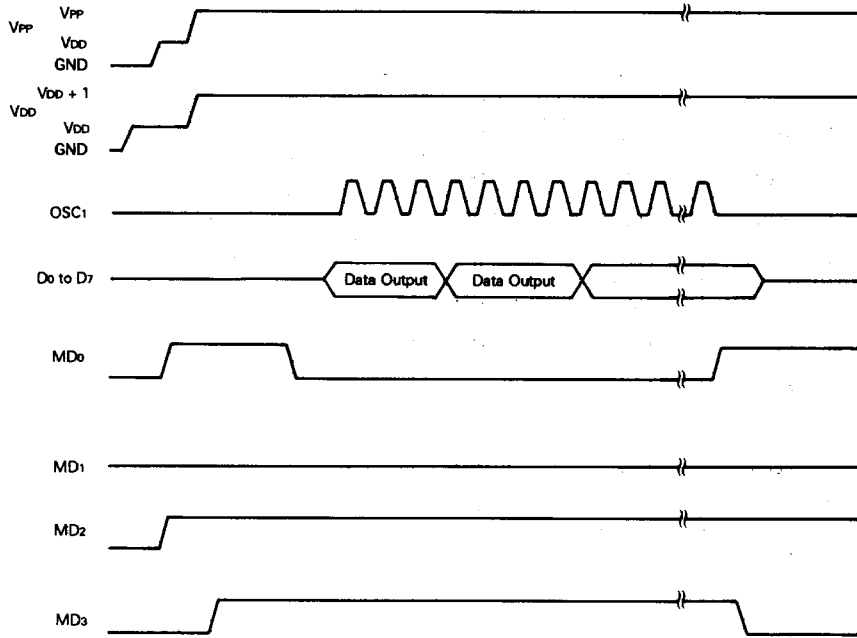
The above procedure of (2) to (12) is shown in the diagram below.



10.3 PROGRAM MEMORY READING PROCEDURE

- (1) Pull down the pins not to be used to GND via the resistor. The OSC₁ pin at the low level.
- (2) Supply 5 V to the V_{DD} pin. The V_{PP} pin at the low level.
- (3) Wait 10 μs and then supply 5 V to the V_{PP} pin.
- (4) Set the mode setting pin to the program memory address 0 clear mode.
- (5) Supply 6 V to V_{DD} and 12.5 V to V_{PP}.
- (6) Assume the program inhibit mode.
- (7) Assume the verify mode. Output data sequentially 1 address at a time at intervals of 4 inputs when a clock pulse is input to the OSC₁ pin.
- (8) Assume the program inhibit mode.
- (9) Assume the program memory address 0 clear mode.
- (10) Change the V_{DD}, V_{PP} pin voltage to 5 V.
- (11) Power off.

The above procedure of (2) to (9) is shown in the diagram below.



11. ASSEMBLER RESERVED WORDS

Table 11-1 lists the reserved symbols defined in the μPD17P107's device file (AS17107).

Table 11-1 Reserved Symbol List

Name	Attribute	Value	R/W	Description
P0B0	FLG	0.71H.0	R/W	Port 0B, bit 0
P0B1	FLG	0.71H.1	R/W	Port 0B, bit 1
P0B2	FLG	0.71H.2	R/W	Port 0B, bit 2
P0B3*	FLG	0.71H.3	R	Value "0" fixed
P0C0	FLG	0.72H.0	R/W	Port 0C, bit 0
P0C1	FLG	0.72H.1	R/W	Port 0C, bit 1
P0C2	FLG	0.72H.2	R/W	Port 0C, bit 2
P0C3	FLG	0.72H.3	R/W	Port 0C, bit 3
P0D0	FLG	0.73H.0	R/W	Port 0D, bit 0
P0D1	FLG	0.73H.1	R/W	Port 0D, bit 1
P0D2	FLG	0.73H.2	R/W	Port 0D, bit 2
P0D3	FLG	0.73H.3	R/W	Port 0D, bit 3
BCD	FLG	0.7EH.0	R/W	BCD operation flag
PSW	MEM	0.7FH	R/W	Program status word
Z	FLG	0.7FH.1	R/W	Zero flag
CY	FLG	0.7FH.2	R/W	Carry flag
CMP	FLG	0.7FH.3	R/W	Compare flag

*: P0B3, which is not available in the μPD17P107, has been registered as a read only flag to be used as a dummy bit when using a built-in macro.

12. INSTRUCTION SETS

12.1 INSTRUCTION SET LIST

b ₁₄ -b ₁₁		b ₁₅		0	1
		BIN	HEX		
0 0 0 0	0	ADD	r, m	ADD	m, #i
0 0 0 1	1	SUB	r, m	SUB	m, #i
0 0 1 0	2	ADDC	r, m	ADDC	m, #i
0 0 1 1	3	SUBC	r, m	SUBC	m, #i
0 1 0 0	4	AND	r, m	AND	m, #i
0 1 0 1	5	XOR	r, m	XOR	m, #i
0 1 1 0	6	OR	r, m	OR	m, #i
0 1 1 1	7	RET			
		RETSK			
		RORC	r		
		STOP	s		
		HALT	h		
		NOP			
1 0 0 0	8	LD	r, m	ST	m, r
1 0 0 1	9	SKE	m, #i	SKGE	m, #i
1 0 1 0	A				
1 0 1 1	B	SKNE	m, #i	SKLT	m, #i
1 1 0 0	C	BR	addr	CALL	addr
1 1 0 1	D			MOV	m, #i
1 1 1 0	E			SKT	m, #n
1 1 1 1	F			SKF	m, #n

12.2 INSTRUCTION LIST

Legend

- M : One of data memory
- m : Data memory address specified by (m_H, m_L) of each bank
- m_H : Data memory address high (row address) : 3 bits
- m_L : Data memory address low (column address) : 4 bits
- R : One of general register specified by $[(RP), r]$
- r : General register address low (column address) : 4 bits
- RP : General register pointer
- PC : Program counter
- SP : Stack pointer
- STACK : Stack specified by (SP)
- i : Immediate data : 4 bits
- n : Bit position : 4 bits
- addr : One of program memory address : 11 bits
- a_H : Program memory address high : 3 bits
- a_M : Program memory address middle : 4 bits
- a_L : Program memory address low : 4 bits
- CY : Carry flag
- CMP : Compare flag
- s : Stop release condition
- h : Halt release condition
- [] : Address of M,R
- () : Contents of M,R

Instruction	Mnemonic	Operand	Function	Operation	Machine Code			
					Op. Code	3-Bit	4-Bit	4-Bit
Add	ADD	r,m	Add memory to register	$R ← (R) + (M)$	0000	m_H	m_L	r
		m,#i	Add immediate data to memory	$M ← (M) + i$	1000	m_H	m_L	i
	ADDC	r,m	Add memory to register with carry	$R ← (R) + (M) + (CY)$	0010	m_H	m_L	r
		m,#i	Add immediate data to memory with carry	$R ← (M) + i + (CY)$	1010	m_H	m_L	i
Subtraction	SUB	r,m	Subtract memory from register	$R ← (R) - (M)$	0001	m_H	m_L	r
		m,#i	Subtract immediate data from memory	$M ← (M) - i$	1001	m_H	m_L	i
	SUBC	r,m	Subtract memory from register with borrow	$R ← (R) - (M) - (CY)$	0011	m_H	m_L	r
		m,#i	Subtract immediate data from memory with borrow	$M ← (M) - i - (CY)$	1011	m_H	m_L	i
Compare	SKE	m,#i	Skip if memory equal to immediate data	$M = i$, skip if zero	0100	m_H	m_L	i
	SKGE	m,#i	Skip if memory greater than or equal to immediate data	$M = i$, skip if not borrow	1100	m_H	m_L	i
	SKLT	m,#i	Skip if memory less than immediate data	$M = i$, skip if borrow	1101	m_H	m_L	i
	SKNE	m,#i	Skip if memory not equal to immediate data	$M = i$, skip if not zero	0101	m_H	m_L	i
Logic operation	AND	m,#i	Logical AND of memory and immediate data	$M ← (M) AND i$	10100	m_H	m_L	i
		r,m	Logical AND of register and memory	$R ← (R) AND (M)$	00100	m_H	m_L	r
	OR	m,#i	Logical OR of memory and immediate data	$M ← (M) OR i$	10110	m_H	m_L	i
		r,m	Logical OR of register and memory	$R ← (R) OR (M)$	00110	m_H	m_L	r
XOR	m,#i	Logical XOR of memory and immediate data	$M ← (M) XOR i$	10101	m_H	m_L	i	
	r,m	Logical XOR of register and memory	$R ← (R) XOR (M)$	00101	m_H	m_L	r	
Transfer	LD	r,m	Load memory of register	$R ← (M)$	01000	m_H	m_L	r
	ST	m,r	Store register to memory	$(M) ← R$	11000	m_H	m_L	r
	MOV	m,#i	Move immediate data to memory	$M ← i$	11101	m_H	m_L	i
Judge	SKT	m,#n	Test memory bits, then skip if all bits specified are true	$CMP ← 0$ skip if $M_n = \text{all "1"}$	11110	m_H	m_L	n
	SKF	m,#n	Test memory bits, then skip if all bits specified are false	$CMP ← 0$ skip if $M_n = \text{all "0"}$	11111	m_H	m_L	n

Instruction	Mne-monic	Oper-and	Function	Operation	Machine Code			
					Op.-Code	3-Bit	4-Bit	4-Bit
Branch	BR	addr	Jump to the address	PC←ADDR	01100	a _H	a _M	a _L
	RORC	r	Rotate register right with carry	(CY)→(R)→CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP←(SP)−1 STACK←((PC)+1). PC←ADDR	11100	a _H	a _M	a _L
	RET		Return to main routine from subroutine	PC←(STACK).SP←(SP)+1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditional	PC←(STACK).SP←(SP)+1 and skip	00111	001	1110	0000
Other	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU, restart by condition h	HALT	00111	011	1111	h
	NOF		No operation	No Operation	00111	100	1111	0000

13. ELECTRIC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V _{DD}		-0.3 to +7.0	V	
Supply Voltage	V _{FP}		-0.3 to +13.5	V	
Input Voltage	V _I	P0C, P0D, RESET	0.3 to V _{DD} +0.3	V	
		P0B	-0.3 to +11	V	
Output Voltage	V _O	P0C, P0D	0.3 to V _{DD} +0.3	V	
		P0B	-0.3 to +11	V	
High-level Output Amperage	I _{OH}	P0B, P0C, P0D per pin	-5	mA	
		Total for all pins	-15	mA	
Low-level Output Amperage	I _{OL}	P0B, P0C, P0D per pin	30	mA	
		Total for all pins	100	mA	
Operating Temperature	T _{opt}		-40 to +85	°C	
Storage temperature	T _{stg}		-65 to +150	°C	
Power Dissipation	P _d	T _a = 85 °C	16 pin DIP	400	mW
			16 pin SOP	190	mW

CAPACITY (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacity	C _{IN}			15	pF	f = 1 MHz, 0 V at other than measured pins
Input/Output Capacity	C _{IO}			15	pF	

DC CHARACTERISTICS (T_a = -40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-level Input Voltage	V _{IH1}	0.7 V _{DD}		V _{DD}	V	Other than specified below.	
	V _{IH2}	0.8 V _{DD}		V _{DD}	V	P0B, RESET	
	V _{IH3}	0.8 V _{DD}		9	V	P0B*	
	V _{IH4}	V _{DD} - 0.5		V _{DD}	V	OSC ₁	
Low-level Input Voltage	V _{IL1}	0		0.3 V _{DD}	V	Other than specified below.	
	V _{IL2}	0		0.2 V _{DD}	V	P0B, RESET	
	V _{IL3}	0		0.5	V	OSC ₁	
P0C, D High-level Output Voltage	V _{OH}	V _{DD} - 2.0			V	V _{DD} = 4.5 to 6.0 V I _{OH} = -2 mA	
		V _{DD} - 1.0			V	I _{OH} = -200 μA	
P0B, C, D Low-level Input Voltage	V _{OL}			2.0	V	V _{DD} = 4.5 to 6.0 V I _{OL} = 15 mA	
				0.5	V	I _{OL} = 600 μA	
P0B, C, D High-level Input Leak Current	I _{IH1}			5	μA	V _{IN} = V _{DD}	
				10	μA	V _{IN} = 9 V*	
P0B, C, D Low-level Input Leak Current	I _{IL}			-5	μA	V _{IN} = 0 V	
P0B, C, D High-level Output Leak Current	I _{LOH1}			5	μA	V _{OUT} = V _{DD}	
				10	μA	V _{OUT} = 9 V*	
P0B, C, D Low-level Output Leak Current	I _{LOL}			-5	μA	V _{OUT} = 0 V	
Supply Amperage	I _{DD1}		0.4	1.2	mA	Run mode	V _{DD} = 5 V ±10 % f _{CC} = 1.0 MHz ±20 %
			50	150	μA		V _{DD} = 3 V ±10 % f _{CC} = 250 kHz ±20 %
	I _{DD2}		0.3	0.9	mA	HALT mode	V _{DD} = 5 V ±10 % f _{CC} = 1.0 MHz ±20 %
			40	120	μA		V _{DD} = 3 V ±10 % f _{CC} = 250 kHz ±20 %
	I _{DD3}		0.1	10	μA	STOP mode	V _{DD} = 5 V ±10 %
			0.1	5	μA		V _{DD} = 3 V ±10 %

*: If N-ch open-drain input/output selected.

μPD17P107

LOW-SUPPLY VOLTAGE DATA HOLDING CHARACTERISTICS IN DATA MEMORY STOP MODE (T_a = -40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data Holding Supply Voltage	V _{DDDR}	2.0		6.0	V	
Data Holding Supply Amperage	I _{DDDR}		0.1	5.0	μA	V _{DDDR} = 2.0 V
Release Signal Set Time	t _{SREL}	0			μs	

AC CHARACTERISTICS (T_a = -40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Internal Clock Cycle Time	T _{cy}	6.6		160	μs	V _{DD} = 4.5 to 6.0 V
		26.6		160	μs	
POB ₀ , POB ₁ , High/Low Level Width	T _{PBH} T _{PBL}	10			μs	
RESET, High/Low Level Width	T _{RSH} T _{RSL}	10			μs	

DC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High-Level Input Voltage	V _{IH1}	0.7 V _{DD}		V _{DD}	V	Other than OSC ₁
	V _{IH2}	V _{DD} - 0.5		V _{DD}	V	OSC ₁
Low-Level Input Voltage	V _{IL1}	0		0.3 V _{DD}	V	Other than OSC ₁
	V _{IL2}	0		0.4	V	OSC ₁
Input Leak Current	I _{LI}			10	μA	V _{IN} = V _{IL} or V _{IH}
High-Level Output Voltage	V _{OH}	V _{DD} - 1.0			V	I _{OH} = -1 mA
Low-Level Output Voltage	V _{OL}			0.4	V	I _{OL} = 1.6 mA
V _{DD} Supply Current	I _{DD}			30	mA	
V _{PP} Supply Current	I _{PP}			30	mA	MD0 = V _{IL} , MD1 = V _{IH}

NOTE 1: V_{PP} must not be a minimum of +13.5 V including overshoot.

2: Impress V_{DD} before V_{PP} and break it after V_{PP}.

AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

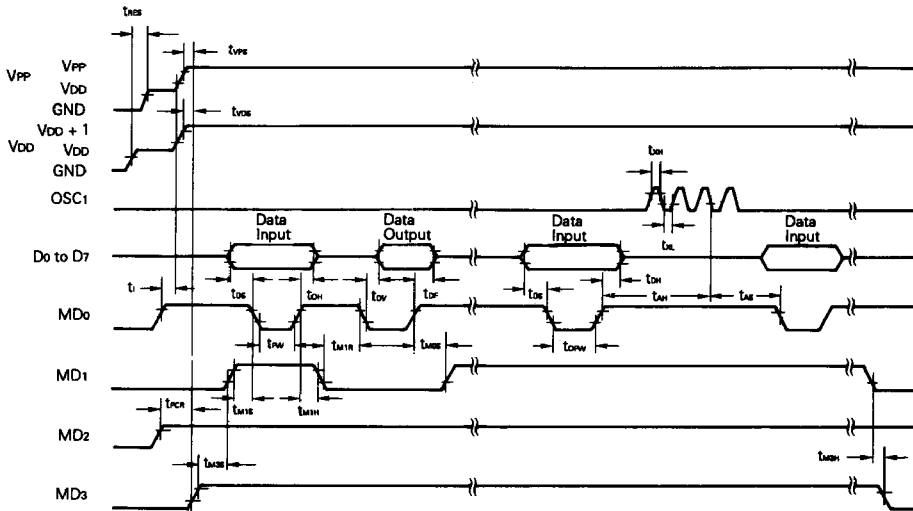
CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITION
Address Set-Up Time *2 (for MD0 ↓)	t _{AS}	t _{AS}	2			μs	
MD1 Set-Up Time (for MD0 ↓)	t _{M1S}	t _{OES}	2			μs	
Data Set-Up Time (for MD0 ↓)	t _{DS}	t _{DS}	2			μs	
Address Hold Time *2 (for MD0 ↑)	t _{AH}	t _{AH}	2			μs	
Data Hold Time (for MD0 ↑)	t _{DH}	t _{DH}	2			μs	
MD0 ↑ → Data Output Float Delay Time	t _{DF}	t _{DF}	0		130	ns	
V _{PP} Set-Up Time (for MD3 ↑)	t _{VPS}	t _{VPS}	2			μs	
V _{DD} Set-Up Time (for MD3 ↑)	t _{VDS}	t _{VCS}	2			μs	
Initial Program Pulse Width	t _{PW}	t _{PW}	0.95	1.0	1.05	ms	

CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITION
Additional Program Pulse Width	t _{OPW}	t _{OPW}	0.95		21.0	ms	
MD0 Set-Up Time (for MD1 ↑)	t _{MOS}	t _{CES}	2			μs	
MD0 ↓ → Data Output Delay Time	t _{OV}	t _{OV}			1	μs	MD0 = MD1 = V _{IL}
MD1 Hold Time (for MD0 ↑)	t _{M1H}	t _{BEH}	2			μs	t _{M1H} + t _{M1R} ≥ 50 μs
MD1 Recover Time (for MD0 ↓)	t _{M1R}	t _{OR}	2			μs	
Program Counter Reset Time	t _{PCR}	-	10			μs	
OSC ₁ Input High/Low Level Width	t _{XH} t _{XL}	-	0.42			μs	
OSC ₁ Input Frequency	f _{OSC}	-			1.2	MHz	
Initial Mode Set Time	t _I	-	2			μs	
MD3 Set-Up Time (for MD1 ↑)	t _{M3S}	-	2			μs	
MD3 Hold Time (for MD1 ↓)	t _{M3H}	-	2			μs	
MD3 Set-Up Time (for MD0 ↓)	t _{M3SR}	-	2			μs	At program memory read
Address *2 → Data Output Delay Time	t _{DAD}	t _{ACC}	2			μs	At program memory read
Address *2 → Data Output Hold Time	t _{HAD}	t _{OH}	0		130	ns	At program memory read
MD3 Hold Time (for MD0 ↑)	t _{M3HR}	-	2			μs	At program memory read
MD3 ↓ → Data Output Float Delay Time	t _{DFR}	-	2			μs	At program memory read
Reset Set-Up Time	t _{RES}		10			μs	

*1: A symbol of the corresponding μPD27C256.

*2: The internal address signal is incremented (+1) at the 3rd OSC₁ input falling and is not connected to a pin.

PROGRAM MEMORY WRITING TIMING



PROGRAM MEMORY READING TIMING

