VOLTAGE SYNTHESIZER SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The 4-bit CMOS microcomputer μPD1730 designed for digital tuning purposes is capable of direct LED connections, and features a built-in D/A converter for voltage synthesizer applications.

The CPU functions include 4-bit parallel addition and subtraction (AD, SU instructions, etc.), logical operations (EXL instruction, etc.), multiple bit test (TMT instruction, etc.), CARRY F/F setting and resetting (STC instruction, etc.), interrupt, and timer functions.

This 30-pin shrink DIP (Dual In-line Package) includes I/O (Input/Output) ports controlled by a powerful set of input and output instructions (IN, OUT instructions, etc.), a 6-bit D/A converter, and a 4-bit A/D converter.

The A/D converter can be used as an S-curve input pin during auto fine tuning (AFT) when the device is used in TV applications.

FEATURES

- 4-bit microcomputer for digital tuning applications
- Built-in 13-bit D/A converter for voltage synthesizers
- 5 V ± 10 % single source power supply
- CMOS low power consumption
- Simple back-up of data memory (RAM) (using CE pin)
- Program memory (ROM): 16 bits x 1008 steps
- Data memory (RAM): 4 bits x 48 words
- Powerful set of 67 instructions (all 1-word instructions)
- Instruction execution time of 33.3 μsec (when connected to 4.5 MHz ceramic resonator)
- Wide range of addition and subtraction instructions (12 addition and 12 subtraction instructions)
- Powerful composite judgement instructions (TMT, TMF instructions, etc.)
- Storage-to-storage transfer at same row address
- Indirect transfer between registers MVRD, MVRS instructions, etc.)
- Powerful set of 16 general registers (located in RAM space)
- Stack level: 1 level
- Instruction controlled stop watch capability (supply current 10 μA MAX.)
- 14 powerful I/O ports (PA_0 to PA_3: 1-bit unit input and output settings, PB_0 to PB_3: group input and output settings, PC_1 to PC_3, PM_1, PM_2: output-only port, RS: input-only port)
- Direct LED drive capability (segments only, N-channel open-drain 12 V, 40 mA MAX.)
- Built-in 6-bit D/A comparator
- Built-in 4-bit A/D comparator
- Built-in horizontal synchronizing signal detector circuit
- Manual tuning with externally connected variable registance (to vary tuning D/A output)

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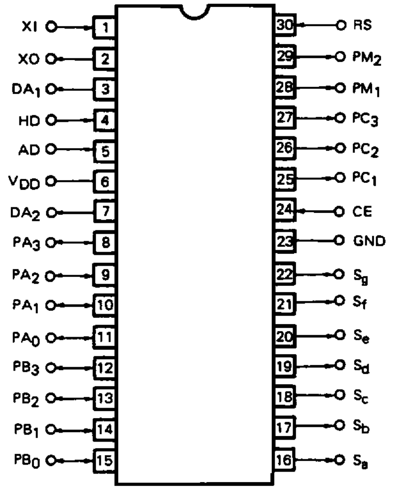
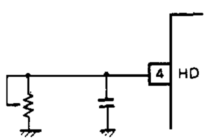
ORDERING INFORMATION

Order Code	Package
μPD1730CT-XXX	30-pin plastic shrink DIP (400 mil)

PIN CONFIGURATION (Top View)



PIN DESCRIPTION

PIN NO.	SYMBOL	NAME	DESCRIPTION	OUTPUT TYPE
1 2	XI XO	Ceramic Resonator	Ceramic resonator connector pin. Use a 4.5 MHz resonator. Use a quartz crystal resonator in applications (such as clocks) where precision is required.	Input (XI) CMOS push-pull (XO)
3	DA_1	Tuning D/A Comparator Output	Voltage synthesizer 13-bit D/A (Digital to Analog) converter output pin. Since a combined 8-bit PWM (Pulse Width Modulation) and 5-bit RMP (Rate Multiplier) is used as the conversion method, integration with a simple CR filter is possible. The output is switched to high level when reset by switching the power on (V_{DD}: Low → High) and when the clock is stopped.	CMOS push-pull
4	HD	Horizontal Synchronizing Signal input	Horizontal synchronizing signal detector pin. When in HD mode, the PM_3 internal port is set if the input frequency applied to this pin is between 14.832 and 16.480 kHz, but is reset if outside this range. This HD pin can also be connected to a potentiometer circuit used for tuning purposes (VR mode). Connecting a capacitor and variable resistor to this pin when in VR mode enables direct control of the tuning 13-bit D/A converter (DA_1 pin) by the variable resistor. Connect the circuit as shown in the following diagram.  HD and VR modes are selected by the PG_0 internal port (PG_0 = 1: VR mode, PG_0 = 0: HD mode).	Input
5	AD	A/D Converter Input	A/D (Analog to Digital) converter input. The built-in 4-bit A/D converter connected internally to this pin is a programmed successive comparison type. The A/D converter reference voltage is V_{DD} (5 V ± 10 %).	Input
6	V_{DD}	Power Supply	The μPD1730's power supply pin. A 5 V ± 10 % voltage is supplied during device operations, but this can be lowered to 2.5 V during internal data memory (RAM) hold status (following execution of the CKSTP instruction). The device is reset when the voltage applied to this pin is changed from 0 to 4.5 V (power ON reset), and the program is started from address 0 (see Section 1.5 "TIMER F/F").	–
7	DA_2	D/A Converter Output	6-bit D/A converter output pin. Since output pulses are generated by a 1.4 kHz rate multiplier (RMP) method, the output voltage can be divided into 64 levels when passed a CR integrating circuit. A low level output is generated by power ON reset (V_{DD}: Low → High) and when the clock is stopped.	CMOS push-pull

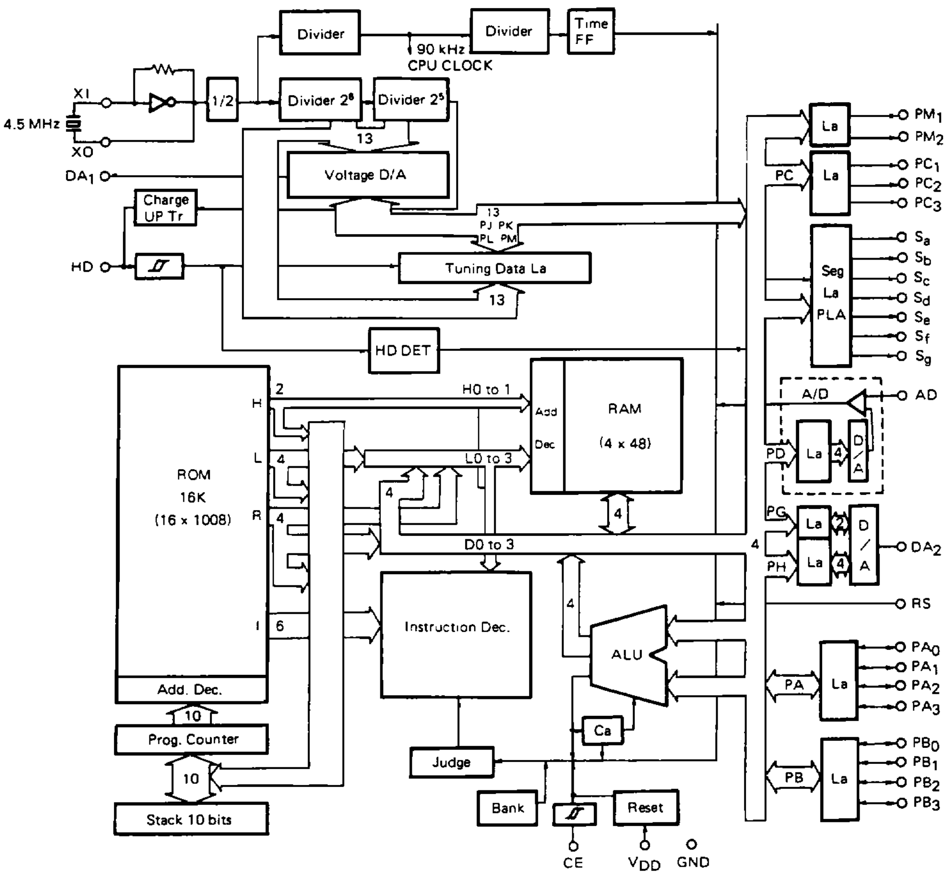
PIN NO.	SYMBOL	NAME	DESCRIPTION	OUTPUT TYPE
8 to 11	PA_3 to PA_0	Port A	4-bit input/output port. This port can be specified "input" or "output" one bit at a time. This designation is executed according to the contents of address 1FH of a data memory (RAM) called the PAIO word (see Notes 1 and 2).	CMOS push-pull (I/O)
12 to 15	PB_3 to PB_0	Port B	4-bit input/output port. This port can be set to 4-bit input port by executing an input instruction (IN instruction), or to 4-bit output port by executing an output instruction (OUT, SPB or RPB instruction). (See Notes 1 and 2.)	CMOS push-pull (I/O)
16 to 22	Sa to Sg	Segment Signal Output	Display segment signal output pins. The memory contents at any address in the data memory (RAM) can be loaded into the segment PLA (Programmable Logic Array) by the SEG instruction, and passed to these pins via that segment PLA. The segment PLA can specify 32 different patterns. (See Section 5, "SEGMENT PLA".) These pins can also be used as the key return signal source for the key matrix. Since the output format is N-channel open-drain, pull-up resistance is required. The segment signal outputs are switched to high level (pull-up potential) when the CE pin is changed to low level.	N-channel open-drain
23	GND	Ground	The device's ground pin.	–
24	CE	Chip Enable	Device selector signal input pin. This pin is switched to high level for normal operations, but to low level when the device is not being used. Switching this CE pin to low level results in the segment signal outputs (Sa to Sg) being switched off and left at the pull-up potential (without effecting DA_1, DA_2, port A, port B, port C, and port M). Note, however, that inputs of less than 134 μsec are not accepted. If the CKSTP instruction being used by a program is executed while the CE pin is at low level, the internal clock generator and CPU stop operating to enable a memory (RAM) hold state where the consumption current is low (less than 250 μA). When the CE pin is switched from low to high level, the device is reset, and the program is started from address 0. (See Section 1.5, "TIMER F/F".)	Input
25 to 27	PC_1 to PC_3	Port C	3-bit output port (see Notes 1 and 3.)	CMOS push-pull
28 29	PM_1 PM_2	Port M	2-bit output port. Since this is an N-channel open-drain output (resistivity of 14 V), an external pull-up resistance is required. (See Notes 1 and 3.)	N-channel open-drain
30	RS	Remote Control Signal Input	1-bit input port. The status of this pin can be checked directly by using the TRS instruction. A remote control input signal is applied.	Input

Notes 1: In port operation instructions (input/output, test port, and set/reset instructions), PB_0 corresponds to the least significant bit of the register or operand data, and PB_3 corresponds to the most significant bit. The same applies to PA, PC, and PM.

2: All input/output ports (PA and PB) are switched to input mode when the device is reset (V_{DD} and CE switched from low to high level) or when the CKSTP instruction is executed.

3: Output-only ports (PC and PM) are changed to high impedance state when the device is reset (but only when V_{DD} is switched from low to high level) or when the CKSTP instruction is executed.
Note that when CE alone is switched from low to high level, the previous state is maintained without the ports being switched to high impedance. But if CE is switched from low to high level after V_{DD} has been changed from low to high level or the CKSTP instruction has been executed, these output ports are switched to high impedance.

μPD1730 BLOCK DIAGRAM



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1. CPU

1.1 PROGRAM COUNTER (PC)

The program counter used to address the program memory (ROM) (that is, programs) is a 10-bit binary counter.

PC_9	PC_8	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0

10 bits

The program counter is normally incremented by one each time an instruction is executed. But when a jump or subroutine call instruction is executed, the address specified in the operand is loaded. And when a skip instruction (e.g. ADS, TMT or RTS instructions) is executed, address of the next instruction after that is loaded irregardless of the skip conditions. If there are conditions to be skipped in this case, the next instruction after the skip instruction is regarded as NOP (no-operation).

That is, NOP is executed and the address of the next instruction after that is specified.

1.2 STACK REGISTER (SR)

The stack register is a 1 x 10 bits register used to store the program counter contents incremented by +1 when a subroutine call instruction is executed (that is, the 10-bit return address). The stack register contents are loaded into the program counter by executing a return instruction (RT or RTS). This is followed by a return to the main program flow.

1.3 PROGRAM MEMORY (ROM)

This 16 bits x 1008 steps ROM is used for program storage. The ROM address range available for use consists of the 1008 steps from 000H to 3EFH.

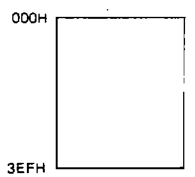


Fig. 1-1 ROM Configuration

1.4 DATA MEMORY (RAM)

The 4-bit x 48 words RAM is normally used to store data. The section from address 00H thru 0FH known as the general register can be used in transfers and in arithmetic operations with the memory. It can also be used as an ordinary memory.

Address 1FH (called the PAIO word) is used in specifying port A (PA_0 to PA_3) as input or output.

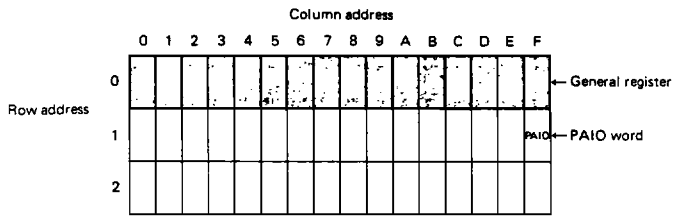


Fig. 1-2 RAM Configuration

1.5 TIMER F/F (TM F/F)

The timer F/F is to be set with an 8 Hz (125 ms) signal and reset by the test timer instruction (TTM instruction). This timer F/F is automatically set every 125 ms so that it can be used to count the clock (one second by 8 counts) or the mute time.

Since the timer F/F can be reset only by the execution of TTM instruction **this instruction must be executed within the period of 125 ms under any circumstance.** When this instruction is executed within a period of 125 ms or more, the timer F/F fails to count up the clock and becomes unable to control the correct time.

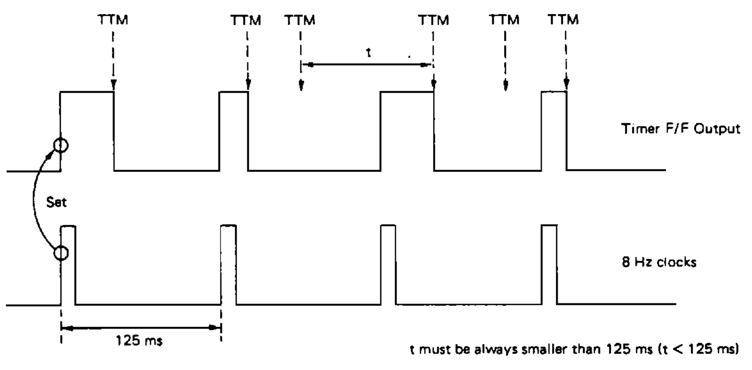


Fig. 1-3 Execution Timing of TTM Instruction

This timer F/F can be also used to judge the detection of power failure. It is reset when V_{DD} changes from low to high or it is set again by the execution of CKSTP instruction or when CE changes from low to high.(Note 3) Fig. 1-4 shows the status transition diagram illustrating the aforementioned relations.

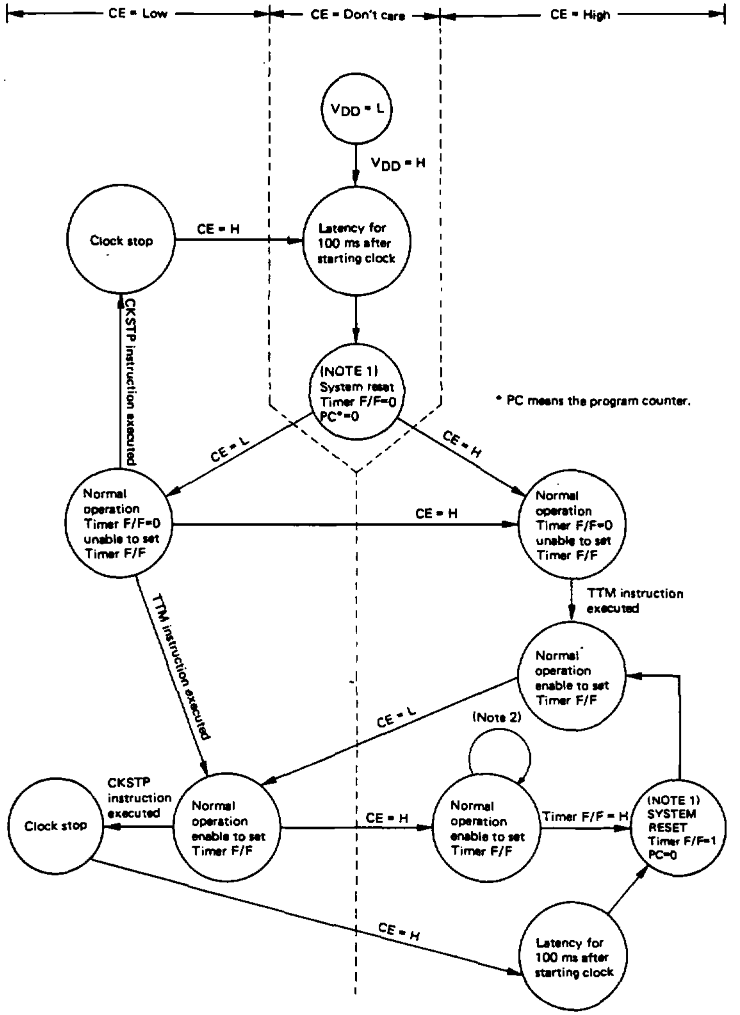


Fig. 1-4 Changes in CPU Status due to CE Pin Status

Note 1: The following operations are done under the system reset status:
① The program counter is reset to address 0.
② BANK F/F is reset (BANK0).
③ I/O port becomes the input mode.

Note 2: This loop cannot be exited if the TTM instruction is executed at the same time that the timer F/F is set. In this case, the loop is exited when the timer F/F is next executed (125 msec later), and the program jumps to address 0 with timer F/F = 1. Note, therefore, that if the TTM instruction is executed periodically, and by chance corresponds with the timer F/F setting cycle (125 msec), the program will never be cleared to address 0.

As apparent from the above illustration, the program starts from the address 0 after the power is turned on (V_{DD} changes from Low to High), no matter what condition the CE pin is held, **while the timer F/F remains reset.** The timer F/F is not set again unless the TTM instruction was once executed (status unable to set the timer F/F). Once the TTM instruction was executed, however, the timer F/F can be set at any time at the intervals of 125 ms each.

If the power is being fed (V_{DD} = high) and the CE pin changes from low to high, the program flow jumps to the address 0 immediately when the timer F/F is set(Note 4). The program therefore starts from the address 0 **while the time F/F remains set.**

As you could understand well from the above explanation, the contents of Timer F/F vary between the time the power failure is recovered (V_{DD} changes from low to high) and the time when the power is continuously fed (V_{DD} =high and CE=low) or when the device is restored from the backed-up condition. Through testing the contents of this timer F/F (i.e. the execution of TTM instruction) it is possible to judge if it is restored from the power failure or from the non-power failure. In other words the power failure can be judged if the execution of TTM instruction, which is executed within 125 ms from the start of program from the address 0, results in 0 (false) or it can be determined as non-power failure (backed-up condition) if the result of test turns to 1 (true).

Care must be also taken to the programming when restoring from the non-power failure (V_{DD}=high and CE changes from low to high) while the clock function of a given program, if provided, needed to be operated (without using the CKSTP instruction) even if CE was low. The program flow in this case jumps to the address 0 immediately after the timer F/F is set. It is therefore necessary to update the clock after executing the TTM instruction to detect the power failure (the execution results in finding true). Otherwise the clock delays by 125 ms each whenever the CE pin changes from low to high.

Note 3: The program starts from the address 0 after the timer F/F was set if CE pin changed from low to high following the execution of CKSTP instruction in case of μPD1730. The timer F/F is reversely reset and the program starts from the address 0 under μPD1701, μPD1703, μPD1704, μPD1710 and μPD1719. It must be noted when executing the CKSTP instruction that the contents of timer F/F differ between μPD1730 and the group of μPD1701, μPD1703, μPD1704, μPD1710 and μPD1719.

Note 4: Even if the CE pin changes from low to high level, the program flow does not move to address 0 when the setting of the timer F/F and the execution of the TTM instruction overlap. If this is the case, the system judges that the timer F/F is set by the TTM instruction execution and the timer F/F is reset. This point must be kept in mind when a power failure detection is done by the TTM instruction. That is, you should know that the TTM instruction has higher priority than the setting of the timer F/F when they overlap. Therefore, the clock does not become incorrect and a misjudging of a power failure does not occur. However, if the TTM instruction execution and the timer F/F setting happen to coincide in the following program, the program does not jump to address 0 forever. (The timer F/F will not be reset.)

```
A:    TTM
      JMP     B
      JMP     A
       :
B:    +-----+ <-------- 3n Step program
      |     |           (n < 1249)
      +-----+
      JMP     A
```

In this example the program executes the normal TTM instruction, skips the next 'JMP B' instruction because the timer F/F is reset, and executes 'JMP A' instruction. Therefore, it cycles this loop. The cycle is 100 μs. (3 steps) The timer F/F is set once every 125 ms and the operations of B are performed. This operations take (3n + 3) steps (multiple of 100 μs). If the CE pin happens to change from low to high level during the TTM instruction execution in this program, operations in B are done due to the judgement that the timer F/F is set by the TTM instruction. However, the timer F/F is set again (125 ms later) when the next TTM instruction is executed because the time interval from the last TTM execution to the next TTM execution is a multiple of 100 μs. Therefore, the timer F/F will not be reset and the program cycles this endless loop. This problem occurs in a program where the TTM instruction is executed in every 125 ms. **If this is the case, change the program so that the TTM instruction is not executed after 125 ms (3750 steps) from the TTM execution.**

1.6 CARRY F/F (C F/F)

The CARRY F/F is normally set when a carry or borrow is generated as the result of executing an arithmetic operation, and reset when no carry or borrow is generated. The CARRY F/F contents remain unchanged if no arithmetic operation instruction is executed. The CARRY F/F can be set and reset directly by the respective carry F/F set and reset instructions (STC and RSC).

1.7 BANK F/F (B F/F)

The BANK F/F is used in port group addressing. The two operand bits of the instruction are also involved in this addressing process (see Section 2, "PORTS"). The bank and corresponding BANK F/F contents are listed in Table 1-1.

Bank designations are executed by the BANK0, BANK1, or BANK2 instruction.

In μPD1700 series devices with a data memory (RAM) of at least 64 words (μPD1704, μPD1706, μPD1707, μPD1708, μPD1710, μPD1711, μPD1712, μPD1713, μPD1714, μPD1715, and μPD1719) the bank is divided into 64-word groups, and designation of these groups is also executed by the same BANK F/F.

Since the μPD1730 RAM has only 48 words, this RAM is BANK0. And this RAM cannot be accessed when not in BANK0 status. Before accessing this RAM, the BANK0 instruction must be executed in advance to set BANK to 0.

When the power is switched on (V_{DD} changed from low to high) or when CE is switched from low to high (that is, when the device is reset), the BANK F/F is reset and BANK0 is specified automatically.

Table 1-1 Bank Designations

BANK	BANK F/F1	BANK F/F0
0	0	0
1	0	1
2	1	0

2. PORTS

The μPD1730 input/output ports are port A (PA_3 to PA_0) and port B (PB_3 to PB_0), and the output ports are port C (PC_3 to PC_1) and port M (PM_2 and PM_1). The internal ports are port D (PD_3 to PD_1), port G (PG_3, PG_2, and PG_0), port H (PH_3 to PH_0), port J (PJ_3 to PJ_0), port K (PK_3 to PK_0), port L (PL_3 to PL_0), and port M (PM_3 and PM_0). Apart from not having externally connected pins, these internal ports are handled in the same way as external ports. That is, the port operation instructions IN, OUT, SPB, and RPB can be used without modification.

Addressing of these ports is achieved by using the two direct addressing bits in the instructions operand, plus the bank F/F bank designation. These port addresses are listed in Table 2-1, and a list of ports is given in Table 2-2.

The same bank designations are used in both port and RAM addressing. Since the RAM is BANK0 in μPD1730, the bank must always be set to 0 for RAM access purposes.

Table 2-1 Port Address

Direct Add.		BANK		
#1	#0	0	1	2
0	0	Port A	—	Port J
0	1	Port B	—	Port K
1	0	Port C	Port G	Port L
1	1	Port D	Port H	Port M

Table 2-2 List of Ports

BANK	Direct Add.	Port	I/O	Function
0	0	PA_0 to PA_3	I/O	General purpose input/output port (I/O can be specified for each bit)
	1	PB_0 to PB_3	I/O	General purpose input/output port
	2	PC_1 to PC_3	O	General purpose output port
	3	PD_0 to PD_3	O	A/D converter comparison data
1	2	PG_0	O	HD pin mode selection (0: HD mode, 1: VR mode)
		PG_2 to PG_3	O	DA_2 (6-bit D/A converter) control data
	3	PH_0 to PH_3	O	
2	0	PJ_0 to PJ_3	I/O	DA_2 (13-bit D/A converter) control data
	1	PK_0 to PK_3	I/O	
	2	PL_0 to PL_3	I/O	
	3	PM_0	I/O	
		PM_1, PM_2	O	General purpose output port
		PM_3	I	Station detection when in HD mode (0: Station tuned, 1: No station)

2.1 PORT A

Port A (PA_3 to PA_0) can be set to input or output in 1-bit steps. Input or output is set by the contents of address 1FH in the data memory (RAM). These contents are called the **PAIO word.** Input port is set by setting the corresponding PAIO word bit to "0", and output port is set by setting "1".

	#3	#2	#1	#0
PAIO Word (Address 1FH)	PA_3	PA_2	PA_1	PA_0

Example 1. Set PA_3 to PA_0 to output ports.

	#3	#2	#1	#0
PAIO Word (Address 1FH)	1	1	1	1

Example 2. Set PA_3 to output port, and PA_2 to PA_0 to input ports.

	#3	#2	#1	#0
PAIO Word (Address 1FH)	1	0	0	0

After Port A has been set to input/output port by PAIO word, an input/output instruction must be executed. And once input or output mode has been set, it is maintained until the PAIO word contents (address 1FH data) are changed.

Example:

```
BANK0
MVI   1FH, 1111B ; Set all port A bits to output port mode
  :
MVI   08H, 1100B ; Set PA3 and PA2 to high level and PA1 and PA0 to low level
OUT   0, 08H     ; Output PA3 and PA2 = high level and PA1 and PA0 = low level
  :
```

Note, however, that port A is automatically set to input port mode when the power is switched on (V_{DD} changed from low to high), when the CKSTP instruction is executed, and when the CE pin is changed from low to high. And pay special attention to the fact that the PAIO word contents may not necessarily match the port A input status at this stage. Port A remains in input mode until the PAIO word contents are set.

When output port mode is set by the PAIO word, the output latch circuit contents are passed directly to the port. Note that the output latch circuit contents are undefined when the power is switched on (V_{DD} changed from low to high), and are held when the clock is stopped.

Therefore, where it is necessary to avoid an undefined output status when output port is first defined by PAIO word, specify output status by the SPB or RPB and OUT instructions before setting the port status.

2.2 PORT B

Port B (PB_3 to PB_0) can be specified input or output as a 4-bit group. All four bits are switched to input port status when an input instruction (IN) is executed, or to output port status when an output instruction (OUT, SPB, or RPB) is executed. That is, input/output mode can be switched by executing input and output instructions.

Data specified by the OUT instruction is output from port B to switch the port to output mode when the OUT instruction is executed. But when the SPB or RPB instruction is executed, the port B data latch contents are output at bits apart from those specified by the instruction operand, thereby switching port B to output port mode. The port B data latch contents are only changed when the OUT, SPB, or RPB instruction is executed.

Port B is automatically set to input port mode when the power is switched on (V_{DD} changed from low to high), when the CKSTP instruction is executed, and when the CE pin is changed from low to high, and remains in input mode until an output instruction (OUT, SPB, or RPB) is executed. And note that the port B data latch contents remain unchanged when the CKSTP instruction is executed or when the CE pin is changed from low to high (and that these contents are undefined when the power is switched on (V_{DD} changed from low to high)).

2.3 PORT C

Port C (PC_3 to PC_1) is a CMOS push-pull type output-only port. Normally, this port is accessed by executing an output instruction (OUT, SPB, or RPB). If an input instruction (IN) is executed, the current output data is read into a specified register. There is no change to the contents output by execution of the IN instruction.

When an output instruction is executed, output of "1" results in output of a high level, and output of "0" results in output of a low level (GND potential). When the power is switched on (V_{DD} changed from low to high) and when the CKSTP instruction is executed, port C is switched to high impedance. The internal data latch contents remain unchanged at this stage (but these contents are undefined when the power is switched on (V_{DD} changed from low to high)).

2.4 PORT M

Port M (PM_2 and PM_1) is an N-channel open-drain type output-only port. This port is normally accessed by executing an output instruction (OUT, SPB, or RPB). If an input instruction (IN) is executed, the current output data is read into a specified register. There is no change to the contents output by execution of the IN instruction.

When an output instruction is executed, output of "1" results in output of a high level (pull-up potential), and output of "0" results in output of a low level (GND potential). When the power is switched on (V_{DD} changed from low to high) or when the CKSTP instruction is executed, port M is switched to "1" output status (high impedance status). That is, pull-up potential output status.

The internal data latch contents remain unchanged at this stage (but these contents are undefined when the power is switched on (V_{DD} changed from low to high)).

3. D/A CONVERTERS

μPD1730 features a 13-bit D/A converter (DA_1) for voltage synthesizer applications and 6-bit D/A converter (DA_2) ideal for volume control, etc.

3.1 DA_1

The conversion method used in the 13-bit tuning D/A converter is a combination of 8-bit pulse width modulation (PWM) and a 5-bit rate multiplier (RMP). Since output pulse signals are obtained from DA_1, D/A conversion is achieved by adding an external low-pass filter.

The DA_1 configuration is outlined in Figure 3-1.

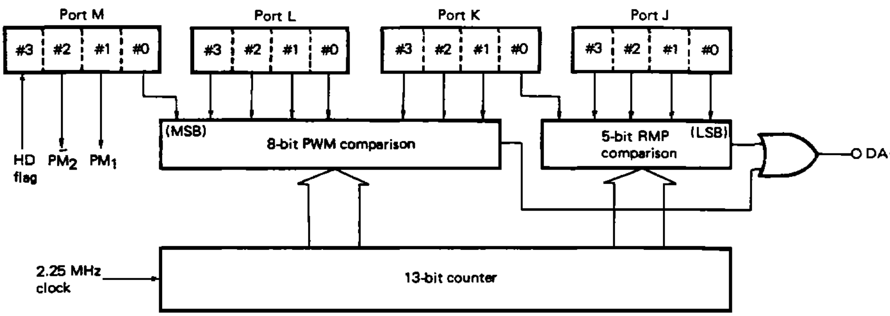


Fig. 3-1 DA_1 Configuration

With a 2.25 MHz fundamental clock frequency, 13-bit D/A conversion is executed by applying 444 nsec throttle pulse signals to the 8-bit PWM signal from 0 to 32 times.

The output waveform is shown in Figure 3-2.

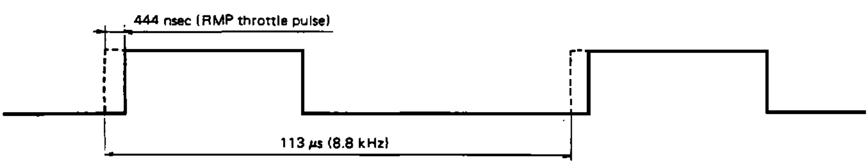


Fig. 3-2 DA_1 Output Waveform

The DA_1 output can be set to internal or external setting mode.

3.1.1 Internal setting mode (INT Mode)

In internal setting mode, the D/A converter (DA_1) output value is set by setting in the internal ports J (PJ_3 to PJ_0), K (PK_3 to PK_0), L (PL_3 to PL_0), and M (PM_0).

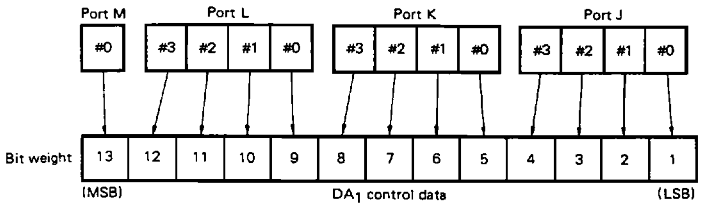


Fig. 3-3 Port Allocation

The bit weight of each port is shown in Figure 3-3. When all bits are set to 0, DA_1 generates a high level output rather than a pulse signal. And if all bits are set to 1, a low level output is generated.

Since D/A converter and CPU operations are asynchronous, unwanted data may appear when setting the port data. To prevent misoperation in µPD1730, the D/A converter conversion data is updated when port M data is set (OUT, SPB, or RPB instruction). The D/A converter output thus remains the same even if changes occur in the port J, port K, or port L value. Therefore, to change the D/A converter output value, data will have to be finally set in port M even if no change in port M data occurs.

3.1.2 External setting mode (VR Mode)

In external setting mode with a variable resistor and capacitor connected to the HD pin, the DA_1 output is varied by changing the variable register value. This mode is set by setting internal port PG_0 to 1. A 56.8 µsec output pulse is obtained from the HD pin to charge up the capacitor every 3.64 msec. And during the discharge interval, the corresponding value is set in the internal ports (ports J, K, L, and M), thereby executing the D/A conversion.

The device cannot be used in HD mode when VR mode has been set.

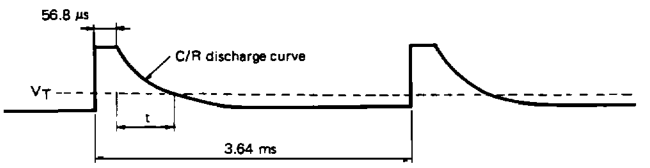


Fig. 3-4 HD Pin Waveform

The HD pin waveform is shown in Figure 3-4. The counter operates only during interval t from the start of discharge up to the threshold voltage (V_T). Therefore, the longer the discharge time t the larger than D/A converter control data. The relationship between discharge time t, capacitor capacitance C, and variable resistor resistance R is expressed by the following equation:

$$\frac{V_{DD}}{V_T} = \exp\frac{-t}{CR}$$

For a D/A output value in the 0.5 to 31 V range in TV applications, C = 0.05 µF and R = 1.5 to 100 kΩ.

3.2 DA_2

Since a 6-bit D/A converter RMP method is used, D/A conversion is executed by connecting a simple low-pass filter. Using a fundamental clock of 90.9 kHz, conversion data is set in internal ports G (PG_2 and PG_3) and H (PH_0 to PH_3).

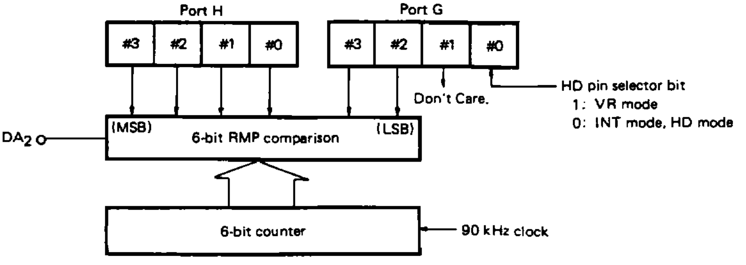


Fig. 3-5 DA_2 Configuration

The relationship between the set data and output pulse is expressed by

$$\text{Duty} = \frac{n}{64} \text{ (where n is a decimal value in the } 0 \leqq n \leqq 63 \text{ range)}$$

The output waveform is shown in Figure 3-6. Low level is set when n = 0.

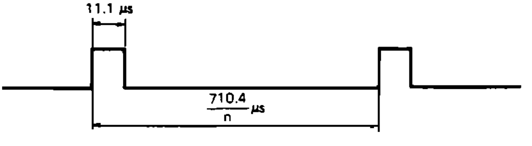


Fig. 3-6 DA_2 Output Waveform

4. A/D CONVERTER

μPD1730 is equipped with a programmed successive comparison type 4-bit A/D converter. Analog inputs are applied to the AD pin. When used in TV applications, an S-curve output from the video intermediate frequency (VIF) stage is normally applied to the input, and this can be used, to judge the optimum tuning frequency during auto fine tuning (AFT). The AD pin can also be used as a 1-bit input port capable of setting the threshold level by program.

4.1 OPERATING PRINCIPLES

The μPD1730 A/D converter consists of a resistance string 4-bit D/A converter and a comparator. Data is set in the D/A converter via internal port D. That is, comparison data is set in port D by executing an output instruction (OUT, SPB, or RPB), and is read by executing an input instruction (IN, TPT, or TPF).

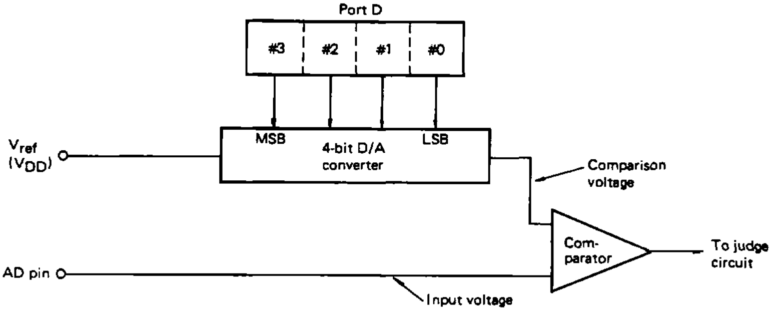


Fig. 4-1 A/D Converter Configuration

The D/A converter can generate 16 different comparison voltages (obtained by dividing the reference voltage V_{ref} (V_{DD})) in accordance to the data set in port D. This comparison voltage is applied to the comparator together with the analog voltage applied to the AD pin (input voltage). The two voltages are compared, and the result is obtained by executing the TADT (Test A/D comparator, then skip if True) or the TADF (Test A/D comparator, then skip if False) instruction. The relationship between the input and comparison voltages is as follows:

True if input voltage > comparison voltage
False if input voltage ≦ comparison voltage

4.2 D/A CONVERTER CONFIGURATION

The D/A converter used in μPD1730 is a so-called resistance string type D/A converter where 16 resistors are connected in series between V_{ref} (V_{DD}) and GND, and the voltage of a subsequent point is selected. It should be noted that the resistance is not the same for all resistors in the series. The value of the two resistors at both ends are 1.5/16 times the other resistors. The D/A converter configuration is outlined in Figure 4-2.

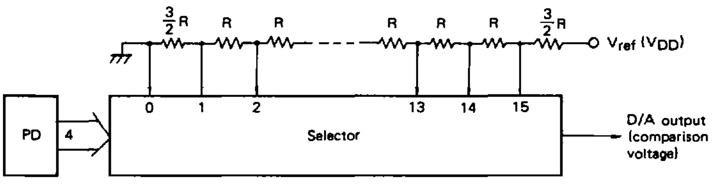


Fig. 4-2 D/A Converter Configuration

In the μPD1730 D/A converter, a GND level output is generated when the value set in port D is 0000B, and a 3/34 x V_{ref} comparison voltage is generated when the port D value is 0001B. The comparison voltage V_{out} when a value of n (decimal number) is set is given by the following equation:

$$V_{out} = V_{ref} \times \frac{2n+1}{34} \quad \text{(where } 15 \geqq n \geqq 1\text{)}$$

Table 4-1 Input Data and Comparison Voltages

Input data (port D)		Comparison voltage	
DEC.	Binary	x Vref	Vref = 5 V
0	0000	0	0 (V)
1	0001	3/34	0.44118
2	0010	5/34	0.73529
3	0011	7/34	1.02941
4	0100	9/34	1.32353
5	0101	11/34	1.61765
6	0110	13/34	1.91176
7	0111	15/34	2.20588
8	1000	17/34	2.50000
9	1001	19/34	2.79412
10	1010	21/34	3.08824
11	1011	23/34	3.38235
12	1100	25/34	3.67647
13	1101	27/34	3.97059
14	1110	29/34	4.26471
15	1111	31/34	4.55882

In the programmed successive comparison A/D converter, the relationship between input voltage V_{in} and the comparison voltage V_n for data n set in the D/A converter is given by the following expression:

$$V_n < V_{in} \leqq V_{n+1}$$

The A/D conversion data output is usually n.

Note that the μPD1730 A/D converter differs from the other A/D converters used in other μPD1700 series devices (such as μPD1709 and μPD1716).

For actual applications, compare and judge input values using the data listed in Table 4-1. The range of A/D converter input voltages V_{in} which can be measured is expressed as:

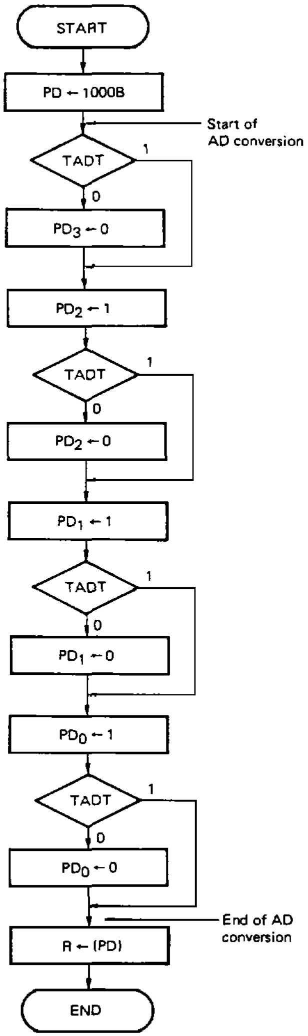
$$0 \leqq V_{in} \leqq V_{15} \; (= V_{ref} \times 31/34)$$

If V_{in} lines in the $V_{15} < V_{in} \leqq V_{ref}$ (V_{DD}) range, it is handled as a "range over" voltage.

As was mentioned above, A/D conversion is achieved by executing the TADT or TADF instruction. For example, consider the input of an analog signal where $V_{in} = V_{14}$ ($V_{ref} \times 13.5/16$). When this is compared with the V_{13} comparison voltage, the result "true" (since input voltage > comparison voltage) is passed to the judge circuit. The input voltage is then compared with the V_{14} comparison voltage, resulting in output of a "false" result since input voltage ≦ comparison voltage.

4.3 EXAMPLE OF AN A/D CONVERSION PROGRAM

Binary search method



Example flow chart

```
START:
        MVI     R, 1000B
        OUT     3, R
        TADT
        RPB     3,1000B
        SPB     3,0100B
        TADT
        RPB     3,0100B
        SPB     3,0010B
        TADT
        RPB     3,0010B
        SPB     3,0001B
        TADT
        RPB     3,0001B
        IN      R, 3
```

Example coding

A/D conversion time: 366.3 μsec
Total number of steps: 16 steps

D

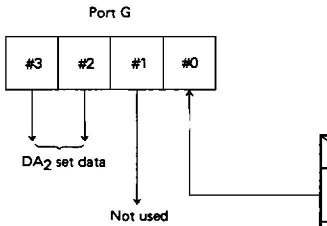
5. HORIZONTAL SYNCHRONIZING SIGNAL DETECTOR CIRCUIT

μPD1730 features a built-in horizontal synchronizing signal detector circuit designed to detect broadcast signals during auto tuning operations.

The input signal applied to the HD pin is measured by a 5-bit counter (gate time: 1.82 msec). The internal port PM_3 is reset (to 0) if an input signal within the 14.831 to 16.480 kHz range is applied, but is set (to 1) if a signal outside this range is applied. That is, the presence on an input broadcast signal can be detected by testing this PM_3 port (using the IN, TPT, or TPF instruction) during auto tuning, etc.

Since this HD pin also serves as an external connection pin when in DA_1 output external setting mode (VR mode), HD mode must be set if the HD circuit is to be used. HD mode can be set by setting the PG_0 internal port to 0. Note that since PG_2 is undefined when the power is switched on, it must always be specified by program.

Table 5-1 PG_2 Mode Table



	DA_1 set mode	HD pin operation mode
0	Internal setting mode (INT mode)	HD mode (horizontal synchronizing signal detector mode)
1	External setting mode	VR mode (output of variable resistance to DA_1)

6. PROGRAMMABLE LOGIC ARRAY (PLA)

μPD1730 is equipped with a user program segment PLA. Normally, key return signal source patterns and dynamic switching display patterns are programmed. A total of 32 patterns (16 types x 2) can be generated.

6.1 SEGMENT PLA CONFIGURATION

The segment PLA consists of a 5-bit segment latch circuit, and a PLA which has seven outputs corresponding to segment pins (pins S_a to S_g) and which accepts the segment latch circuit output.

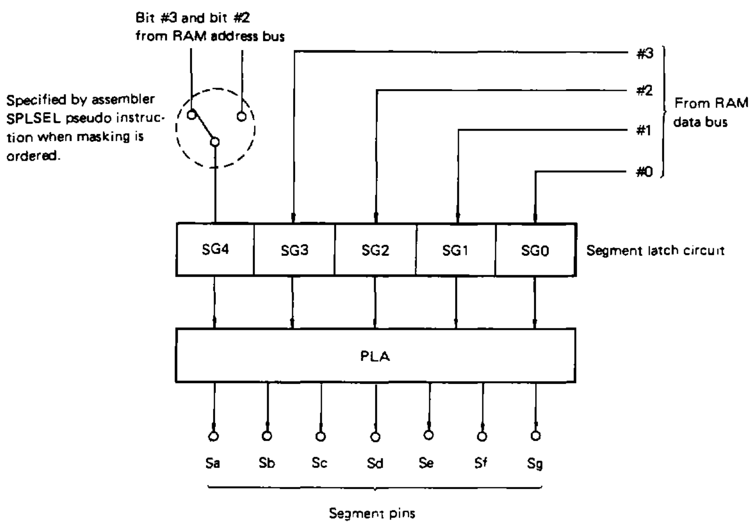


Fig. 6-1 Segment PLA Configuration

The data memory (RAM) contents specified by the SEG instruction operand are latched by the four lower bits (SG0 to SG3) of the segment latch circuit. For example, if the SEG 1,05H instruction is executed within the RAM contents shown below, the RAM contents addressed by 1 (RAM row address designation) and register 05H contents (column address designation), that is, the contents "F" of address 16H, are latched.

Column address

Row address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0						6										
1							F									
2																

The contents of bit #3 or bit #2 of the RAM column address specified by the SEG instruction are latched by the most significant bit (SG4) of the segment latch circuit. When masking is ordered, it is necessary to specify which bit contents are to be latched (see Section 6.3, "PLA PROGRAM EXAMPLE"). If bit #3 is connected, 0 is latched by SG4 when the RAM in column address 00H to 07H is specified by the SEG instruction, and 1 is latched when 08H to 0BH is specified. And if bit #2 is connected, 0 is latched when 00H to 03H and 08H to 0BH are specified, and 1 is latched when 04H to 07H and 0CH to 0FH are specified.

The 32 segment patterns are divided into two groups of 16 patterns each by the data latched in SG4. Therefore, a different segment pattern output can be obtained from the segment pin if a different RAM column address is specified by the SEG instruction, even though the RAM data contents are the same.

The 16 patterns generated when SG4 is 0 are called "pattern group 0", and the patterns generated when SG4 is 1 "pattern group 1".

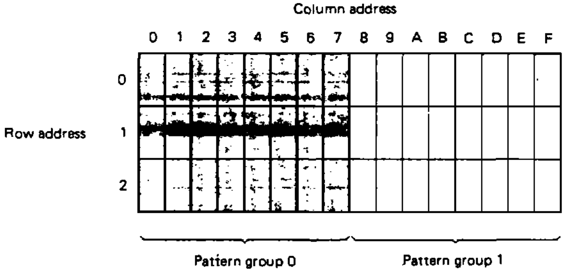


Fig. 6-2 Pattern Group Division When SG4 is Specified to Bit #3

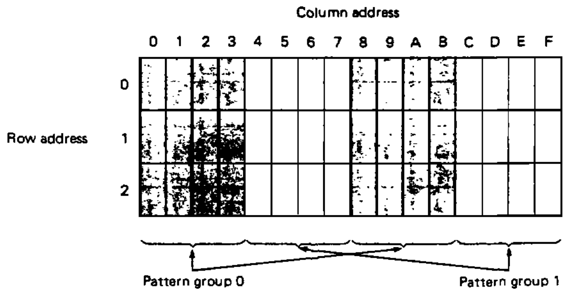


Fig. 6-3 Pattern Group Division When SG4 is Specified to Bit #2

The pattern group division is decided when the program is written, taking into account the efficiency of the RAM and the program (ROM). And SPLSEL is used to decide whether SG4 input bit #3 or bit #2 is to be specified. Use either the

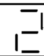
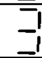
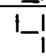
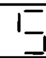
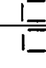
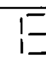
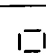
SPLSEL 3 or SPLSEL 2

Description (see Section 6.3, "PLA PROGRAM EXAMPLE").

6.2 SEGMENT PLA PATTERN EXAMPLE

Examples of pattern group 0 and pattern group 1 are shown in Tables 6-1 and 6-2 respectively.

Table 6-1 Pattern Group 0 Pattern Example

Segment latch					Segment output (Note)							Output pattern
SG4	SG3	SG2	SG1	SG0	S_g	S_f	S_e	S_d	S_c	S_b	S_a	
0	0	0	0	0	1	0	0	0	0	0	0	
	0	0	0	1	1	1	1	1	0	0	1	
	0	0	1	0	0	1	0	0	1	0	0	
	0	0	1	1	0	1	1	0	0	0	0	
	0	1	0	0	0	0	1	1	0	0	1	
	0	1	0	1	0	0	1	0	0	1	0	
	0	1	1	0	0	0	0	0	0	1	0	
	0	1	1	1	1	0	1	1	0	0	0	
	1	0	0	0	0	0	0	0	0	0	0	
	1	0	0	1	0	0	1	0	0	0	0	
	1	0	1	0	1	1	1	1	1	1	1	Blank (Display off)
	1	0	1	1	0	0	0	0	1	1	0	
	1	1	0	0	0	1	1	1	1	1	1	
	1	1	0	1	1	1	1	0	1	1	1	
	1	1	1	0	0	0	1	1	1	0	0	
	1	1	1	1	0	1	0	0	0	1	1	

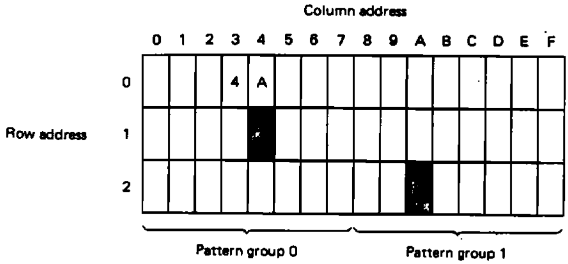
Note:

Segment outputs are set by active low. When active high, 0 is replaced by 1, and 1 is replaced by 0. And since the μPD1730 segment output is an N-channel open-drain format, it is normally set to active low.

Table 6-2 Pattern Group 1 Pattern Example

Segment latch					Segment output							Output pattern
SG4	SG3	SG2	SG1	SG0	S_g	S_f	S_e	S_d	S_c	S_b	S_a	
1	0	0	0	0	0	0	0	0	0	0	0	Key all ON
	0	0	0	1	1	1	1	1	1	1	0	Seg a (Key)
	0	0	1	0	1	1	1	1	1	0	1	Seg b (Key)
	0	0	1	1	1	1	1	1	0	1	1	Seg c (Key)
	0	1	0	0	1	1	1	0	1	1	1	Seg d (Key)
	0	1	0	1	1	1	0	1	1	1	1	Seg e (Key)
	0	1	1	0	1	0	1	1	1	1	1	Seg f (Key)
	0	1	1	1	0	1	1	1	1	1	1	Seg g (Key)
	1	0	0	0	1	1	1	1	1	1	1	Key all OFF
	1	0	0	1	1	1	1	1	1	1	1	Not used.
	1	0	1	0	1	1	1	1	1	1	1	Not used.
	1	0	1	1	1	1	1	1	1	1	1	Not used.
	1	1	0	0	1	1	1	1	1	1	1	Not used.
	1	1	0	1	1	1	1	1	1	1	1	Not used.
	1	1	1	0	1	1	1	1	1	1	1	Not used.
	1	1	1	1	1	1	1	1	1	1	1	Not used.

When the above display pattern is used, the following output contents are obtained during execution of the SEG instruction. In this case, however, column address bit #3 is specified as the segment latch circuit SG4 input.



(1) SEG 1, 03H. . . RAM address 14H contents (0011B) are latched.

Output pattern "  "

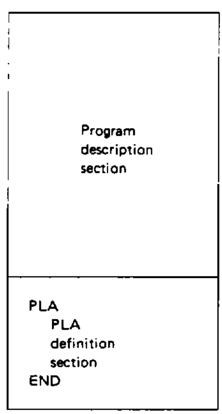
(2) SEG 2, 04H. . . RAM address 2AH contents (0011B) are latched.

Output pattern "Seg C"

As can be seen from this example, different output patterns can be obtained if the SG4 contents are different, even though the data set in the four lower bits of the segment latch circuit are the same.

6.3 PLA PROGRAM EXAMPLE

The PLA needs to be defined in μPD1730. **When ordering masks, those where the PLA section has not been defined cannot be accepted.** The PLA definition is described at the end of the assembler source program. The following items are included. Note that all items must be described – not a single one can be omitted.



(1) PLA pseudo instruction

In addition to the end of the program description section, this description also indicates the beginning of the PLA definition section.

(2) SPLSEL (Segment PLA Select) pseudo instruction

Description used to select the RAM address division for generation of segment pattern groups 0 and 1. Two description examples are given below.

SPLSEL 3 or SPLSEL 2

(3) DSP (Define Segment PLA) pseudo instruction

Definition of the 32 types of segment PLA patterns. The 16 patterns in pattern group 0 must be defined sequentially. A description example is given below. The first bit to be described is segment g (Sg pin).

```
DSP  1  1  1  1  0  0  1  B
     ↑                 ↑
     Sg                Sa
```

The remaining bits are then described in descending order.

(4) END

In addition to the end of the PLA definition section, this description also indicates the end of the source program. The program is not assembled without this description.

Note 1: In μPD1700 series devices which include the DIGIT PLA function (μPD1701, μPD1703, μPD1704, μPD1705, μPD1707, and μPD1710), the DIGIT PLA definition is also required. DIGIT PLA is defined by using the DDP (Define Digit PLA) pseudo instruction.

Note 2: Although the PLA definition must commence with PLA and end with END, the intermediate SPLSEL, DSP, DDP, and MTDIG can be described in any order.

PLA Program Example

```
; * * * *  PLA DEFINITION * * * *
PLA
;
SPLSEL 3                     ;  RAM ADDR BIT #3
;
;* * *  SEGMENT PATTERN    0 * * *
;
;          g f e d c b a
DSP        1 0 0 0 0 0 0 B      ;  0
DSP        1 1 1 1 0 0 1 B      ;  1
DSP        0 1 0 0 1 0 0 B      ;  2
DSP        0 1 1 0 0 0 0 B      ;  3
DSP        0 0 1 1 0 0 1 B      ;  4
DSP        0 0 1 0 0 1 0 B      ;  5
DSP        0 0 0 0 0 1 0 B      ;  6
DSP        1 0 1 1 0 0 0 B      ;  7
DSP        0 0 0 0 0 0 0 B      ;  8
DSP        0 0 1 0 0 0 0 B      ;  9
DSP        1 1 1 1 1 1 1 B      ;  BLANK
DSP        0 0 0 0 1 1 0 B      ;  E
DSP        0 1 1 1 1 1 1 B      ;  SEG G ON
DSP        1 1 1 0 1 1 1 B      ;  SEG D ON
DSP        0 0 1 1 1 0 0 B      ;  SEG A, B, F, G ON
DSP        0 1 0 0 0 1 1 B      ;  SEG C, D, E, G ON
;
;* * *  SEGMENT PATTERN    1 * * *
;
DSP        0 0 0 0 0 0 0 B      ;  SEG ALL ON, KEY RETURN
DSP        1 1 1 1 1 1 0 B      ;  SEG A ON
DSP        1 1 1 1 1 0 1 B      ;  SEG B ON
DSP        1 1 1 1 0 1 1 B      ;  SEG C ON
DSP        1 1 1 0 1 1 1 B      ;  SEG D ON
DSP        1 1 0 1 1 1 1 B      ;  SEG E ON
DSP        1 0 1 1 1 1 1 B      ;  SEG F ON
DSP        0 1 1 1 1 1 1 B      ;  SEG G ON
DSP        1 1 1 1 1 1 1 B      ;  SEG ALL OFF
DSP        1 1 1 1 1 1 1 B      ;  NO USE
DSP        1 1 1 1 1 1 1 B      ;  NO USE
DSP        1 1 1 1 1 1 1 B      ;  NO USE
DSP        1 1 1 1 1 1 1 B      ;  NO USE
DSP        1 1 1 1 1 1 1 B      ;  NO USE
DSP        1 1 1 1 1 1 1 B      ;  NO USE
DSP        1 1 1 1 1 1 1 B      ;  NO USE
;
;
;
END
```

D

7. μPD1730 INSTRUCTION

7.1 INSTRUCTION SET

b_{13} b_{12} b_{11} b_{10} \ b_{15} b_{14}		0 0	0 1	1 0	1 1
		0	1	2	3
0 0 0 0	0	NOP	——	——	ST M, r
0 0 0 1	1	SPB P, N BANK1 BANK2 STC	ORI M, I	SEG D_H, r	MVRS M, r
0 0 1 0	2	——	MVI M, I	OUT P, r	IN r, P
0 0 1 1	3	RPB P, N BANK0 RSC	ANI M, I	CKSTP	MVRD r, M
0 1 0 0	4	RT	AI M, I	MVSR M_1, M_2	AD r, M
0 1 0 1	5	RTS	SI M, I	EXL r, M	SU r, M
0 1 1 0	6	JMP ADDR	AIC M, I	LD r, M	AC r, M
0 1 1 1	7	CAL ADDR	SIB M, I	——	SB r, M
1 0 0 0	8	TPF P, N TCEF	AIN M, I	TRS TADT TADF	ADN r, M
1 0 0 1	9	TPT P, N TCET	SIN M, I	TTM	SUN r, M
1 0 1 0	A	TMF M, N	AICN M, I	——	ACN r, M
1 0 1 1	B	TMT M, N	SIBN M, I	——	SBN r, M
1 1 0 0	C	SLTI M, I	AIS M, I	SLT r, M	ADS r, M
1 1 0 1	D	SGEI M, I	SIS M, I	SGE r, M	SUS r, M
1 1 1 0	E	SEQI M, I	AICS M, I	SEQ r, M	ACS r, M
1 1 1 1	F	SNEI M, I	SIBS M, I	SNE r, M	SBS r, M

7.2 INSTRUCTIONS

NOTE :
- D_H : Data memory address high (row address) [2 bits]
- D_L : Data memory address low (column address) [4 bits]
- Rn : Register number [4 bits]
- I : Immediate data [4 bits]
- N : Bit position [4 bits]
- ADDR : Program memory address [10 bits]
- — : All "1"
- r : General register
  One of addresses 00–0FH of BANK0
- M : Data memory address
- P : Port, $0 \leq P \leq 3$
- N_1 : Bit position of status word 1 $0 \leq N_1 \leq 7$
- N_2 : Bit position of status word 2 $0 \leq N_2 \leq 7$
- ( ) : Content of register or memory
- c : Carry
- b : Borrow
- [ ] : Decoded value of content of register of memories

	Mnemonic	Operand		Function	Operation	Machine code			
		1ST	2ND			Operation code			
Addition	AD	r	M	Add memory to register	r←(r)+(M)	1 1 0 1 0 0	D_H	D_L	Rn
	ADS	r	M	Add memory to register, then skip if carry	r←(r)+(M) skip if carry	1 1 1 1 0 0	D_H	D_L	Rn
	ADN	r	M	Add memory to register, then skip if not carry	r←(r)+(M) skip if not carry	1 1 1 0 0 0	D_H	D_L	Rn
	AC	r	M	Add memory to register with carry	r←(r)+(M)+c	1 1 0 1 1 0	D_H	D_L	Rn
	ACS	r	M	Add memory to register with carry, then skip if carry	r←(r)+(M)+c skip if carry	1 1 1 1 1 0	D_H	D_L	Rn
	ACN	r	M	Add memory to register with carry, then skip if not carry	r←(r)+(M)+c skip if not carry	1 1 1 0 1 0	D_H	D_L	Rn
	AI	M	I	Add immediate data to memory	M←(M)+I	0 1 0 1 0 0	D_H	D_L	I
	AIS	M	I	Add immediate data to memory, then skip if carry	M←(M)+I skip if carry	0 1 1 1 0 0	D_H	D_L	I
	AIN	M	I	Add immediate data to memory, then skip if not carry	M←(M)+I skip if not carry	0 1 1 0 0 0	D_H	D_L	I
	AIC	M	I	Add immediate data to memory with carry	M←(M)+I+c	0 1 0 1 1 0	D_H	D_L	I
	AICS	M	I	Add immediate data with carry, then skip if carry	M←(M)+I+c skip if carry	0 1 1 1 1 0	D_H	D_L	I
	AICN	M	I	Add immediate data with carry, then skip if not carry	M←(M)+I+c skip if not carry	0 1 1 0 1 0	D_H	D_L	I
Subtraction	SU	r	M	Subtract memory from register	r←(r)−(M)	1 1 0 1 0 1	D_H	D_L	Rn
	SUS	r	M	Subtract memory from register, then skip if borrow	r←(r)−(M) skip if borrow	1 1 1 1 0 1	D_H	D_L	Rn
	SUN	r	M	Subtract memory from register, then skip if not borrow	r←(r)−(M) skip if not borrow	1 1 1 0 0 1	D_H	D_L	Rn
	SB	r	M	Subtract memory from register with borrow	r←(r)−(M)−b	1 1 0 1 1 1	D_H	D_L	Rn
	SBS	r	M	Subtract memory from register with borrow, then skip if borrow	r←(r)−(M)−b skip if borrow	1 1 1 1 1 1	D_H	D_L	Rn
	SBN	r	M	Subtract memory from register with borrow, then skip if not borrow	r←(r)−(M)−b skip if not borrow	1 1 1 0 1 1	D_H	D_L	Rn
	SI	M	I	Subtract immediate data from memory	M←(M)−I	0 1 0 1 0 1	D_H	D_L	I
	SIS	M	I	Subtract immediate data from memory, then skip if borrow	M←(M)−I skip if borrow	0 1 1 1 0 1	D_H	D_L	I
	SIN	M	I	Subtract immediate data from memory, then skip if not borrow	M←(M)−I skip if not borrow	0 1 1 0 0 1	D_H	D_L	I
	SIB	M	I	Subtract immediate data from memory, with borrow	M←(M)−I−b	0 1 0 1 1 1	D_H	D_L	I
	SIBS	M	I	Subtract immediate data with borrow, then skip if borrow	M←(M)−I−b skip if borrow	0 1 1 1 1 1	D_H	D_L	I
	SIBN	M	I	Subtract immediate data with borrow, then skip if not borrow	M←(M)−I−b skip not borrow	0 1 1 0 1 1	D_H	D_L	I

	Mnemonic	Operand		Function	Operation	Machine code			
		1ST	2ND			Operation code			
Comparison	SEQ	r	M	Skip if register equal memory	r − M skip if zero	1 0 1 1 1 0	D_H	D_L	R_n
	SNE	r	M	Skip if register not equals memory	r − M skip if not zero	1 0 1 1 1 1	D_H	D_L	R_n
	SGE	r	M	Skip if register is greater than or equal to memory	r − M skip if not borrow (r) ≧ (M)	1 0 1 1 0 1	D_H	D_L	R_n
	SLT	r	M	Skip if register is less than memory	r − M skip if borrow (r) < (M)	1 0 1 1 0 0	D_H	D_L	R_n
	SEQI	M	I	Skip if memory equals immediate data	M − I skip if zero	0 0 1 1 1 0	D_H	D_L	I
	SNEI	M	I	Skip if memory not equal immediate data	M − I skip if not zero	0 0 1 1 1 1	D_H	D_L	I
	SGEI	M	I	Skip if memory is greater than or equal to immediate data	M − I skip if not borrow (M) ≧ I	0 0 1 1 0 1	D_H	D_L	I
	SLTI	M	I	Skip if memory is less than immediate data	M − I skip if borrow (M) < I	0 0 1 1 0 0	D_H	D_L	I
Logical operation	ANI	M	I	Logic AND of memory and immediate data	M ← (M) ∧ I	0 1 0 0 1 1	D_H	D_L	$\bar{I}$
	ORI	M	I	Logic OR of memory and immediate data	M ← (M) ∨ I	0 1 0 0 0 1	D_H	D_L	I
	EXL	r	M	Exclusive OR Logic of memory and register	r ← (r) ⊕ (M)	1 0 0 1 0 1	D_H	D_L	R_n
Transfer	LD	r	M	Load memory to register	r ← (M)	1 0 0 1 1 0	D_H	D_L	R_n
	ST	M	r	Store register to memory	M ← (r)	1 1 0 0 0 0	D_H	D_L	R_n
	MVRD	r	M	Move memory to destination memory referring to register in the same row	[D_H, Rn] ← (M)	1 1 0 0 1 1	D_H	D_L	R_n
	MVRS	M	r	Move source memory referring to register to memory in the same row	M ← [D_H, Rn]	1 1 0 0 0 1	D_H	D_L	R_n
	MVSR	M_1	M_2	Move memory to memory in the same row	[D_H, DL_1] ← [D_H, DL_2]	1 0 0 1 0 0	D_H	D_{L1}	D_{L2}
	MVI	M	I	Move immediate data to memory	M ← I	0 1 0 0 1 0	D_H	D_L	I
Bit test	TMT	M	N	Test memory bits, then skip if all bits specified are true	if M(N) = all "1", then skip	0 0 1 0 1 1	D_H	D_L	N
	TMF	M	N	Test memory bits, then skip all bits specified are false	if M(N) = all "0", then skip	0 0 1 0 1 0	D_H	D_L	N
Jump	JMP	ADDR		Jump to the address specified	PC ← ADDR	0 0 0 1 1 0	ADDR (10 bits).		
Subroutine	CAL	ADDR		Call subroutine	Stack ← (PC) + 1, PC ← ADDR	0 0 0 1 1 1	ADDR (10 bits)		
	RT			Return to main routine	PC ← (stack)	0 0 0 1 0 0	—	—	—
	RTS			Return to main routine, then skip unconditionary	PC ← (stack), and skip	0 0 0 1 0 1	—	—	—
F/F test	TTM			Test and reset timer F/F, then skip if it has not been set	if Timer F/F = 1, then Timer F/F ← 0 if Timer F/F = 0, then skip	1 0 1 0 0 1	—	—	—

	Mnemonic	Operand		Function	Operation	Machine code			
		1ST	2ND			Operation code			
Status word and terminal test	STC			Set carry F/F	carry F/F ← 1	0 0 0 0 0 1	—	0 0 1 0	—
	RSC			Reset carry F/F	carry F/F ← 1	0 0 0 0 1 1	—	0 0 1 0	—
	BANK0			Select BANK0	BANK F/F0 ← 0, BANK F/F1 ← 0	0 0 0 0 1 1	—	1 1 0 0	—
	BANK1			Select BANK1	BANK F/F0 ← 1, BANK F/F1 ← 0	0 0 0 0 0 1	—	0 1 0 0	—
	BANK2			Select BANK2	BANK F/F0 ← 0, BANK F/F1 ← 1	0 0 0 0 0 1	—	1 0 0 0	—
	TCET			Test CE, skip if true	if CE = 1, then skip	0 0 1 0 0 1	—	0 0 1 0	—
	TCEF			Test CE, skip if false	if CE = 0, then skip	0 0 1 0 0 0	—	0 0 1 0	—
	TRS			Test remote signal, then skip if it is not high level	Skip if RS = 0	1 0 1 0 0 0	—	—	—
Input / output	SEG	D_H	r	Output segment pattern based on the memory specified indirectly	$SG_{0\sim4} \leftarrow [D_H, (Rn)]$, $S_{0\sim8} \leftarrow \{SG_{0\sim4}\}$	1 0 0 0 0 1	D_H	—	Rn
	IN	r	P	Input data on port to register	r ← (Port (P))	1 1 0 0 1 0	P	—	Rn
	OUT	P	r	Output contents of register to port	(Port (P)) ← (r)	1 0 0 0 1 0	P	—	Rn
	SPB	P	N	Set port bits	$(Port(P))_N \leftarrow 1$	0 0 0 0 0 1	P	0 0 0 0	N
	RPB	P	N	Reset port bits	$(Port(P))_N \leftarrow 0$	0 0 0 0 1 1	P	0 0 0 0	N
	TPT	P	N	Test port bits, then skip if all bits specified are true	if $(Port(P))_N$ = all 1s, then skip	0 0 1 0 0 1	P	0 0 0 0	N
	TPF	P	N	Test port bits, then skip if all bits specified are false	if $(Port(P))_N$ = all 0s, then skip	0 0 1 0 0 0	P	0 0 0 0	N
Test A/D	TADT			Test A-D comparator, then skip it true	if $V_{in} > V_{comp}$, then skip	1 0 1 0 0 0	0 0	0 0 0 0	—
	TADF			Test A-D comparator, then skip it false	if $V_{in} \leq V_{comp}$, then skip	1 0 1 0 0 0	1 0	0 0 0 0	—
Others	CKSTP			Clock stop by CE	stop clock if CE = 0	1 0 0 0 1 1	—	1 1 1 0	1 1 1 0
	NOP			No operation		0 0 0 0 0 0	—	—	—

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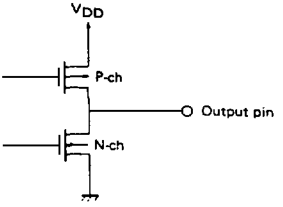
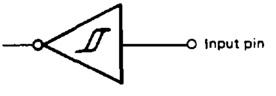
8. INPUT AND OUTPUT CIRCUITS

The μPD1730 input and output circuits for each pin are shown below in partially simplified form.

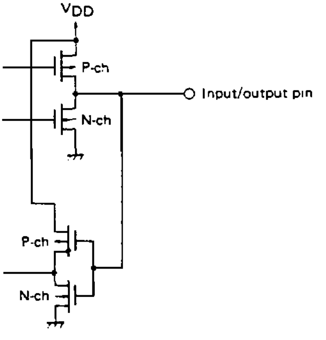
(1) DA_1, DA_2, PC_1 to PC_3



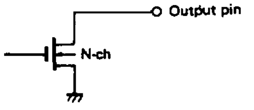
(2) CE



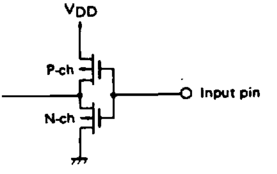
(3) PA_0 to PA_3, PB_0 to PB_3



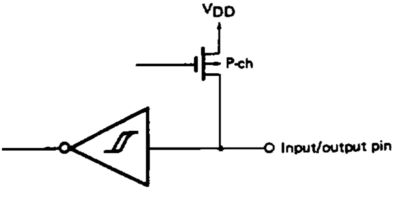
(4) Sa to Sg, PM_1, PM_2



(5) RS



(6) HD



9. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{DD}	–0.3 to 6.0	V
Input Voltage	V_I	–0.3 to V_{DD} +0.3	V
Output Voltage	V_O	–0.3 to V_{DD} +0.3	V
Output Absorption Current	I_{O1}	10 (per non-segment pin)	mA
Output Absorption Current	I_{O2}	50 (total for non-segment pins)	mA
Output Absorption Current	I_{O3}	50 (per segment)	mA
Power Consumption	P_D	500 (T_a = 75 °C)	mW
Operating Temperature	T_a	–25 to +75	°C
Storage Temperature	T_{stg}	–55 to +125	°C
Output Break Down Strength	V_{BDS}	15 (S_a to S_g, PM_1, PM_2)	V

RECOMMENDED OPERATING RANGE

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	CE = High
Data Retention Voltage	V_{DR}	2.5		5.5	V	CE = Low, CKSTP instruction executed
Operating Temperature	T_a	–25		+75	°C	
Output Break Down Strength	V_{BDS}			14	V	S_a to S_g, PM_1, PM_2
Oscillator Frequency	f_c		4.5		MHz	
Supply Voltage Rise Time	T_{rise}			500	ms	0 → 4.5 V

DC CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_a = –25 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
Supply Current	I_{DD}			5	mA	Unloaded, f_c = 4.5 MHz
Data Retention Voltage	V_{DR}	2.5		5.5	V	CKSTP instruction executed (CE = Low)
Data Retention Current	I_{DR}			250	μA	CKSTP instruction executed (CE = Low) T_a = 25 °C, V_{DD} = 5 V
High Level Input Voltage	V_{IH1}	0.7 V_{DD}			V	Port A, RS, HD, CE
High Level Input Voltage	V_{IH2}	0.6 V_{DD}			V	Port B
Low Level Input Voltage	V_{IL1}			0.3 V_{DD}	V	Port A, RS, HD, CE
Low Level Input Voltage	V_{IL2}			0.2 V_{DD}	V	Port B
High Level Output Current	I_{OH1}	0.5			mA	Port A (V_{OH} = V_{DD} – 0.5 V)
High Level Output Current	I_{OH2}	0.4			mA	Port B (V_{OH} = V_{DD} – 0.5 V)
High Level Output Current	I_{OH3}	10			mA	Port C (V_{OH} = V_{DD} – 0.5 V)
High Level Output Current	I_{OH4}	1			mA	DA_1, DA_2 (V_{OH} = V_{DD} – 0.5 V)
Low Level Output Current	I_{OL1}	0.5			mA	Port A (V_{OL} = 0.5 V)
Low Level Output Current	I_{OL2}	0.4			mA	Port B (V_{OL} = 0.5 V)
Low Level Output Current	I_{OL3}	2			mA	PC_1, PC_2 (V_{OL} = 0.5 V)
Low Level Output Current	I_{OL4}	0.5			mA	PC_3 (V_{OL} = 0.5 V)
Low Level Output Current	I_{OL5}	1			mA	DA_1, DA_2 (V_{OL} = 0.5 V)
Low Level Output Current	I_{OL6}	5			mA	PM_1, PM_2 (V_{OL} = 1 V)
Low Level Output Current	I_{OL7}	30			mA	S_a to S_g (V_{OL} = 3 V)
Output Leakage Current	I_L			5	μA	PM_1, PM_2, S_a to S_g (V_O = 14 V)

AC CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_a = –25 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Horizontal synchronizing signal detection frequency	f_{HD}	14.85		16.48	kHz	f_c = 4.5 MHz

A/D CONVERTER CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_a = –25 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Resolution		4	4	4	bit	
Absolute accuracy				±2.5	LSB	T_a = –10 to +50 °C, V_{DD} = 5 V
		Monotone at all steps				
Analog input resistance	R_{IA}	1			MΩ	
Analog input voltage	V_{IA}	0		V_{DD}	V	

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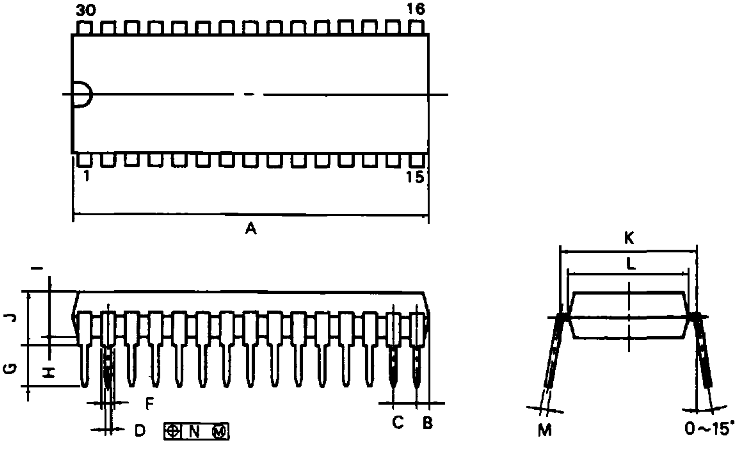
10. PACKAGE DIMENSION

30-pin plastic shrink DIP (400 mil) dimension



S30C-70-400B

NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007