DATA SHEET

MOS INTEGRATED CIRCUIT

# μPD17P218

## 4-BIT SINGLE-CHIP MICROCONTROLLER FOR INFRARED REMOTE CONTROLLER

### DESCRIPTION

The μPD17P218 is a model of the μPD17218 with a one-time PROM instead of an internal mask ROM. ★

Since the user can write programs to the μPD17P218, it is ideal for experimental production or small-scale production of the μPD17215, 17216, 17217 or 17218 systems.

When reading this document, also read the documents related to the μPD17215, 17216, 17217 and 17218.

**Detailed functions are described in the following user's manual. Read this manual when designing your system.**

**μPD172×× Series User's Manual: IEU-1317**

### FEATURES

- Pin compatible with μPD17215, 17216, 17217 and 17218 (except PROM programming function)
- Carrier generator circuit for infrared remote controller (REM output)
- 17K architecture: General-purpose register method
- Program memory (one-time PROM): 16K bytes (8192 × 16)
- Data memory (RAM): 223 × 4 bits
- Pull-up resistor can be connected to $\overline{\text{RESET}}$ pin**Note**.
- Low-voltage detection circuit ($\overline{\text{WDOUT}}$ output)**Note**
- Operating voltage range: 2.0 to 5.5 V ($f_x$ = 4 MHz: normal mode, 8 μs)
  2.2 to 5.5 V ($f_x$ = 4 MHz: high-speed mode, 4 μs)
  3.5 to 5.5 V ($f_x$ = 8 MHz: high-speed mode, 2 μs)

**Note**: Can be selected by mask option with the mask model.

### APPLICATIONS

Preset remote controllers, toys, and portable systems

### ORDERING INFORMATION

| Part Number | Package | Quality Grade |
|---|---|---|
| μPD17P218GT | 28-pin plastic SOP (375 mil) | Standard |
| μPD17P218CT | 28-pin plastic shrink DIP (400 mil) | Standard |

Please refer to "Quality Grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

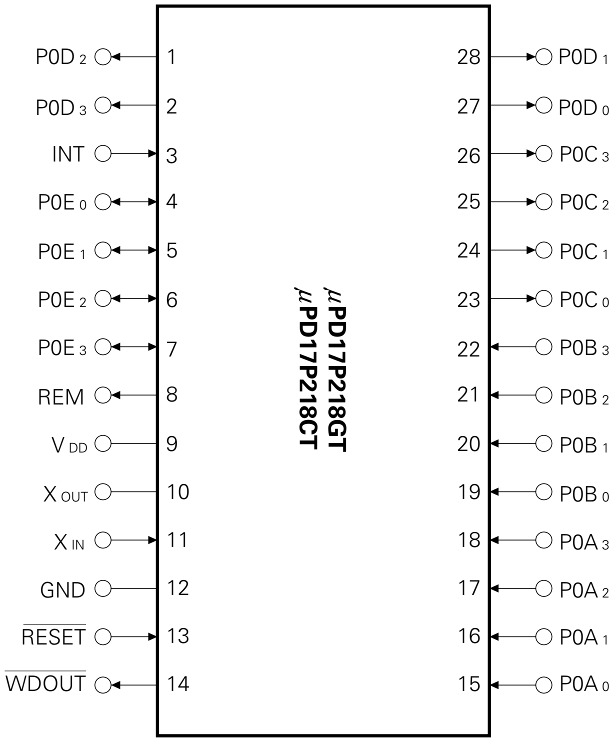
**The information in this document is subject to change without notice.**

**The mark ★ shows major revised points.**

Document No. IC - 3252
(O. D. No. IC - 8797)
Date Published September 1994 P
Printed in Japan

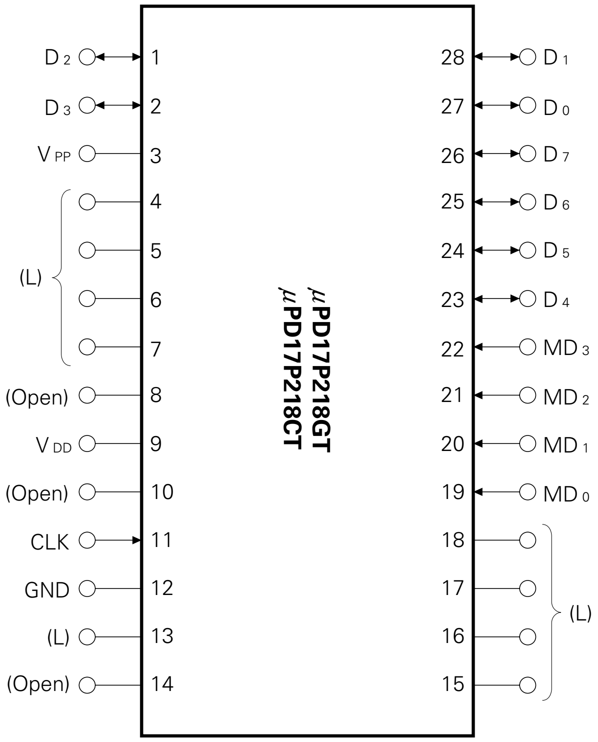
## PIN CONFIGURATION (TOP VIEW)

(1) Normal operation mode



GND : Ground
INT : External interrupt request signal input
$P0A_0$-$P0A_3$ : Port 0A (CMOS input)
$P0B_0$-$P0B_3$ : Port 0B (CMOS input)
$P0C_0$-$P0C_3$ : Port 0C (N-ch open-drain output)
$P0D_0$-$P0D_3$ : Port 0D (N-ch open-drain output)
$P0E_0$-$P0E_3$ : Port 0E (CMOS push-pull output)
REM : Remote controller transmission output (CMOS push-pull output)
$\overline{\text{RESET}}$ : Reset input
$V_{DD}$ : Positive power supply
$\overline{\text{WDOUT}}$ : Hang-up detection/low-voltage detection output (N-ch open-drain output)
$X_{IN}$, $X_{OUT}$ : Oscillation connection

(2) PROM programming mode



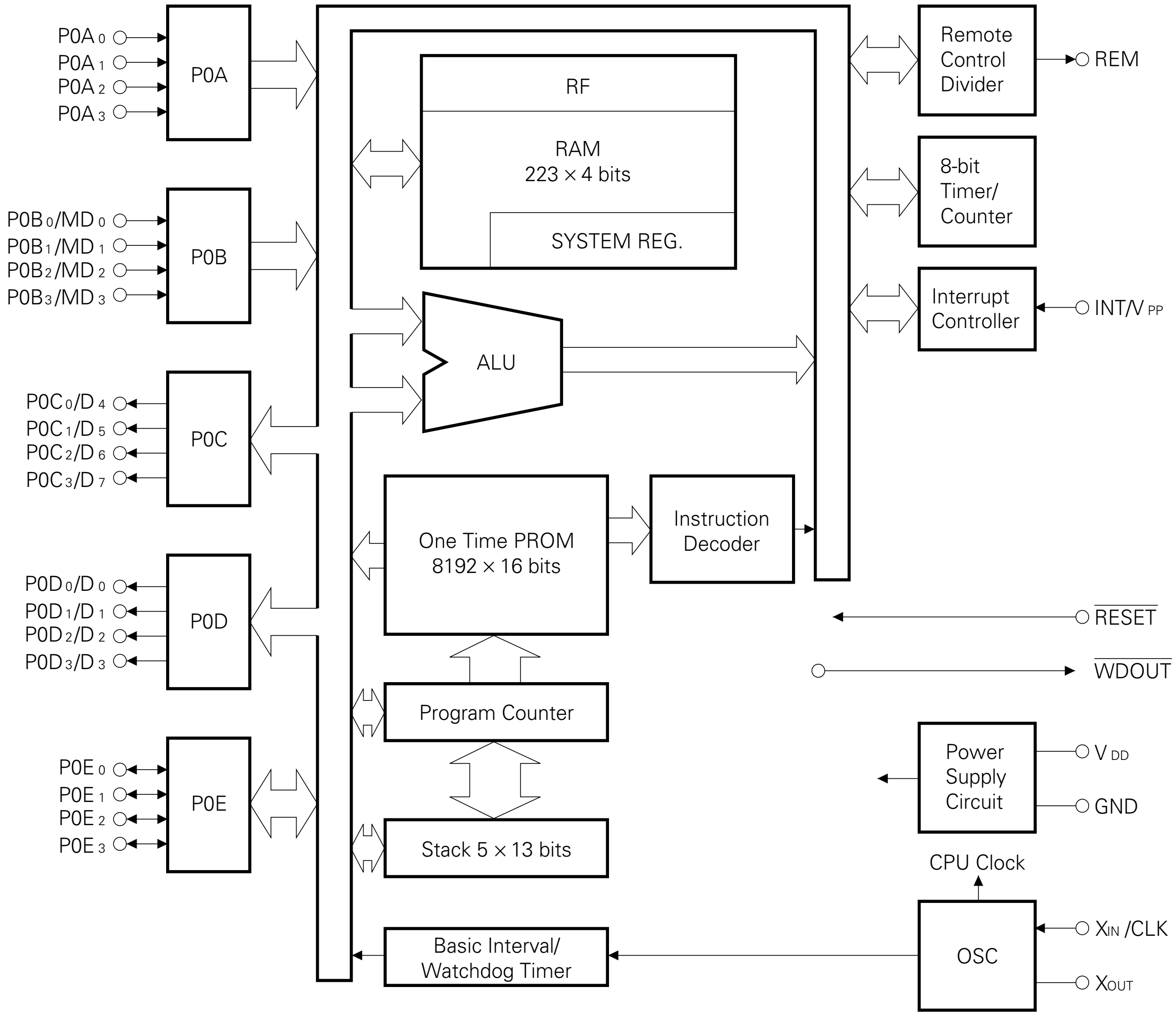
**Note: Those enclosed in parentheses indicate the processing of the pins not used in PROM programming mode.**

**L : Ground these pins through a resistor (470 W).**

**Open : Do not connect anything to these pins.**

CLK : PROM clock input
$D_0$-$D_7$ : PROM data I/O
GND : Ground
$MD_0$-$MD_3$ : PROM mode selection
$V_{DD}$ : Positive power supply
$V_{PP}$ : PROM writing power supply

## BLOCK DIAGRAM



## CONTENTS

## ★ 1. DIFFERENCES BETWEEN μPD17P218 AND μPD17215/17216/17217/17218

The μPD17P218 is a model of the μPD17218 provided with a one-time PROM as the program memory, to which the user can write data, instead of an internal mask ROM.

Table 1-1 shows the differences among the μPD17P218, μPD17215, 17216, 17217, and 17218.

These five products have different memory capacities and mask options but the same CPU function and internal hardware. Therefore, the μPD17P218 can be used to evaluate the program of a system using the μPD17215, 17216, 17217, or 17218. **Note that part of the electrical specifications of the μPD17P218 such as supply current and low-voltage detection voltage are different from those of the μPD17215, 17216, 17217, and 17218.**

For the detail of the CPU functions and internal hardware, refer to the Data Sheet of the μPD17215, 17216, 17217, and 17218.

**Table 1-1 Differences between μPD17P218 and 17215/17216/17217/17218**

| Product Name<br>Item | μPD17P218 | μPD17215 | μPD17216 | μPD17217 | μPD17218 |
|---|---|---|---|---|---|
| Program Memory | One-time PROM | Mask ROM | | | |
| | 16 K bytes (8192 × 16)<br>(0000H-1FFFH) | 4 K bytes (2048 × 16)<br>(0000H-07FFH) | 8 K bytes (4096 × 16)<br>(0000H-0FFFH) | 12 K bytes (6144 × 16)<br>(0000H-17FFH) | 16 K bytes (8192 × 16)<br>(0000H-1FFFH) |
| Data Memory | 223 × 4 bits | 111 x 4 bits | | 223 x 4 bits | |
| Pull-Up Resistor of $\overline{\text{RESET}}$ Pin | Provided | Any (mask option) | | | |
| Low-Voltage Detector Circuit [Note] | Provided | Any (mask option) | | | |
| $V_{PP}$ Pin, Operation Mode Select Pin | Provided | Not provided | | | |
| Instruction Execution Time | 2 μs (8 MHz ceramic oscillator: in high-speed mode)<br>4 μs (4 MHz ceramic oscillator: in high-speed mode)<br>16 μs (1 MHz ceramic oscillator: in high-speed mode) | | | | |
| Operation When P0C, P0D Are Standby | Retain output level immediately before standby mode | | | | |
| Operating Voltage Range | 2.2 to 5.5 V (at 4 MHz, in high-speed mode) | | | | |
| Package | 28-pin plastic SOP (375 mil)<br>28-pin plastic shrink DIP (400 mil) | | | | |

**Note**: Although the circuit configuration of the low-voltage detector circuit is identical, its electrical specifications differ depending on the product.

## 2. PIN FUNCTIONS

### 2.1 IN NORMAL MODE

| Pin No. | Symbol | Function | Output Format | On Reset |
|---|---|---|---|---|
| 15<br>16<br>17<br>18 | $\mathrm{P0A_0}$<br>$\mathrm{P0A_1}$<br>$\mathrm{P0A_2}$<br>$\mathrm{P0A_3}$ | 4-bit CMOS input port with pull-up resistor.<br>Can be used for key return input of key matrix. This port can release standby mode when at least one of pins goes low. | — | Input |
| 19<br>20<br>21<br>22 | $\mathrm{P0B_0}$<br>$\mathrm{P0B_1}$<br>$\mathrm{P0B_2}$<br>$\mathrm{P0B_3}$ | 4-bit CMOS input port with pull-up resistor.<br>Can be used for key return input of key matrix. This port can release standby mode when at least one of pins goes low. | — | Input |
| 23<br>24<br>25<br>26 | $\mathrm{P0C_0}$<br>$\mathrm{P0C_1}$<br>$\mathrm{P0C_2}$<br>$\mathrm{P0C_3}$ | 4-bit N-ch open-drain output port.<br>Can be used for key source output of key matrix. This port retains output level immediately before standby mode is set when standby mode is set, and outputs low level on reset. | N-ch open-drain | Low-level output |
| 27<br>28<br>1<br>2 | $\mathrm{P0D_0}$<br>$\mathrm{P0D_1}$<br>$\mathrm{P0D_2}$<br>$\mathrm{P0D_3}$ | 4-bit N-ch open-drain output port.<br>Can be used for key source output of key matrix. This port retains output level immediately before standby mode is set when standby mode is set, and outputs low level on reset. | N-ch open-drain | Low-level output |
| 4<br>5<br>6<br>7 | $\mathrm{P0E_0}$<br>$\mathrm{P0E_1}$<br>$\mathrm{P0E_2}$<br>$\mathrm{P0E_3}$ | 4-bit I/O port which can be set in input or output mode in bit units.<br>In output mode, this port serves as high-current CMOS output port.<br>In input mode, it serves as CMOS input port to which pull-up resistor can be connected by program in bit units. On reset, this port is set as input port. | CMOS push-pull | Input |
| 8 | REM | Infrared remote controller transmission output pin. Outputs low level on reset. | CMOS push-pull | Low-level output |
| 13 | $\overline{\mathrm{RESET}}$ | System reset input pin. By inputting low level to this pin, CPU can be reset. While low level is input to this pin, oscillation circuit stops oscillating.<br>$\overline{\mathrm{RESET}}$ pin of μPD17P218 is provided with pull-up resistor. | — | Input |
| 9 | $\mathrm{V_{DD}}$ | Positive power supply pin | — | — |
| 12 | GND | Ground | — | — |
| 3 | INT | External interrupt request input | — | Input |
| 14 | $\overline{\mathrm{WDOUT}}$ | Output for detection of hang-up or voltage drop.<br>Outputs low level when watchdog timer overflows, when stack overflows/underflows, or when low voltage is detected. Connect this pin to $\overline{\mathrm{RESET}}$ pin. | N-ch open-drain | High-impedance or low-level output |
| 11<br>10 | $\mathrm{X_{IN}}$<br>$\mathrm{X_{OUT}}$ | Connect ceramic oscillator for system clock oscillation across these pins. | — | (Oscillation stops) |

### 2.2 IN PROM PROGRAMMING MODE

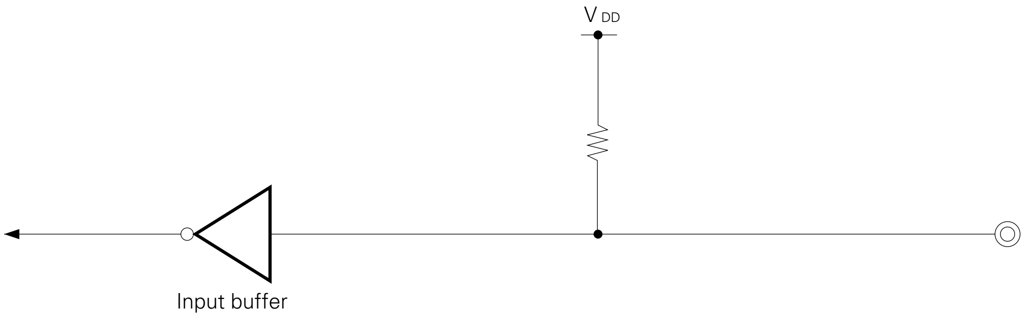
| Pin No. | Symbol | Function | Output Format | On Reset |
|---|---|---|---|---|
| 3 | $V_{PP}$ | Power supply for PROM programming.<br>Apply 12.5 V to this pin as the program voltage when writing/verifying program memory. | — | — |
| 9 | $V_{DD}$ | Positive power supply. Apply 6 V to this pin when writing/ verifying program memory. | — | — |
| 11 | CLK | Inputs clock for PROM programming. | — | — |
| 12 | GND | Ground | — | — |
| 19<br>\|<br>22 | $MD_0$<br>\|<br>$MD_3$ | Input pins used to select operation mode when PROM is programmed. | — | Input |
| 23<br>\|<br>26<br>27<br>28<br>1<br>2 | $D_4$<br>\|<br>$D_7$<br>$D_0$<br>$D_1$<br>$D_2$<br>$D_3$ | Input/output 8-bit data for PROM programming. | CMOS push-pull | Input |

**Remarks:** Pins other than above are not used in the PROM programming mode. For the processing of the unused pins, refer to **PIN CONFIGURATION (2) PROM programming mode**.

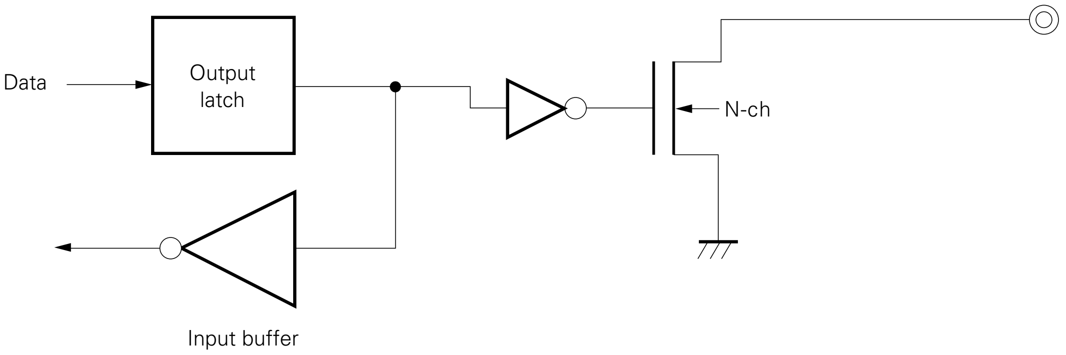
### 2.3 PIN I/O CIRCUITS

This section shows the I/O circuits of the $\mu$PD17P218 pins in simplified schematic diagrams.

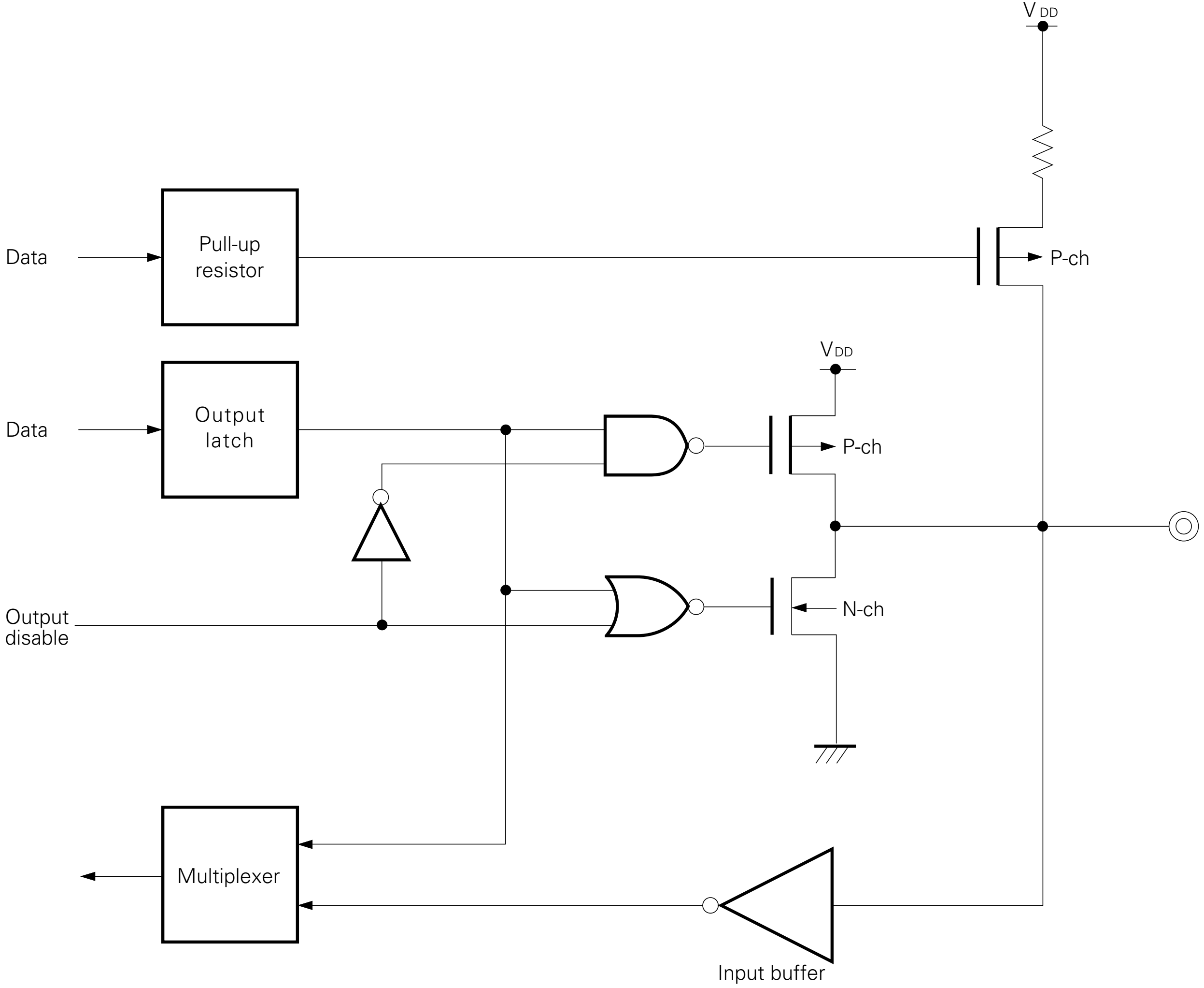
(1) $P0A_0$-$P0A_3$, $P0B_0/MD_0$-$P0B_3/MD_3$



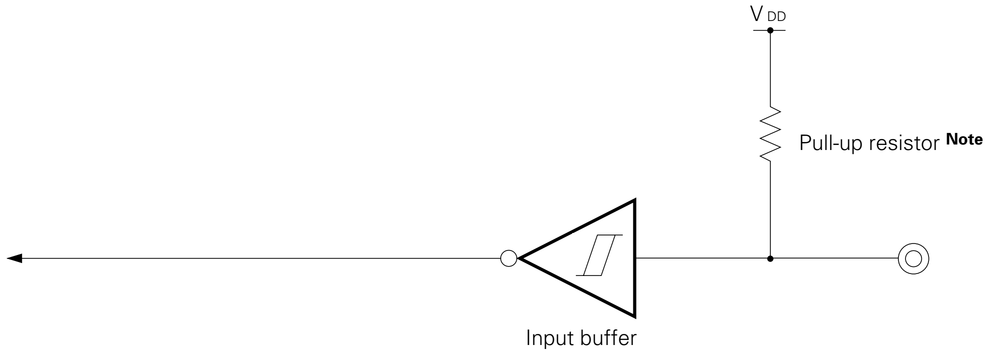
(2) $P0C_0/D_4$-$P0C_3/D_7$, $P0D_0/D_0$-$P0D_3/D_3$



(3) $P0E_0$-$P0E_3$



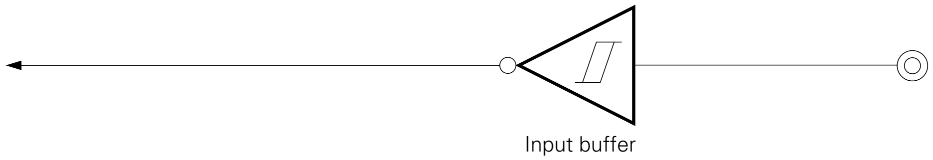
(4) $\overline{\text{RESET}}$



**Note**: Can be selected with mask option when mask products such as μPD17215, 17216, 17217, and 17218 are used.

**Remarks:** Schmitt trigeer input with hysteresis characteristics

(5) INT (Schmitt trigger input)



**Remarks:** Schmitt trigeer input with hysteresis characteristics

## 2.4 PROCESSING OF UNUSED PINS ★

Process the unused pins as follows:

Table 2-1 Processing of Unused Pins

| Pin | Recommended Connection |
|---|---|
| P0A$_0$-P0A$_3$ | Connect to $V_{DD}$ |
| P0B$_0$-P0B$_3$ | Connect to $V_{DD}$ |
| P0C$_0$-P0C$_3$ | Connect to GND |
| P0D$_0$-P0D$_3$ | Connect to GND |
| P0E$_0$-P0E$_3$ | Input : Connect to $V_{DD}$ or GND<br>Output : Open |
| REM | Open |
| INT | Connect to GND |
| $\overline{\text{WDOUT}}$ | Connect to GND |

## 2.5 NOTES ON USING INT AND $\overline{\text{RESET}}$ PINS ★

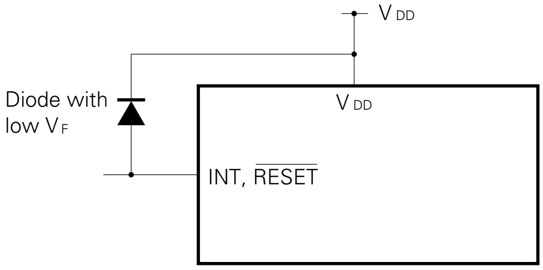
In addition to the functions shown in **2 PIN FUNCTIONS**, the INT and $\overline{\text{RESET}}$ pins also have a function to set a test mode (for IC testing) in which the internal operations of the μPD17P218 are tested.

When a voltage higher than $V_{DD}$ is applied to either of these pins, the test mode is set. This means that, even during normal operation, the μPD17P218 may be set in the test mode and malfunction if a noise exceeding $V_{DD}$ is applied.

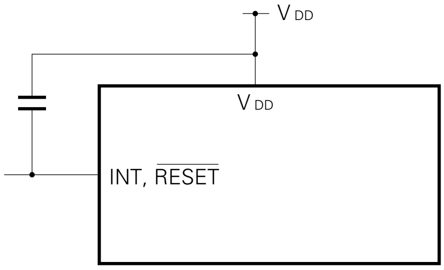
For example, if the wiring length of the INT or $\overline{\text{RESET}}$ pin is too long, noise superimposed on the wiring line of the pin may cause the above problem.

Therefore, keep the wiring length of these pins as short as possible to suppress the noise; otherwise, take noise preventive measures as shown below by using external components.

- **Connect diode with low $V_F$ between $V_{DD}$ and INT/$\overline{\text{RESET}}$ pin**



- **Connect capacitor between $V_{DD}$ and INT/$\overline{\text{RESET}}$ pin**



Moreover, if the test mode is set by the INT pin, low level is output from the $\overline{\text{WDOUT}}$ pin. In this case, connect the $\overline{\text{WDOUT}}$ pin to the $\overline{\text{RESET}}$ pin.

## 3. WRITING/VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The program memory of the μPD17P218 is a one-time PROM of 8192 x 16 bits. To write data to or verify this one-time PROM, the pins shown in the following table are used. No address input pin is used, as the address is updated by the clock input from the CLK pin.

**Table 3-1 Pins Used to Write/Verify Program Memory**

| Pin Name | Function |
|---|---|
| $V_{PP}$ | Applies voltage when program memory is written/verified.<br>Apply +12.5 V to this pin. |
| $V_{DD}$ | Positive power supply.<br>Apply +6 V to write/verify program memory. |
| CLK | Input clock to update address when program memory is written/verified.<br>Program memory address is updated when four pulses are input to this pin. |
| $MD_0$-$MD_3$ | Select operation mode when program memory is written/verified. |
| $D_0$-$D_7$ | Input/output 8-bit data when program memory is written/verified. |

### 3.1 OPERATION MODE FOR WRITING/VERIFICATION OF PROGRAM MEMORY

If +6 V is applied to the $V_{DD}$ and +12.5 V to the $V_{PP}$ pin after μPD17P218 has been placed in the reset status for a fixed time ($V_{DD}$ = 5V, $\overline{\text{RESET}}$ = 0V), μPD17P218 enters program memory write/verify mode.

The $MD_0$ to $MD_3$ pins are used to set the operating modes listed in the following table.

Leave the pins not used for program memory writing/verification open or connect to GND through pull-down resistors (470 Ω) (Refer to **PIN CONFIGRATION (2) PROM programming mode**).

**Table 3-2 Operating Mode Specification**

| Operating Mode Specification | | | | | | Operating Mode |
|---|---|---|---|---|---|---|
| $V_{PP}$ | $V_{DD}$ | $MD_0$ | $MD_1$ | $MD_2$ | $MD_3$ | |
| +12.5 V | +6 V | H | L | H | L | Program memory address 0 clear mode |
| | | L | H | H | H | Write mode |
| | | L | L | H | H | Verify mode |
| | | H | × | H | H | Program inhibit mode |

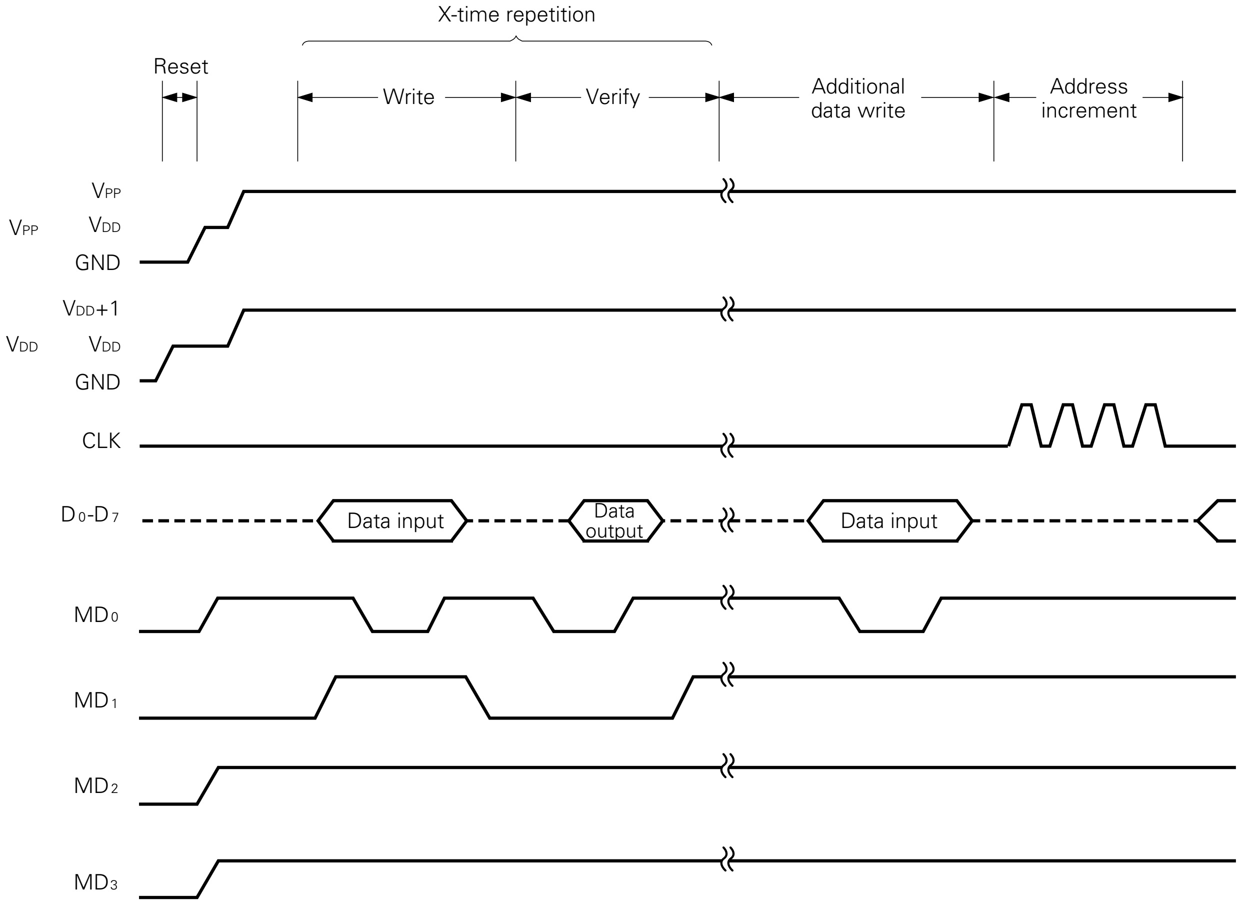
Remarks: ×: don't care (L or H)

### 3.2 PROGRAM MEMORY WRITE PROCEDURE

The program memory write procedure is as follows. High-speed program memory write is possible.

(1) Ground the unused pins through pull-down resistors. The CLK pin must be low.
(2) Supply 5 V to the $V_{DD}$ pin. The $V_{PP}$ pin must be low.
(3) After waiting for 10 microseconds, supply 5 V to the $V_{PP}$ pin.
(4) Operate the $MD_0$ to $MD_3$ pins to set program memory address 0 clear mode.
(5) Supply 6 V to the $V_{DD}$ pin and 12.5 V to the $V_{PP}$ pin.
(6) Set program inhibit mode.
(7) Write data in 1-millisecond write mode.
(8) Set program inhibit mode.
(9) Set verify mode. If data has been written connectly, proceed to step (10). If data has not yet been written, repeat steps (7) to (9).
(10) Write additional data for (the number of times data was written (×) in steps (7) to (9)) times 1 milliseconds.
(11) Set program inhibit mode.
(12) Supply a pulse to the CLK pin four times to update the program memory address by 1.
(13) Repeat steps (7) to (12) to the last address.
(14) Set program memory address 0 clear mode.
(15) Change the voltages of $V_{DD}$ and $V_{PP}$ pins to 5 V.
(16) Turn off the power supply.

Steps (2) to (12) are illustrated below.



**Remarks:** Broken line indicates high impedance.

### 3.3 PROGRAM MEMORY READ PROCEDURE

(1) Ground the unused pins through pull-down resistors. The CLK pin must be low.

(2) Supply 5 V to the $V_{DD}$ pin. The $V_{PP}$ pin must be low.

(3) After waiting for 10 microseconds, supply 5 V to the $V_{PP}$ pin.

(4) Operate the $MD_0$ to $MD_3$ pins to set program memory address 0 clear mode.

(5) Supply 6 V to the $V_{DD}$ pin and 12.5 V to the $V_{PP}$ pin.

(6) Set program inhibit mode.

(7) Set verify mode. Data of each address is sequentially output each time a clock pulse is input to the CLK pin four times.

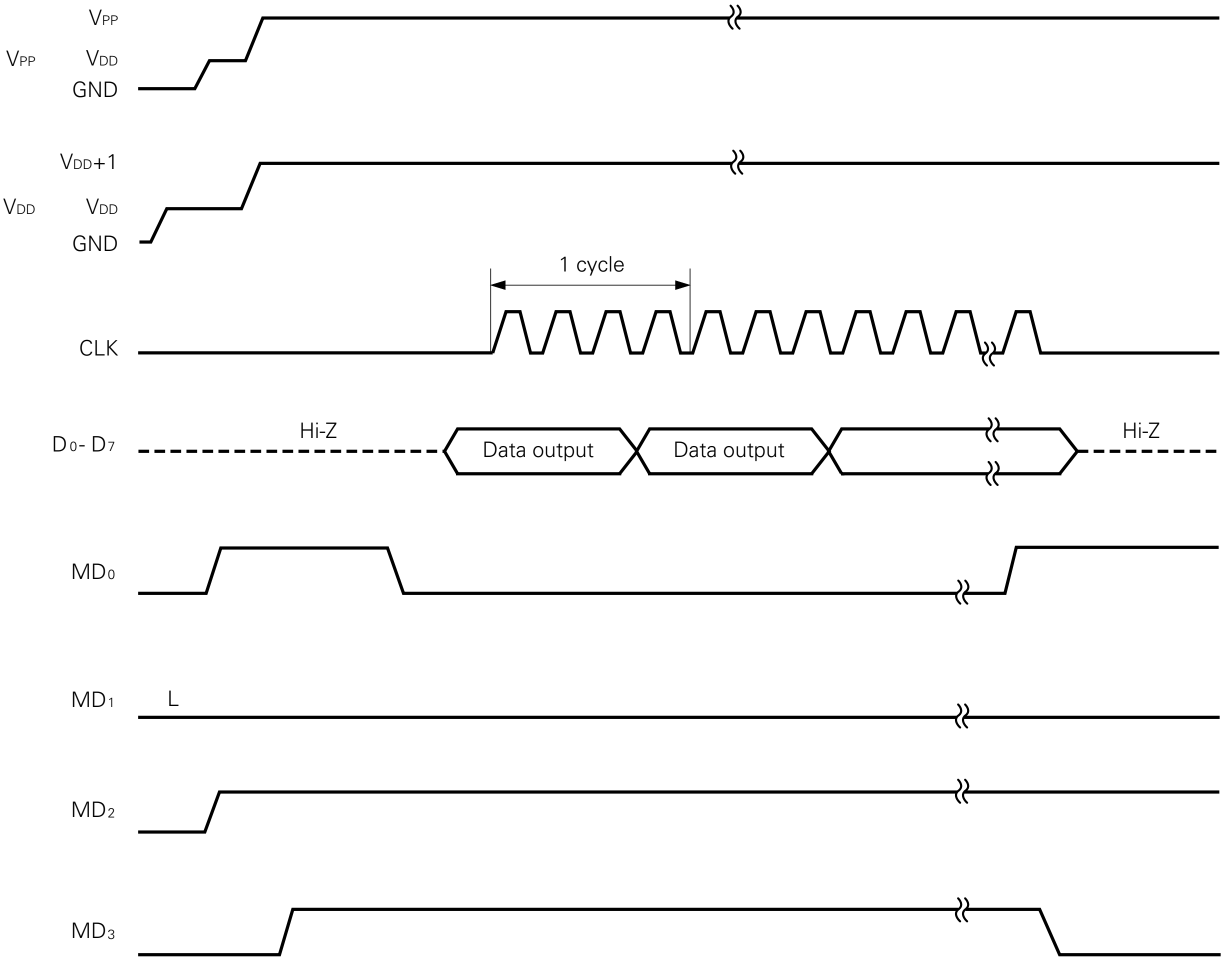
(8) Set program inhibit mode.

(9) Set program memory address 0 clear mode.

(10) Change the voltages of $V_{DD}$ and $V_{PP}$ pins to 5 V.

(11) Turn off the power supply.

Steps (2) to (9) are illustrated below.



## 4. ELECTRICAL SPECIFICATIONS (PRELIMINARY)

**ABSOLUTE MAXIMUM RATINGS** ($T_a$ = 25 °C)

| Item | Symbol | Conditions | | Ratings | Unit | |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | | –0.3 to +7.0 | V | |
| Input Voltage | $V_I$ | | | –0.3 to $V_{DD}$ +0.3 | V | |
| Output Voltage | $V_O$ | | | –0.3 to $V_{DD}$ +0.3 | V | |
| High-Level Output Current **Note** | $I_{OH}$ | REM pin | Peak value | –36.0 | mA | |
| | | | Effective value | –24.0 | mA | |
| | | 1 pin (P0E pin) | Peak value | –7.5 | mA | |
| | | | Effective value | –5.0 | mA | |
| | | Total of P0E pins | Peak value | –22.5 | mA | |
| | | | Effective value | –15.0 | mA | |
| Low-Level Output Current **Note** | $I_{OL}$ | 1 pin | Peak value | 7.5 | mA | |
| | | | Effective value | 5.0 | mA | |
| | | Total of P0E pins | Peak value | 30.0 | mA | |
| | | | Effective value | 20.0 | mA | |
| | | Total of P0C, P0D, $\overline{\text{WDOUT}}$ pins | Peak value | 22.5 | mA | |
| | | | Effective value | 15.0 | mA | |
| Operating Temperature | $T_{opt}$ | | | –40 to +85 | °C | ★ |
| Storage Temperature | $T_{stg}$ | | | –60 to +150 | °C | |
| Power dissipation | $P_d$ | $T_a$ = 85°C | | 180 | mW | ★ |

**Note**: Effective value = Peak value × $\sqrt{\text{Duty}}$. ★

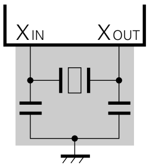
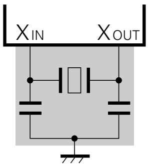
**Caution: Even if one of the parameters exceeds its absolute maximum rating even momentarily, the quality of the product may be degraded. The absolute maximum rating therefore specifies the upper or lower limit of the value at which the product can be used without physical damages. Be sure not to exceed or fall below this value when using the product.** ★

**RECOMMENDED OPERATING RANGE** ($V_{DD}$ = 2.0 to 5.5 V, $T_a$ = –40 to +85 °C) ★

| Item | Symbol | Conditions **Note** | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD1}$ | fx = 1 MHz | High-speed mode (16 μs) | 2.0 | 3.0 | 5.5 | V |
| | $V_{DD2}$ | fx = 4 MHz | Normal mode (8 μs) | | | | |
| | $V_{DD3}$ | | High-speed mode (4 μs) | 2.2 | 3.0 | 5.5 | |
| | $V_{DD4}$ | fx = 8 MHz | High-speed mode (2 μs) | 3.5 | 5.0 | 5.5 | |
| Oscillation Frequency | $f_X$ | | | 1.0 | 4.0 | 8.0 | MHz |

**Note**: Figures in parentheses indicate instruction execution time.

**SYSTEM CLOCK OSCILLATOR CIRCUIT CHARACTERISTICS** ($T_a$ = –40 to +85°C, $V_{DD}$ = 2.0 to 5.5 V)

| Oscillator | Recommended Constants | Item | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Ceramic Oscillator |  | Oscillation frequency ($f_X$) Note 1 | | 1.0 | 4.0 | 8.0 | MHz |
| | | Oscillation stabilization time Note 2 | After $V_{DD}$ has reached MIN value of oscillation voltage range | | | 4 | ms |
| ★ Crystal Oscillator |  | Oscillation frequency ($f_X$) Note 1 | | 1.0 | 4.0 | 8.0 | MHz |
| | | Oscillation stabilization time Note 2 | $V_{DD}$ = 4.5 to 5.5 V | | | 10 | ms |
| | | | | | | 30 | ms |

**Note 1**: The oscillation frequency indicates only the characteristics of the oscillation circuit.

**2**: The oscillation stabilization time is the time required for oscillation to stabilize after $V_{DD}$ has been applied or the STOP mode has been released.

**Caution: Wire the shaded portion in the above figures as follows to prevent adverse influence of wiring capacitance when the system clock oscillation circuit is used:**

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not place the wiring in the vicinity of lines through which a high alternating current flows.**
- **Always keep the ground of the capacitor of the oscillation circuit at the same potential as GND. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not extract a signal from the oscillation circuit.**

**DC CHARACTERISTICS** ($V_{DD}$ = 2.0 to 5.5 V, $T_a$ = –40 to +85 °C)

| Item | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-Level Input Voltage | $V_{IH1}$ | $\overline{\text{RESET}}$, INT pin | | $0.8V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | P0A, P0B | | $0.7V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH3}$ | P0E | $2.0 \text{ V} \leq V_{DD} < 3.0 \text{ V}$ | $V_{DD}–0.3$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | P0E | $3.0 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ | $V_{DD}–0.5$ | | $V_{DD}$ | V |
| | $V_{IH5}$ | $X_{IN}$ | | $0.8V_{DD}$ | | $V_{DD}$ | V |
| Low-Level Input Voltage | $V_{IL1}$ | $\overline{\text{RESET}}$, INT pins | | 0 | | $0.2V_{DD}$ | V |
| | $V_{IL2}$ | P0A, P0B | | 0 | | $0.3V_{DD}$ | V |
| | $V_{IL3}$ | P0E | | 0 | | $0.35V_{DD}$ | V |
| | $V_{IL4}$ | $X_{IN}$ | | 0 | | $0.2V_{DD}$ | V |
| High-Level Output Voltage | $V_{OH}$ | P0E, REM | $I_{OH}$ = –0.5 mA | $V_{DD}–0.3$ | | $V_{DD}$ | V |
| Low-Level Output Voltage | $V_{OL1}$ | P0C, P0D, REM, $\overline{\text{WDOUT}}$ | $I_{OL}$ = 0.5 mA | 0 | | 0.3 | V |
| | $V_{OL2}$ | P0E | $I_{OL}$ = 1.5 mA | 0 | | 0.3 | V |
| High-Level Input Current | $I_{IH}$ | $X_{IN}$ | $V_{IH} = V_{DD}$ | | | 20 | μA |
| Low-Level Input Current | $I_{IL}$ | $X_{IN}$ | $V_{IL}$ = 0 V | | | –20 | μA |
| High-Level Input Leakage Current | $I_{LIH}$ | INT, $\overline{\text{RESET}}$, P0A, P0B, P0E | $V_{IH} = V_{DD}$ | | | 3.0 | μA |
| Low-Level Input Leakage Current | $I_{LIL1}$ | INT | $V_{IL}$ = 0 V | | | –3.0 | μA |
| | $I_{LIL2}$ | P0E | $V_{IL}$ = 0 V<br>w/o pull-up resistor | | | –3.0 | μA |
| High-Level Output Current | $I_{OH}$ | REM | $V_{OH}$ = 1.0 V, $V_{DD}$ = 3 V | –6.0 | –13.0 | –24.0 | mA |
| High-Level Output Leakage Current | $I_{LOH}$ | P0C, P0D, P0E, $\overline{\text{WDOUT}}$ | $V_{OH} = V_{DD}$ | | | 3.0 | μA |
| Low-Level Output Leakage Current | $I_{LOL1}$ | $\overline{\text{WDOUT}}$ | $V_{OL}$ = 0 V | | | –3.0 | μA |
| | $I_{LOL2}$ | P0E | $V_{OL}$ = 0 V<br>w/o pull-up resistor | | | –3.0 | μA |
| Internal Pull-Up Resistor | $R_{U1}$ | $\overline{\text{RESET}}$, P0E | $V_{DD}$ = 3 V ± 10 % | 25 | 50 | 100 | kΩ |
| | | | $V_{DD}$ = 5 V ± 10 % | 25 | 50 | 100 | kΩ |
| | $R_{U2}$ | P0A, P0B | $V_{DD}$ = 3 V ± 10 % | 100 | 200 | 400 | kΩ |
| | | | $V_{DD}$ = 5 V ± 10 % | 100 | 200 | 400 | kΩ |
| Low-Voltage Detector Voltage | $V_{DT}$ | $\overline{\text{WDOUT}}$ = Low level, $V_{DT} = V_{DD}$ | | 0.5 | 1.4 | 2.0 | V ★ |

## ★ DC CHARACTERISTICS ($V_{DD}$ = 2.0 to 5.5 V, $T_a$ = –40 to +85 °C)

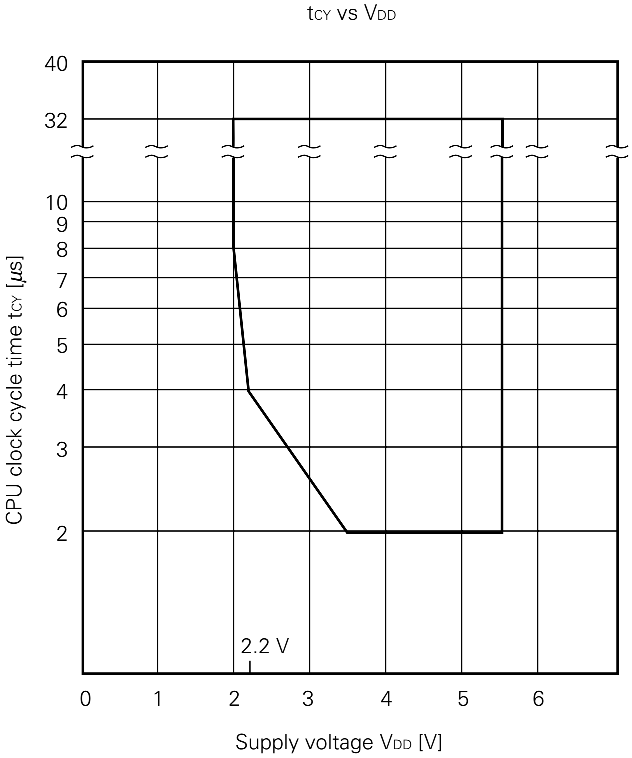
| Item | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Supply Current | $I_{DD1}$ | $f_X$ = 8 MHz | Operating mode (High-speed mode) | $V_{DD}$ = 5 V ± 10 % | | 3.8 | 7.6 | mA |
| | $I_{DD2}$ | $f_X$ = 8 MHz | HALT mode | $V_{DD}$ = 5 V ± 10 % | | 2.6 | 5.2 | mA |
| | $I_{DD3}$ | $f_X$ = 4 MHz | Operating mode (High-speed mode) | $V_{DD}$ = 5 V ± 10 % | | 2.3 | 4.6 | mA |
| | | | | $V_{DD}$ = 3 V ± 10 % | | 1.2 | 2.5 | mA |
| | | | Operating mode (Normal mode) | $V_{DD}$ = 5 V ± 10 % | | 2.0 | 4.0 | mA |
| | | | | $V_{DD}$ = 3 V ± 10 % | | 1.0 | 2.0 | mA |
| | | | | $V_{DD}$ = 2.0 to 2.2 V | | 0.55 | 1.1 | mA |
| | $I_{DD4}$ | $f_X$ = 4 MHz | HALT mode | $V_{DD}$ = 5 V ± 10 % | | 1.8 | 3.6 | mA |
| | | | | $V_{DD}$ = 3 V ± 10 % | | 1.0 | 2.0 | mA |
| | | | | $V_{DD}$ = 2.0 to 2.2 V | | 0.5 | 1.0 | mA |
| | $I_{DD5}$ | $f_X$ = 1 MHz | Operating mode (High-speed mode) | $V_{DD}$ = 3 V ± 10 % | | 0.7 | 2.1 | mA |
| | | | | $V_{DD}$ = 2.0 to 2.2 V | | 0.3 | 0.9 | mA |
| | $I_{DD6}$ | $f_X$ = 1 MHz | HALT mode | $V_{DD}$ = 3 V ± 10 % | | 0.6 | 1.8 | mA |
| | | | | $V_{DD}$ = 2.0 to 2.2 V | | 0.2 | 0.6 | mA |
| | $I_{DD7}$ | | STOP mode ($T_a$ = –40 to +85 °C) | $V_{DD}$ = 5 V ± 10 % | | 1 | 30 | μA |
| | | | | $V_{DD}$ = 3 V ± 10 % | | 1 | 20 | μA |
| | | | | $V_{DD}$ = 2.0 to 2.2 V | | 1 | 16 | μA |
| | $I_{DD8}$ | | STOP mode ($T_a$ = –20 to +70 °C) | $V_{DD}$ = 5 V ± 10 % | | 1 | 20 | μA |
| | | | | $V_{DD}$ = 3 V ± 10 % | | 1 | 10 | μA |
| | | | | $V_{DD}$ = 2.0 to 2.2 V | | 1 | 8 | μA |
| | $I_{DD9}$ | | STOP mode ($T_a$ = 25 °C) | $V_{DD}$ = 5 V ± 10 % | | 1 | 5 | μA |
| | | | | $V_{DD}$ = 3 V ± 10 % | | 1 | 5 | μA |
| | | | | $V_{DD}$ = 2.0 to 2.2 V | | 1 | 5 | μA |
| Data Retention Voltage | $V_{DDR}$ | $\overline{RESET}$ = Low level or in STOP mode | | | 1.3 | | 5.5 | V |

**AC CHARACTERISTICS** ($T_a$ = –40 to +85 °C)

| Item | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| CPU Clock Cycle Time Note<br>(Instruction Execution Time) | $t_{CY1}$ | $V_{DD}$ = 3.5 to 5.5 V | 1.99 | | 32.2 | μs |
| | $t_{CY2}$ | $V_{DD}$ = 2.2 to 5.5 V | 3.98 | | 32.2 | μs |
| | $t_{CY3}$ | $V_{DD}$ = 2.0 to 5.5 V | 7.96 | | 32.2 | μs |
| INT High-Level Width | $t_{IOH1}$ | $V_{DD}$ = 4.5 to 5.5 V | 10.0 | | | μs |
| | $t_{IOH2}$ | $V_{DD}$ = 2.0 to 5.5 V | 50.0 | | | μs |
| INT Low-Level Width | $t_{IOL1}$ | $V_{DD}$ = 4.5 to 5.5 V | 10.0 | | | μs |
| | $t_{IOL2}$ | $V_{DD}$ = 2.0 to 5.5 V | 50.0 | | | μs |
| $\overline{\text{RESET}}$ Low-Level Width | $t_{RSL1}$ | $V_{DD}$ = 4.5 to 5.5 V | 10.0 | | | μs |
| | $t_{RSL2}$ | $V_{DD}$ = 2.0 to 5.5 V | 50.0 | | | μs |

**Note:** CPU clock cycle time (instruction execution time) is determined depending on the connected oscillation frequency and SYSCK (RF: address 02H) in the register file.

The following figure shows CPU clock cycle time $t_{CY}$ characteristics versus supply voltage $V_{DD}$. ★



**DC PROGRAMMING CHARACTERISTICS** ($T_a$ = 25°C, $V_{DD}$ = 6.0 ± 0.25 V, $V_{PP}$ = 12.5 ± 0.3 V)

| Item | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| High-Level Input Voltage | $V_{IH1}$ | Other than CLK | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | CLK | $V_{DD}$ –0.5 | | $V_{DD}$ | V |
| Low-Level Input Voltage | $V_{IL1}$ | Other than CLK | 0 | | 0.3 $V_{DD}$ | V |
| | $V_{IL2}$ | CLK | 0 | | 0.4 | V |
| Input Leakage Current | $I_{LI}$ | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ | | | 10 | μA |
| High-Level Output Voltage | $V_{OH}$ | $I_{OH}$ = –1 mA | $V_{DD}$ –1.0 | | | V |
| Low-Level Output Voltage | $V_{OL}$ | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| $V_{DD}$ Supply Current | $I_{DD}$ | | | | 30 | mA |
| $V_{PP}$ Supply Current | $I_{PP}$ | MD0 = $V_{IL}$, MD1 = $V_{IH}$ | | | 30 | mA |

**Caution 1: $V_{PP}$ must not exceed +13.5 V, including the overshoot.**

**2: Apply $V_{DD}$ before $V_{PP}$ and disconnect it after $V_{PP}$.**

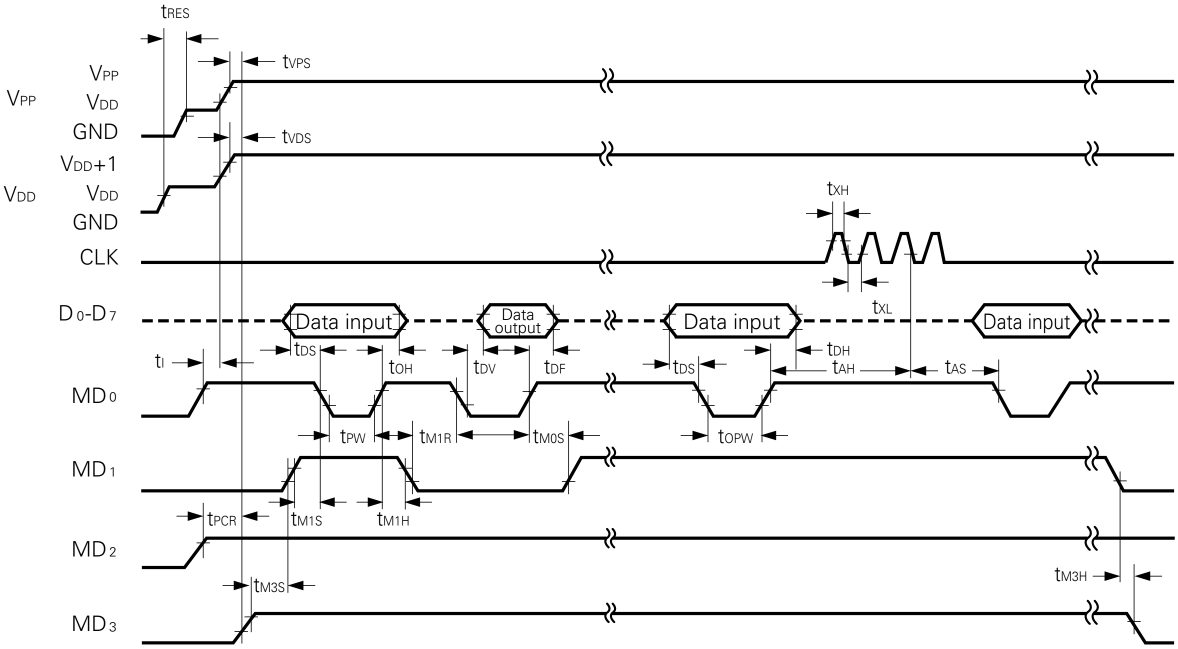
### AC PROGRAMMING CHARACTERISTICS ($T_a$ = 25°C, $V_{DD}$ = 6.0 ± 0.25 V, $V_{PP}$ = 12.5 ± 0.3 V)

| Item | Symbol | **Note 1** | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Address Setup Time **Note 2** (vs.MD0↓) | $t_{AS}$ | $t_{AS}$ | | 2 | | | μs |
| MD1 Setup Time (vs. MD0↓) | $t_{M1S}$ | $t_{OES}$ | | 2 | | | μs |
| Data Setup Time (vs. MD0↓) | $t_{DS}$ | $t_{DS}$ | | 2 | | | μs |
| Address Hold Time **Note 2** (vs.MD0↑) | $t_{AH}$ | $t_{AH}$ | | 2 | | | μs |
| Data Hold Time (vs. MD0↑) | $t_{DH}$ | $t_{DH}$ | | 2 | | | μs |
| MD0 ↑→ Data Output Float Delay Time | $t_{DF}$ | $t_{DF}$ | | 0 | | 130 | ns |
| $V_{PP}$ Setup Time (vs. MD3↑) | $t_{VPS}$ | $t_{VPS}$ | | 2 | | | μs |
| $V_{DD}$ Setup Time (vs. MD3↑) | $t_{VDS}$ | $t_{VCS}$ | | 2 | | | μs |
| Initial Program Pulse Width | $t_{PW}$ | $t_{PW}$ | | 0.95 | 1.0 | 1.05 | ms |
| Additional Program Pulse Width | $t_{OPW}$ | $t_{OPW}$ | | 0.95 | | 21.0 | ms |
| MD0 Setup Time (vs. MD1↑) | $t_{MOS}$ | $t_{CES}$ | | 2 | | | μs |
| MD0 ↓→ Data Output Delay Time | $t_{DV}$ | $t_{DV}$ | MD0 = MD1 = $V_{IL}$ | | | 1 | μs |
| MD1 Hold Time (vs. MD0↑) | $t_{M1H}$ | $t_{OEH}$ | $t_{M1H} + t_{M1R} \geqq 50$ μs | 2 | | | μs |
| MD1 Recovery Time (vs. MD0↓) | $t_{M1R}$ | $t_{OR}$ | | 2 | | | μs |
| Program Counter Reset Time | $t_{PCR}$ | – | | 10 | | | μs |
| CLK Input High-/Low- Level Width | $t_{XH}$,$t_{XL}$ | – | | 0.125 | | | μs |
| CLK Input Frequency | $f_X$ | – | | | | 4.19 | MHz |
| Initial Mode Set Time | $t_I$ | – | | 2 | | | μs |
| MD3 Setup Time (vs. MD1↑) | $t_{M3S}$ | – | | 2 | | | μs |
| MD3 Hold Time (vs. MD1↓) | $t_{M3H}$ | – | | 2 | | | μs |
| MD3 Setup Time (vs. MD0↓) | $t_{M3SR}$ | – | When data is read from program memory | 2 | | | μs |
| Address **Note 2** → Data Output Delay Time | $t_{DAD}$ | $t_{ACC}$ | When data is read from program memory | 2 | | | μs |
| Address **Note 2** → Data Output Hold Time | $t_{HAD}$ | $t_{OH}$ | When data is read from program memory | 0 | | 130 | ns |
| MD3 Hold Time (vs. MD0↑) | $t_{M3HR}$ | – | When data is read from program memory | 2 | | | μs |
| MD3 ↓→ Data Output Float Delay Time | $t_{DFR}$ | – | When data is read from program memory | 2 | | | μs |
| Reset Setup Time | $t_{RES}$ | | | 10 | | | μs |

**Note 1:** These symbols are the corresponding μPD27C256A symbols.

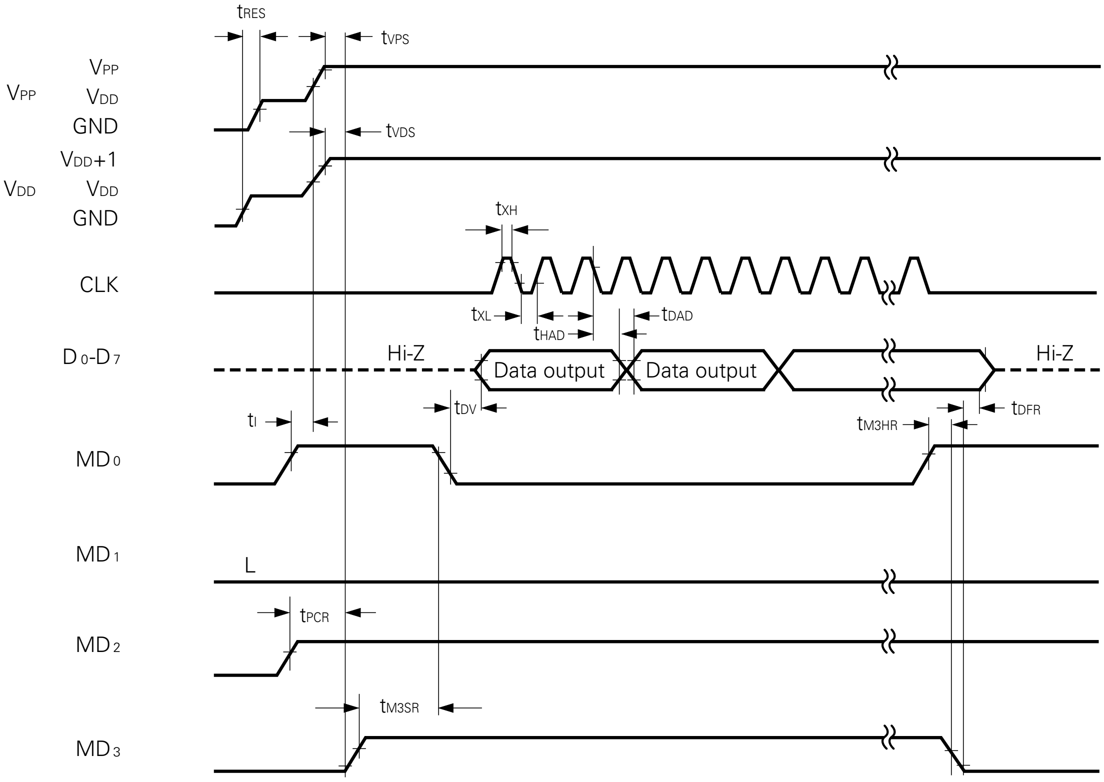
**2:** The internal address is incremented by 1 at the third falling edge of CLK (with four clocks constituting as one cycle). The internal address is not connected to any pin.

### PROGRAM MEMORY WRITE TIMING



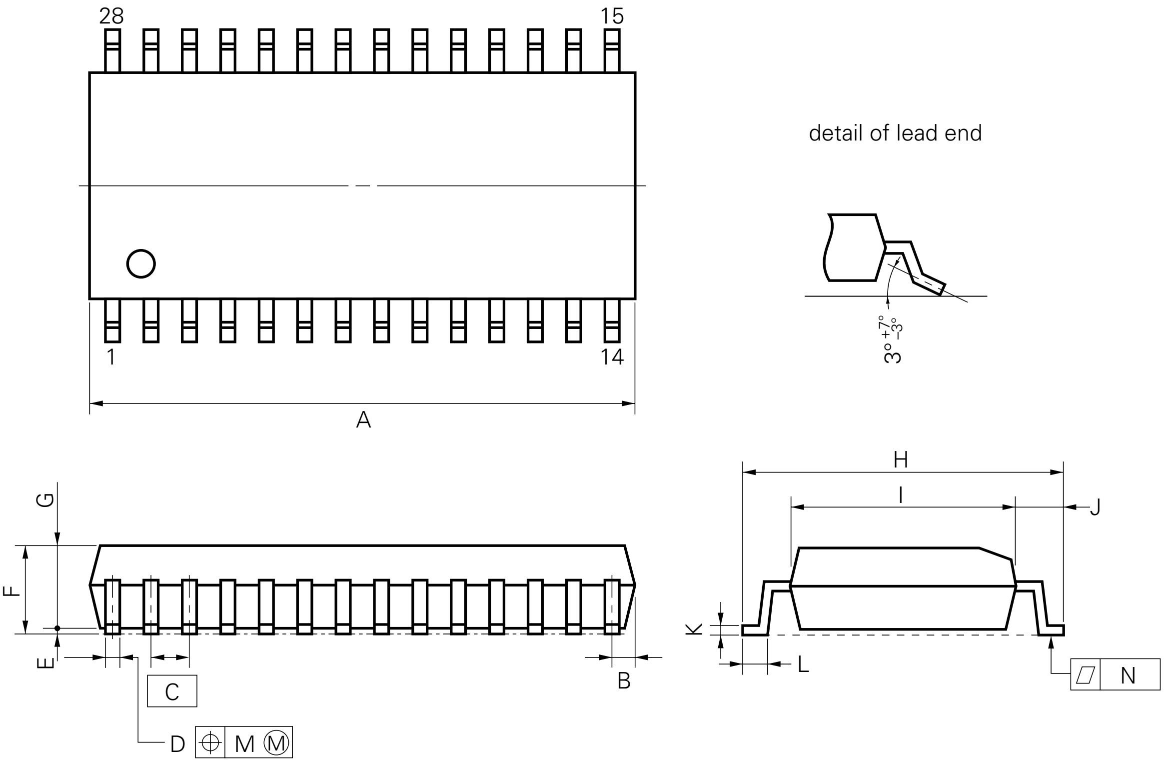
**Remarks:** Broken line indicates high impedance.

### PROGRAM MEMORY READ TIMING



## 5. PACKAGE DRAWINGS

### 28 PIN PLASTIC SOP (375 mil)



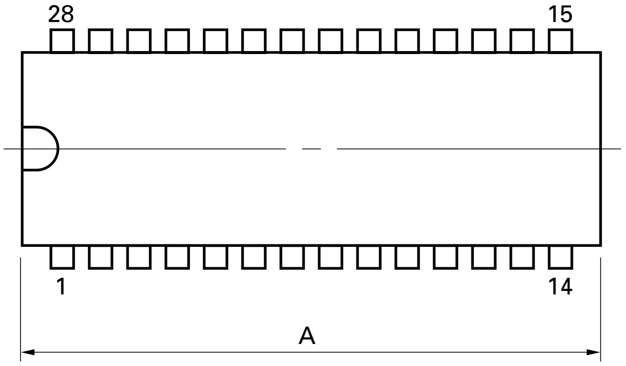
P28GM-50-375B-2

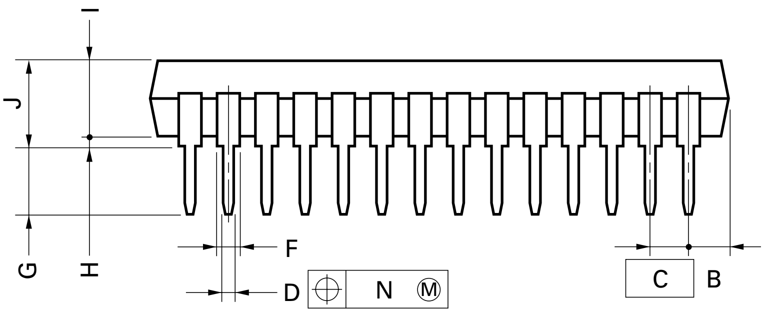
**NOTE**

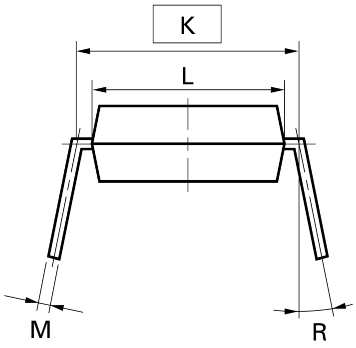
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 18.07 MAX. | 0.712 MAX. |
| B | 0.78 MAX. | 0.031 MAX. |
| C | 1.27 (T.P.) | 0.050 (T.P.) |
| D | $0.40^{+0.10}_{-0.05}$ | $0.016^{+0.004}_{-0.003}$ |
| E | 0.1±0.1 | 0.004±0.004 |
| F | 2.9 MAX. | 0.115 MAX. |
| G | 2.50 | 0.098 |
| H | 10.3±0.3 | $0.406^{+0.012}_{-0.013}$ |
| I | 7.2 | 0.283 |
| J | 1.6 | 0.063 |
| K | $0.15^{+0.10}_{-0.05}$ | $0.006^{+0.004}_{-0.002}$ |
| L | 0.8±0.2 | $0.031^{+0.009}_{-0.008}$ |
| M | 0.12 | 0.005 |
| N | 0.15 | 0.006 |

## 28 PIN PLASTIC SHRINK DIP (400 mil)







**NOTES**

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 28.46 MAX. | 1.121 MAX. |
| B | 2.67 MAX. | 0.106 MAX. |
| C | 1.778 (T.P.) | 0.070 (T.P.) |
| D | 0.50±0.10 | $0.020^{+0.004}_{-0.005}$ |
| F | 0.85 MIN. | 0.033 MIN. |
| G | 3.2±0.3 | 0.126±0.012 |
| H | 0.51 MIN. | 0.020 MIN. |
| I | 4.31 MAX. | 0.170 MAX. |
| J | 5.08 MAX. | 0.200 MAX. |
| K | 10.16 (T.P.) | 0.400 (T.P.) |
| L | 8.6 | 0.339 |
| M | $0.25^{+0.10}_{-0.05}$ | $0.010^{+0.004}_{-0.003}$ |
| N | 0.17 | 0.007 |
| R | 0~15° | 0~15° |

**S28C-70-400B-1**

## 6. RECOMMENDED SOLDERING CONDITIONS ★

For the μPD17P218, soldering must be performed under the following conditions.

For details of recommended conditions for surface mounting, refer to information document “Semiconductor device mounting technology manual” (IEI-1207).

For other soldering methods, please consult with NEC sales personnel.

### Table 6-1 Soldering Conditions of Surface-Mount Type

μPD17P218GT: 28-pin plastic SOP (375 mil)

| Soldering Method | Soldering Conditions | Recommended Conditions Reference Code |
|---|---|---|
| Infrared Reflow | Package peak temperature: 230 °C, Time: 30 seconds max. (more than 210 °C), Number of soldering operations: 1, Maximum number of days: 3 days Note (Afterwards, 20 hours prebaking at 125 °C is required) | IR30-203-1 |
| Pin Partial Heating | Pin temperature: 300 °C max., Time: 3 seconds max. (per side) | — |

**Note**: This means the number of days after unpacking the dry pack. Storage conditions are 25 °C and 65 % RH max.

**Caution: Do not use one soldering method in combination with another. (However, pin partial heating can be performed with other soldering methods.)**

### Table 6-2 Soldering Conditions of Through-Hole Type

μPD17P218CT: 28-pin plastic shrink DIP (400 mil)

| Soldering Method | Soldering Conditions |
|---|---|
| Wave Soldering (Only for lead part) | Solder bath temperature: 260 °C max., Time: 10 seconds max. |
| Pin Partial Heating | Pin temperature: 300 °C max., Time: 10 seconds max. |

**Caution: The wave soldering must be performed at the lead part only. Note that the solder must not be directly contacted to the package body.**

## ★ APPENDIX A. FUNCTION OF μPD17215 SUB-SERIES PRODUCTS

| Item / Product | μPD17215 | μPD17216 | μPD17217 | μPD17218 | μPD17P218 |
|---|---|---|---|---|---|
| ROM Capacity | 4K bytes (2048 x 16)<br>(mask ROM) | 8K bytes (4096 x 16)<br>(mask ROM) | 12K bytes (6144 x 16)<br>(mask ROM) | 16K bytes (8192 x 16)<br>(mask ROM) | 16K bytes (8192 x 16)<br>(one-time PROM) |
| RAM Capacity | 111 x 4 bits | | 223 x 4 bits | | |
| Infrared Remote Controller Carrier Generator Circuit (REM) | Provided (without LED output) | | | | |
| Number of I/O Ports | 20 | | | | |
| External Interrupt (INT) | 1 (rising-edge, falling-edge detection) | | | | |
| Timer | 2 channels { 8-bit modulo timer : 1 channel<br>Basic interval timer: 1 channel | | | | |
| Watchdog Timer | Provided ($\overline{\text{WDOUT}}$ output) | | | | |
| Low-Voltage Detector Circuit **Note** | Provided ($\overline{\text{WDOUT}}$ output) | | | | |
| Serial Interface | None | | | | |
| Stack | 5 levels (3 levels of multiplexed interrupts) | | | | |
| Instruction Execution Time | 2 μs (8-MHz ceramic oscillator: high-speed mode)<br>4 μs (4-MHz ceramic oscillator: high-speed mode)<br>16 μs (1-MHz ceramic oscillator: high-speed mode) | | | | |
| Operation of P0C and P0D in Standby Mode | Retain output level immediately before standby mode | | | | |
| Operating Voltage Range | 2.2 to 5.5 V (4 MHz, high-speed mode) | | | | |
| Standby Function | STOP mode, HALT mode | | | | |
| Package | 28-pin plastic SOP (375 mil)<br>28-pin plastic shrink DIP (400 mil) | | | | |

**Note :** Although the circuit configuration of the low-voltage detection circuit is identical, its electrical specifications differ depending on the product.

## APPENDIX B. DEVELOPMENT TOOLS ★

To develop the programs for the μPD17P218, the following development tools are available:

**Hardware**

| Name | Remarks |
|---|---|
| In-Circuit Emulator<br>IE-17K,<br>IE-17K-ET Note 1,<br>EMU-17K Note 2 | IE-17K, IE-17K-ET, and EMU-17K are the in-circuit emulators used in common with the 17K series microcomputer.<br>IE-17K and IE-17K-ET are connected to a PC-9800 series or IBM PC/AT™ as the host machine with RS-232C. EMU-17K is inserted into the expansion slot of a PC-9800 series. By using these in-circuit emulators with a system evaluation board corresponding to the microcomputer, the emulators can emulate the microcomputer. A higher level debugging environment can be provided by using man-machine interface SIMPLEHOST™.<br>EMU-17K also has a function by which you can check the contents of data memory real-time. |
| SE Board<br>(SE-17215) | This is an SE board for μPD17215 sub-series. It can be used alone to evaluate a system or in combination with an in-circuit emulator for debugging. |
| Emulation Probe<br>(EP-17K28CT) | EP-17K28CT is an emulation probe for 17K series 28-pin shrink DIP (400mil). |
| Emulation Probe<br>(EP-17K28GT) | EP-17K28GT is an emulation probe for 17K series 28-pin SOP (375 mil). When used with EV-9500GT-28 Note 3, it connects an SE board to the target system. |
| Conversion Adapter<br>(EV-9500GT-28 Note 3) | EV-9500GT-28 is a conversion adapter for 28-pin SOP (375 mil) and is used to connect EP-17K28GT to the target system. |
| PROM Programmer<br>(AF-9703 Note 4,<br>AF-9704 Note 4, 5,<br>AF-9706 Note 4) | AF-9703, AF-9704, and AF-9706 are PROM programmers corresponding to μPD17P218. By connecting program adapter AF-9808J or AF-9808H to this PROM programmer, μPD17P218 can be programmed. |
| Program Adapter<br>(AF-9808J Note 4,<br>AF-9808H Note 4) | AF-9808J and AF-9808H are adapters that is used to program μPD17P218CT and μPD17P218GT respectively, and is used in combination with AF-9703, AF-9704, or AF-9706. |

**Note 1:** Low-cost model: External power supply type

**2:** This is a product from IC Corp. For details, consult IC Corp.

**3:** Two EV-9500GT-28s are supplied with the EP-17K28GT. Five EV-9500GT-28s are optionally available as a set.

**4:** These are products from Ando Electric. For details, consult Ando Electric.

**5:** Maintenance product (This is no longer produced.)

**Software**

| Name | Outline | Host Machine | OS Media | Supply | Order Code |
|---|---|---|---|---|---|
| 17K Series Assembler (AS17K) | AS17K is an assembler that can be used in common with the 17K series products. When developing the program of the μPD17P218, AS17K is used in combination with a device file (AS17215, AS17216, AS17217, or AS17218). | PC-9800 series | MS-DOS™ | 5" 2HD | μS5A10AS17K |
| | | | | 3.5" 2HD | μS5A13AS17K |
| | | IBM PC/AT | PC DOS™ | 5" 2HC | μS7B10AS17K |
| | | | | 3.5" 2HC | μS7B13AS17K |
| Device File<br>AS17215<br>AS17216<br>AS17217<br>AS17218 | AS17215, AS17216, AS17217, and AS17218 are device files for μPD17215, 17216, 17217, and 17218 respectirely, and are used in combination with an assembler for the 17K series (AS17K). | PC-9800 series | MS-DOS | 5" 2HD | μS5A10AS17215 Note |
| | | | | 3.5" 2HD | μS5A13AS17215 Note |
| | | IBM PC/AT | PC DOS | 5" 2HC | μS7B10AS17215 Note |
| | | | | 3.5" 2HC | μS7B13AS17215 Note |
| Support Software (SIMPLE-HOST) | SIMPLEHOST is a software package that enables man-machine interface on the Windows™ when a program is developed by using an in-circuit emulator and a personal computer. | PC-9800 series | MS-DOS<br>Windows | 5" 2HD | μS5A10IE17K |
| | | | | 3.5" 2HD | μS5A13IE17K |
| | | IBM PC/AT | PC DOS | 5" 2HC | μS7B10IE17K |
| | | | | 3.5" 2HC | μS7B13IE17K |

**Note:** μS××××AS17215 includes AS17215, AS17216, AS17217, and AS17218.

**Remarks:** The corresponding OS versions are as follows:

| OS | Version |
|---|---|
| MS-DOS | Ver. 3.30 to Ver. 5.00A Note |
| PC DOS | Ver. 3.1 to Ver. 5.0 Note |
| Windows | Ver. 3.0 to Ver. 3.1 |

**Note:** Ver. 5.00/5.00A of MS-DOS and Ver. 5.0 of PC DOS have a task swap function, but this function cannot be used with this software.

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

**[MEMO]**

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