1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The μPD2102AL is a 1024 words by one bit static Random Access Memory requiring no clocks or refreshing. A family of devices with maximum access times ranging from 250 ns to 450 ns meet the requirements of microcomputer memory applications where speed, low cost and easy interfacing are prime design objectives.

All μPD2102AL inputs and outputs are TTL compatible. A single chip-enable ($\overline{CE}$) pin is provided for selection of an individual device in systems with OR-tied outputs. Output data is the same polarity as input data and is nondestructively read out. Only a single +5 volt supply is required. In standby mode, with the supply lowered to 1.5 volts, power dissipation is reduced to 42 mW max.

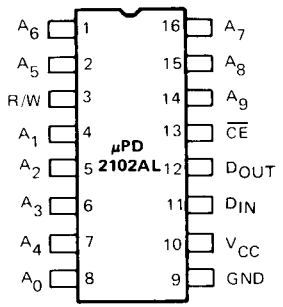
The μPD2102AL family is fabricated using NEC's N-channel MOS silicon gate process, providing excellent contamination protection. This process permits the use of a low cost plastic package (16 pin) and enables high performance, highly reliable MOS circuits to be produced.

3

FEATURES

- Access Time – μPD2102AL-2 – 250 ns Max
  μPD2102AL – 350 ns Max
  μPD2102AL-4 – 450 ns Max
- Single +5 Volts Supply Voltage
- Directly TTL Compatible – All Inputs and Output
- Static MOS – No Clocks or Refreshing Required
- Low Power – Typically 150 mW
- Low Standby Power – 42 mW max
- Three-State Output – OR-TIE Capability
- Simple Memory Expansion – Chip Enable Input
- Fully Decoded – On Chip Address Decode
- Inputs Protected – All Inputs have Protection against Static Charge
- Low Cost Packaging – 16 Pin Plastic Dual-In-Line Configuration

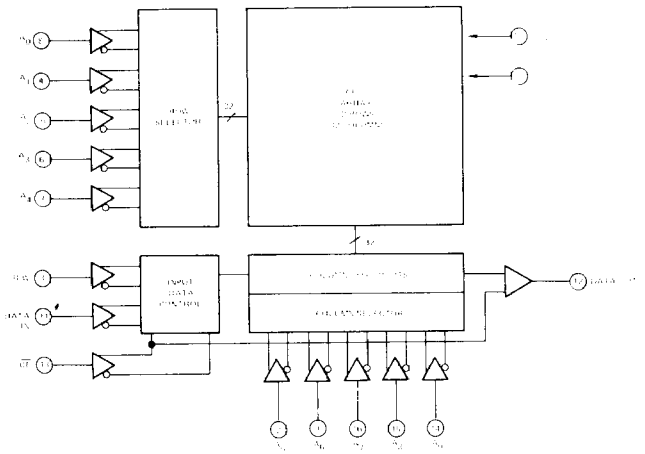
PIN CONFIGURATION



PIN NAMES

$A_0 - A_9$	Address Inputs
R/W	Read/Write
$\overline{CE}$	Chip Enable
V_{CC}	Power (+5V)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . -10°C to 70°C
Storage Temperature . . . . . -65°C to +125°C
Voltage On Any Pin . . . . . -0.5 to +7 Volts ①

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

*T_a = 25°C

DC CHARACTERISTICS

T_a = -10°C to +70°C; V_{CC} = 5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Leakage Current	I_{LI}			±10	μA	V_{IN} = 0 to 5.25V
I/O Leakage Current	I_{LOH}			+5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = +2.4V to V_{CC}
I/O Leakage Current	I_{LOL}			-10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
Power Supply Current	I_{CC1}		30	70	mA	All Inputs = 5.25V, Data Out Open
Input "Low" Voltage	V_{IL}	-0.5		+0.8	V	
Input "High" Voltage	V_{IH}	20		V_{CC}	V	
Output "Low" Voltage	V_{OL}			+0.4	V	I_{OL} = 2.1 mA
Output "High"	V_{OH}	2.4			V	I_{OH} = -100 μA

Note: ① Typical values are for T_a = 25°C and nominal supply voltage

CAPACITANCE

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		3	5	pf	V_{IN} = 0V
Output Capacitance	C_{OUT}		7	10	pf	V_{OUT} = 0V

AC CHARACTERISTICS

READ CYCLE

T_a = −10 C to +70 C; V_{CC} = +5V ±5% unless otherwise noted

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		2102AL-4		2102AL		2102AL-2			
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle	t_{RC}	450		350		250		ns	$t_T = t_r = t_f = 100$ ns $C_L = 100$ pF Load = 1 TTL Gate V_{ref} = 2.0 or 0.8V
Access Time	t_A		450		350		250	ns	
Chip Enable to Output Time	t_{CO}		230		180		130	ns	
Previous Read Data Valid in Respect to Address	t_{OH1}	40		40		40		ns	
Previous Read Data Valid in Respect to Chip Enable	t_{OH2}	0		0		0		ns	

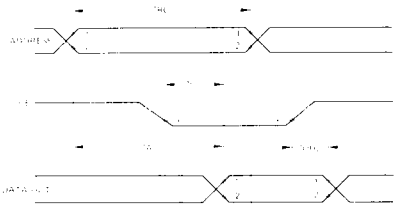
WRITE CYCLE

T_a = 10 C to +70 C; V_{CC} = +5V ± 5% unless otherwise noted

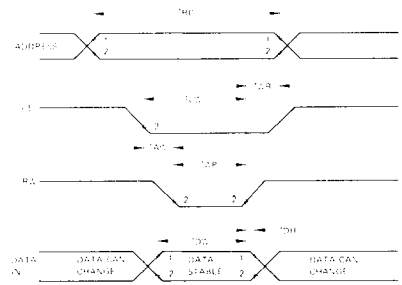
PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		2102AL-4		2102AL		2102AL-2			
		MIN	MAX	MIN	MAX	MIN	MAX		
Write Cycle	t_{WC}	450		350		250		ns	$t_T = t_r = t_f$ = 100 ns C_L = 100 pF Load = 1 TTL Gate V_{ref} = 2.0 or 0.8V
Address to Write Setup Time	t_{AW}	20		20		20		ns	
Write Pulse Width	t_{WP}	300		250		180		ns	
Write Recovery Time	t_{WR}	0		0		0		ns	
Data Setup Time	t_{DW}	300		250		180		ns	
Data Hold Time	t_{DH}	0		0		0		ns	
Chip Enable to Write Setup Time	t_{CW}	300		250		180		ns	

TIMING WAVEFORMS

READ CYCLE



WRITE CYCLE



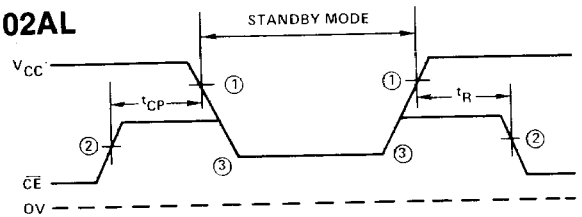
STANDBY CHARACTERISTICS

T_a 0 to +70 C

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
V_{CC} in Standby	V_{PD}	1.5			V	
$\overline{CE}$ Bias in Standby	V_{CES}	2.0			V	+2.0V ≤ V_{PD} ≤ +5.25V
		V_{PD}			V	+1.5V ≤ V_{PD} ≤ +2.0V
Standby Current Drain	I_{PD1}		14	28	mA	All Inputs, V_{PD1} = +1.5
Standby Current Drain	I_{PD2}		18	38	mA	All Inputs, V_{PD2} = +2.0V
Chip Deselect to Standby Time	t_{CP}	0			ns	
Standby Recovery Time	t_R	t_{RC} (1)			ns	

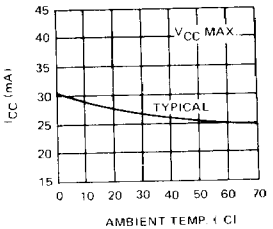
(1) t_{RC} Read Cycle Time

STANDBY MODE TIMING WAVEFORM

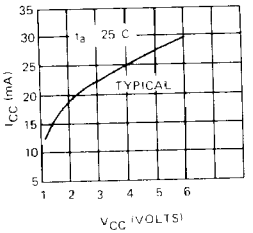


TYPICAL CHARACTERISTICS

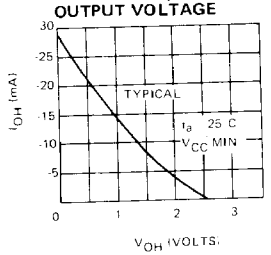
POWER SUPPLY CURRENT VS AMBIENT TEMPERATURE



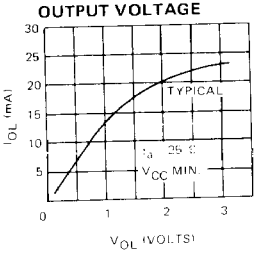
POWER SUPPLY CURRENT VS SUPPLY VOLTAGE



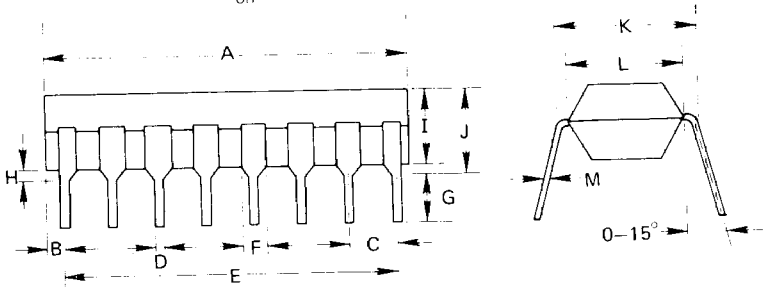
OUTPUT SOURCE CURRENT VS OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS OUTPUT VOLTAGE



PACKAGE OUTLINE μPD2102ALC



ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.05
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.35 MAX.	0.17 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01