

4096 BIT (1024 × 4 BITS) STATIC RAM

DESCRIPTION

The NEC μPD2114L is a 4096 bit static Random Access Memory organized as 1024 words by 4 bits using N-channel Silicon-gate MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding. It therefore requires **no clocks or refreshing to operate and simplifies system design. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.**

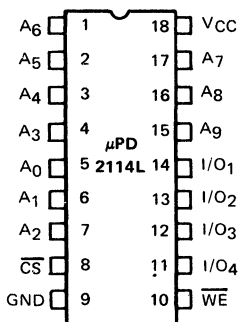
The μPD2114L is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The μPD2114L is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select (\overline{CS}) lead allows easy selection of an individual package when outputs are OR-Tied.

FEATURES

- Access Time: Selection from 150-450 ns
- Single +5 Volt Supply
- Directly TTL Compatible – All Inputs and Outputs
- Completely Static – No Clock or Timing Strobe Required
- Low Operating Power – Typically 0.06 mW/Bit
- Identical Cycle and Access Times
- Common Data Input and Output using Three-State Output
- High Density 18-pin Plastic and Ceramic Packages
- Replacement for 2114L and Equivalent Devices

PIN CONFIGURATION

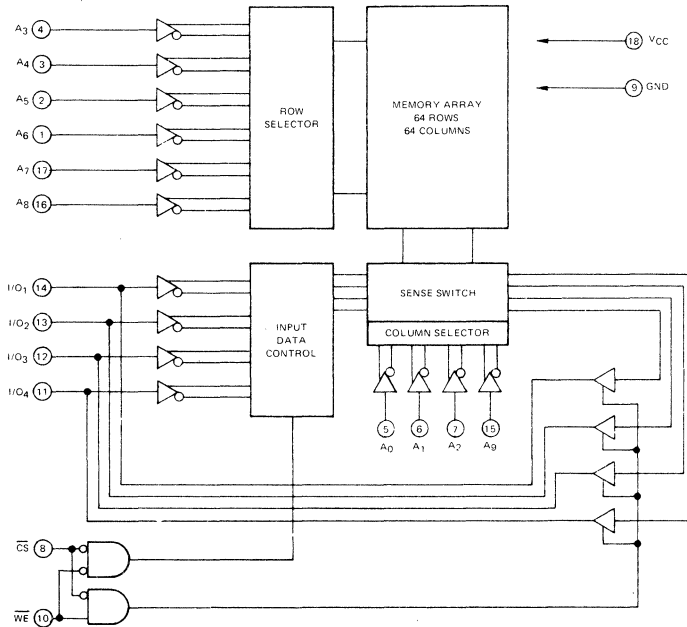


PIN NAMES

A ₀ -A ₉	Address Inputs
\overline{WE}	Write Enable
\overline{CS}	Chip Select
I/O ₁ -I/O ₄	Data Input/Output
VCC	Power (+5V)
GND	Ground

μ PD2114L

BLOCK DIAGRAM



Operating Temperature -10°C to $+80^{\circ}\text{C}$
 Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Voltage on any Pin -0.5 to 7 Volts 1

ABSOLUTE MAXIMUM RATINGS*

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* $T_a = 25^{\circ}\text{C}$

$T_a = 0^{\circ}\text{C}$ to 70°C ; $V_{CC} = +5\text{V} \pm 10\%$ unless otherwise noted.

DC CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Load Current (All Input Pins)	I_{LI}			10	μA	$V_{IN} = 0$ to 5.5V
I/O Leakage Current	I_{LO}			10	μA	$\overline{CS} = 2\text{V}$, $V_{I/O} = 0.4\text{V}$ to V_{CC}
Power Supply Current	I_{CC1}			65	mA	$V_{IN} = 5.5\text{V}$, $I_{I/O} = 0\text{mA}$, $T_a = 25^{\circ}\text{C}$
Power Supply Current	I_{CC2}			70	mA	$V_{IN} = 5.5\text{V}$, $I_{I/O} = 0\text{mA}$, $T_a = 0^{\circ}\text{C}$
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		6.0	V	
Output Low Current	I_{OL}	3.2			mA	$V_{OL} = 0.4\text{V}$
Output High Current	I_{OH}			-1.0	mA	$V_{OH} = 2.4\text{V}$, $V_{CC} = 4.75\text{V}$
						$V_{OH} = 2.2\text{V}$, $V_{CC} = 4.5\text{V}$

$T_a = 25^{\circ}\text{C}$; $f = 1.0\text{MHz}$

CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input/Output Capacitance	$C_{I/O}$			8	pf	$V_{I/O} = 0\text{V}$
Input Capacitance	C_{IN}			5	pf	$V_{IN} = 0\text{V}$

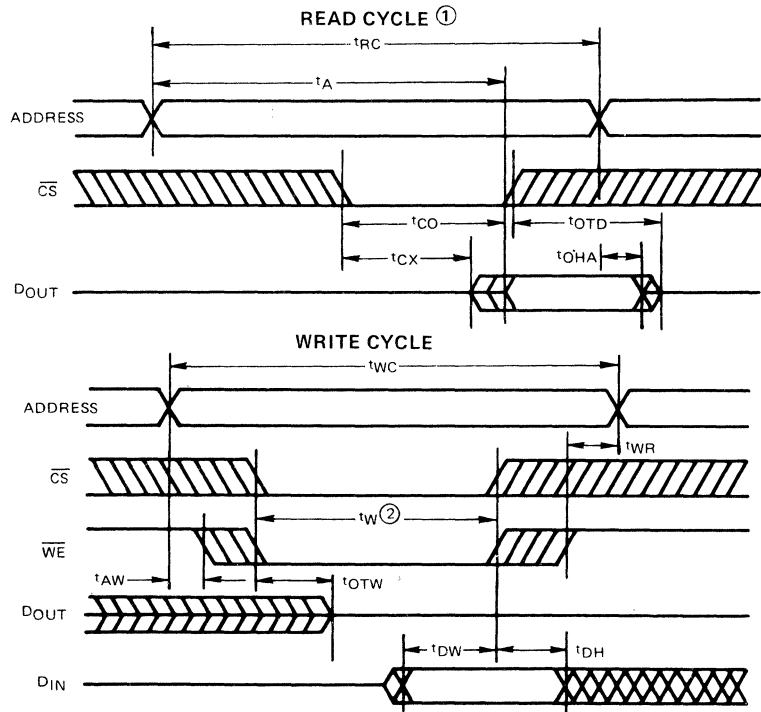
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS										UNIT	TEST CONDITIONS
		2114L		2114L-1		2114L-2		2114L-3		2114L-5			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE													
Read Cycle Time	t _{RC}	450		300		250		200		150		ns	t _T = t _r = t _f = 10 ns
Access Time	t _A		450		300		250		200		150	ns	C _L = 100 pF
Chip Selection to Output Valid	t _{CO}		120		100		80		70		60	ns	Load = 1 TTL gate
Chip Selection to Output Active	t _{CX}	20		20		20		20		20		ns	Input Levels = 0.8 and 2.0V
Output 3-State from Deselection	t _{OTD}		100		80		70		60		50	ns	V _{ref} = 1.5V
Output Hold from Address Change	t _{OHA}	50		50		50		50		50		ns	
WRITE CYCLE													
Write Cycle Time	t _{WC}	450		300		250		200		150		ns	t _T = t _r = t _f = 10 ns
Write Time	t _W	200		150		120		120		80		ns	C _L = 100 pF
Write Release Time	t _{WR}	0		0		0		0		0		ns	Load = 1 TTL gate
Output 3-State from Write	t _{OTW}		100		80		70		60		50	ns	Input Levels = 0.8 and 2.0V
Data to Write Time Overlap	t _{DW}	200		150		120		120		80		ns	V _{ref} = 1.5V
Data Hold from Write Time	t _{DH}	0		0		0		0		0		ns	
Address to Write Setup Time	t _{AW}	0		0		0		0		0		ns	

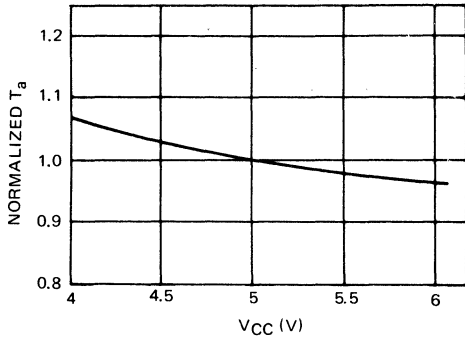


TIMING WAVEFORMS

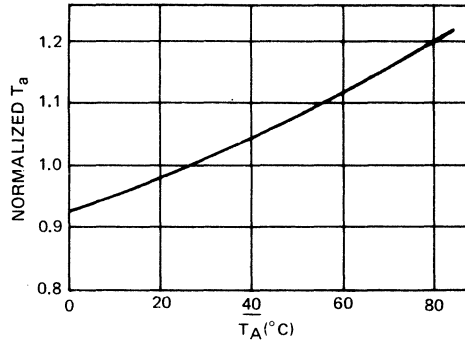


- Notes: ① \overline{WE} is high for Read Cycle
 ② t_W is measured from the latter of \overline{CS} or \overline{WE} going low to the earlier of \overline{CS} or \overline{WE} going high.

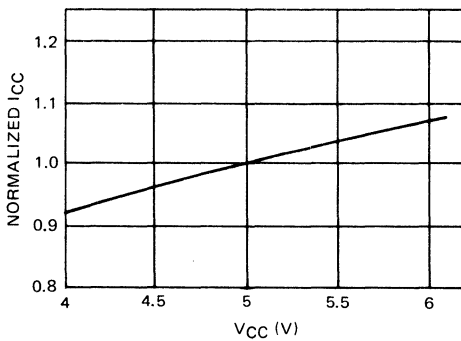
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



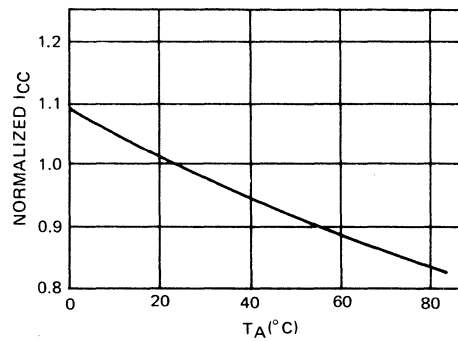
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



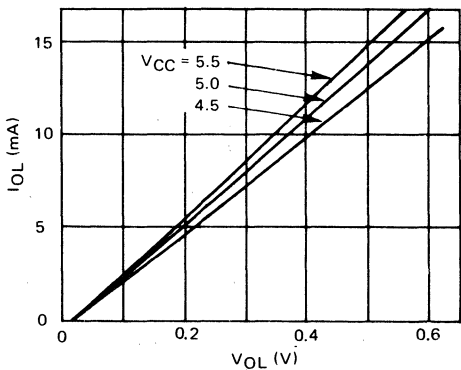
NORMALIZED POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE



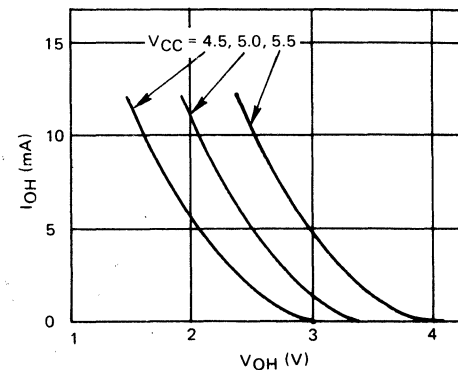
NORMALIZED POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE

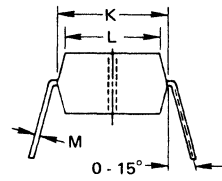
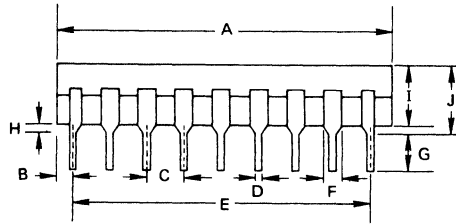


OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



μPD2114L

PACKAGE OUTLINES μPD2114LC

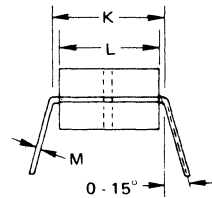
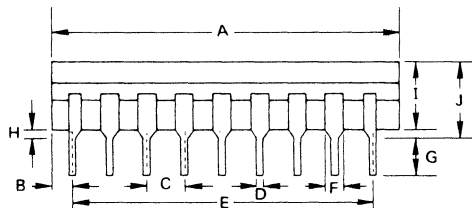


(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

3

μPD2114LD



(CERDIP)

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01