4096 x 1 BIT STATIC RAM

The μPD2147 is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit. Using a scaled NMOS technology, it incorporates an innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. The result is low standby power dissipation without the need for clocks, address setup and hold times. In addition, data rates are not reduced due to cycle times that are longer than access times.

$\overline{CS}$ controls the power down feature. In less than a cycle time after $\overline{CS}$ goes high – deselecting the μPD2147 – the part automatically reduces its power requirements and remains in this lower power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are deselected.

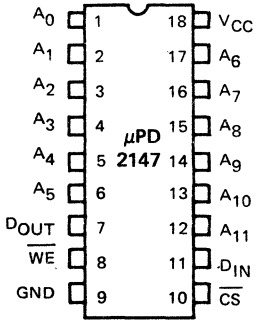
The μPD2147 is placed in an 18-pin ceramic package configured with the industry standard pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out non-destructively and has the same polarity as the input data. A data input and a separate three-state output are used.

FEATURES

- Scaled NMOS Technology
- Completely Static Memory – No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Single +5V Supply
- Automatic Power-Down
- High Density 18-Pin Package
- Directly TTL Compatible – All Inputs and Outputs
- Separate Data Input and Output
- Three-State Output
- Available in a Standard 18-Pin Ceramic Package
- 2 Performance Ranges:

	MAX ACCESS TIME	SUPPLY CURRENT	
		ACTIVE	STANDBY
μPD2147-2	70 ns	160 mA	20 mA
μPD2147-3	55 ns	160 mA	20 mA
μPD2147-5	45 ns	160 mA	20 mA

PIN CONFIGURATION



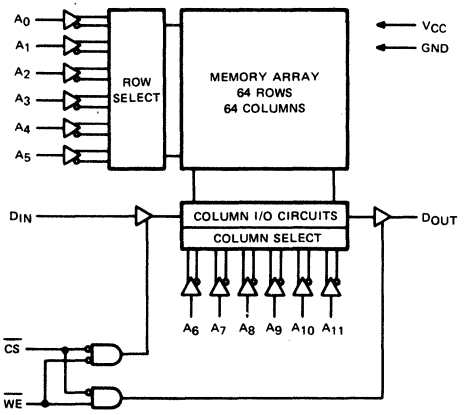
PIN NAMES

A_0-A_{11}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power (+5V)
GND	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +85°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin . . . . . −3.5V to +7 Volts ①
DC Output Current . . . . . 20 mA
Power Dissipation . . . . . 1.2 W

Note: ① with respect to ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%, unless otherwise noted. ①

PARAMETER	SYMBOL	LIMITS MIN	TYP ②	MAX	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}		0.01	10	μA	V_{CC} = Max, V_{IN} = GND to V_{CC}
Output Leakage Current	$\|I_{LO}\|$		0.01	10	μA	CS = V_{IH}, V_{CC} = Max, V_{OUT} = GND to V_{CC}
Operating Current	I_{CC}		120	150	mA	T_a = 25°C; V_{CC} = Max, CS = V_{IL}, Outputs Open
				160	mA	T_a = 0°C; V_{CC} = Max, CS = V_{IL}, Outputs Open
Standby Current	I_{SB}		12	20	mA	V_{CC} = Min to Max, $\overline{CS}$ = V_{IH}
Peak Power-On Current	I_{PO} ③		25	50	mA	V_{CC} = GND to V_{CC} = Min, $\overline{CS}$ = Lower of V_{CC} or V_{IH}Min
Input Low Voltage	V_{IL}	-3.0		0.8	V	
Input High Voltage	V_{IH}	2.0		6.0	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −4.0 mA
Output Short Circuit Current	I_{OS}	-150		+150	mA	V_{OUT} = GND to V_{CC}

Notes: ① The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
② Typical limits are V_{CC} = 5V, T_a = +25°C, and specified loading.
③ I_{CC} exceeds I_{SB} maximum during power on. A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected: otherwise, power-on current approaches I_{CC} active.

CAPACITANCE

$T_a = 25°C$; f = 1.0 MHz①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			5	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}			6	pF	V_{OUT} = 0V

Note: ① This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels . . . . . Gnd to 3.0 Volts
Input Rise and Fall Times . . . . . 5 ns
Input and Output Timing Reference Levels . . . . . 1.5 Volts
Output Load . . . . . See Figure 1

AC CHARACTERISTICS READ CYCLE

T_a = 0°C to +70°C; V_{CC} = +5V ± 10% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD2147-5 MIN	LIMITS μPD2147-5 MAX	LIMITS μPD2147-3 MIN	LIMITS μPD2147-3 MAX	LIMITS μPD2147-2 MIN	LIMITS μPD2147-2 MAX	UNIT	TEST CONDITIONS
Read Cycle Time	t_{RC}①	45		55		70		ns	
Address Access Time	t_{AA}		45		55		70	ns	
Chip Select Access Time	t_{ACS1}		45		55		70	ns	
Chip Select Access Time	t_{ACS2}		45		55		70	ns	
Output Hold From Address Change	t_{OH}	5		5		5		ns	
Chip Select to Output in Low Z	t_{CZ}②	10		10		10		ns	③
Chip Deselection to Output in High Z	t_{HZ}②	0	30	0	30	0	40	ns	④
Chip Selection to Power-Up Time	t_{PU}	0		0		0		ns	
Chip Selection to Power-Down Time	t_{PD}		20		20		30	ns	

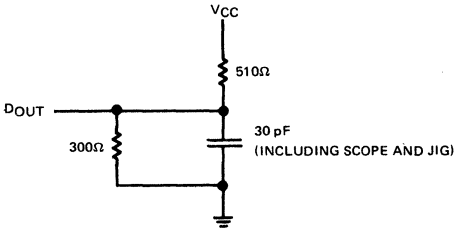
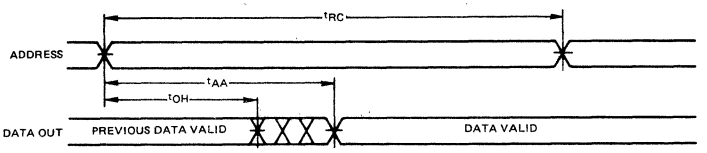


Figure 1

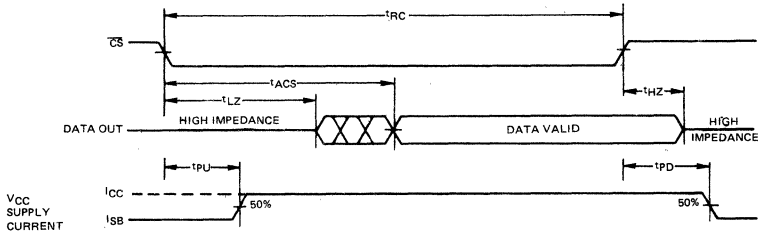
Notes: ① All Read Cycle timings are referenced from the last valid address to the first transitioning address.
② At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min. both for a given device and from device to device.
③ Transition is measured ±200 mV from steady state voltage with specified loading.
④ Transition is measured at V_{OL} +200 mV and V_{OH} −200 mV with specified loading.

TIMING WAVEFORMS
READ CYCLE

READ CYCLE NO. 1 ⑤⑥



READ CYCLE NO. 2 ⑤⑦



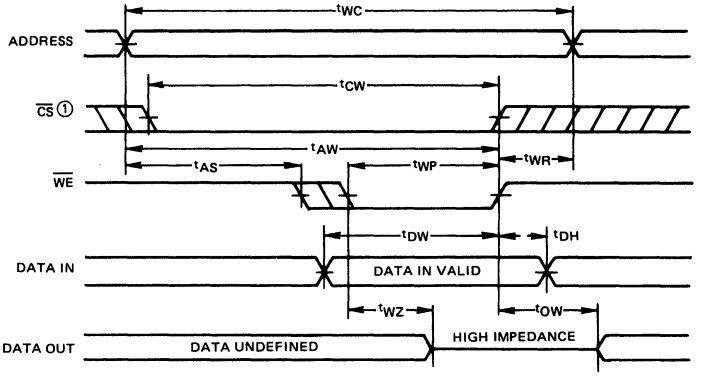
AC CHARACTERISTICS
WRITE CYCLE

PARAMETER	SYMBOL	LIMITS μPD2147-5 MIN	μPD2147-5 MAX	μPD2147-3 MIN	μPD2147-3 MAX	μPD2147-2 MIN	μPD2147-2 MAX	UNIT	TEST CONDITIONS
Write Cycle Time ②	t_{WC}	45		55		70		ns	
Chip Select to End of Write	t_{CW}	45		45		55		ns	
Address Valid to End of Write	t_{AW}	45		45		55		ns	
Address Setup Time	t_{AS}	0		0		0		ns	
Write Pulse Width	t_{WP}	25		25		40		ns	
Write Recovery Time	t_{WR}	0		10		15		ns	
Data Valid to End of Write	t_{DW}	25		25		30		ns	
Data Hold Time	t_{DH}	10		10		10		ns	
Write Enabled to Output with Z	t_{WZ}	0	25	0	25	0	35	ns	③
Output Active From End of Write	t_{OW}	0		0		0		ns	④

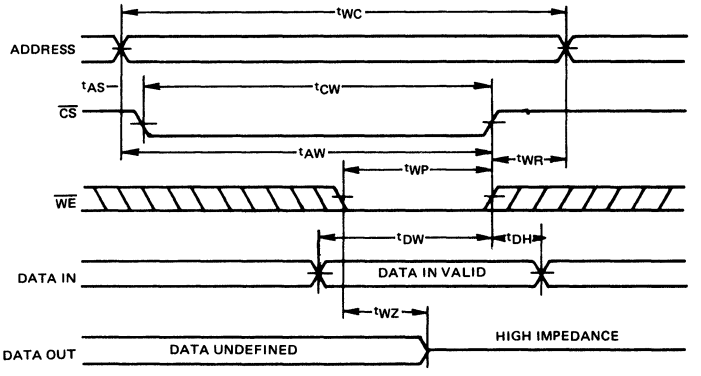
Notes: ① All Read Cycle timings are referenced from the last valid address to the first transitioning address.
② At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min. both for a given device and from device to device.
③ Transition is measured ±200 mV from steady state voltage with specified loading.
④ Transition is measured at V_{OL} +200 mV and V_{OH} −200 mV with specified loading.
⑤ WE is high for Read Cycles.
⑥ Device is continuously selected, $\overline{CS} = V_{IL}$.
⑦ Addresses valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORMS
WRITE CYCLE

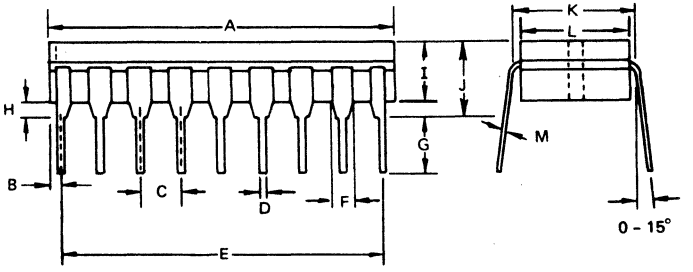
WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) ⑤



WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) ⑤



Notes: ① If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
② All Write Cycle timings are referenced from the last valid address to the first transitioning address.
③ Transition is measured at V_{OL} +200 mV and V_{OH} −200 mV with specified loading.
④ Transition is measured ±200 mW from steady state voltage with specified loading.
⑤ $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.



PACKAGE OUTLINE
μPD2147D

Ceramic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01