NEC
μPD2149
μPD2149-1
μPD2149-2
PRELIMINARY

4096 (1024x4) BIT STATIC RAM

3

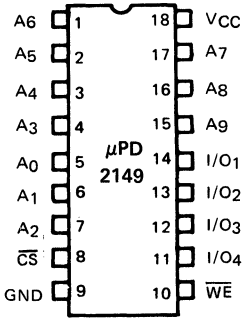
DESCRIPTION

The μPD2149 is a 4096-bit static Random Access Memory organized as 1024 words bv 4-bits. Using a scaled NMOS technology, it incorporates an innovative design approach which provides the ease-of-use features associated with non-clocked static memories.

The μPD2149 is encapsulated in an 18-pin ceramic package configured with the industry standard pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out non-destructively and has the same polarity as the input data.

FEATURES

- Completely Static Memory — No Clock or Timing Strobe Required
- Equal Access and Cycle Times, Faster Chip Select Access
- Single +5V Supply
- High Density 18-Pin Package
- Directly TTL Compatible — All Inputs and Outputs
- Common Input and Output
- Three-State Output
- Access Time: 35-55 ns MAX (From Address)
  15-25 ns MAX (From Chip Select)
- Power Dissipation: 180 mA MAX



PIN NAMES

A_0-A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O
H	X	Not Selected	High Z
L	L	Write	D_{IN}
L	H	Read	D_{OUT}

CAPACITANCE

$T_a = 25°C$; f = 1.0 MHz ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			5	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}			7	pF	V_{OUT} = 0V

AC TEST CONDITIONS

Note: ① This parameter is sampled and not 100% tested.

Input Pulse Levels . . . . . Gnd to 3.0V
Input Rise and Fall Times . . . . . 5 ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

AC CHARACTERISTICS READ CYCLE ①

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$, unless otherwise noted.

PARAMETER	SYMBOL	2149-2 MIN	2149-2 MAX	2149-1 MIN	2149-1 MAX	2149 MIN	2149 MAX	UNIT	TEST CONDITIONS
Read Cycle Time	T_{RC}	35		45		55		ns	
Access Time	T_A		35		45		55	ns	
Chip Selection to Output Valid	T_{CO}		15		20		25	ns	
Chip Selection to Output Active	T_{CX}	0		0		0		ns	
Output 3-State From Deselection	T_{OTD}		10		15		20	ns	②
Output Hold From Address Change	T_{OH}	0		0		0		ns	

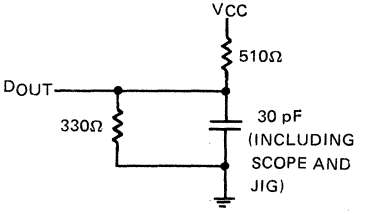


Figure 1

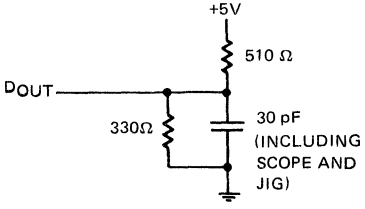
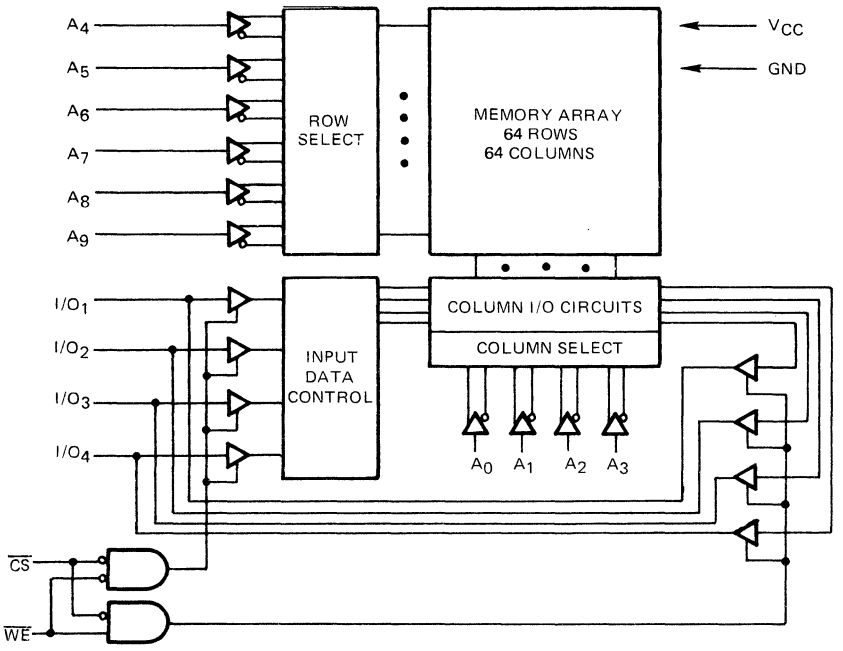


Figure 2

Notes: ① $\overline{WE}$ is high for read cycle.

② Transition is measured ±500 MV from steady state with load of Figure 2. This parameter is sampled and not 100% tested.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +85°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−0.5V to +7V ①
DC Output Current	20 mA
Power Dissipation	1.2W

Note: ① with respect to ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%, unless otherwise noted.

PARAMETER	SYMBOL	MIN	MAX	UNIT	TEST CONDITIONS
Input Leakage Current	I_{LI}	−10	+10	μA	V_{IN} = GND to V_{CC}
Ouput Leakage Current	I_{LO}	−50	+50	μA	CS = V_{IH} V_{OUT} = GND to 4.5V
Power Supply Current	I_{CC}		180	MA	V_{IN} = V_{CC}, I/O = open
Input Low Voltage	V_{IL}	−0.5	0.8	V	
Input High Voltage	V_{IH}	2.0	V_{CC}	V	
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8 MA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −4 MA
Output Short Circuit Current	I_{OS}	TBD	TBD	MA	V_{OUT} = GND to V_{CC}

Note: The operating temperature range is guaranteed with transverse air flow exceeding 400 feet per minute.

AC CHARACTERISTICS WRITE CYCLE

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%, unless otherwise noted.

PARAMETER	SYMBOL	2149-2 MIN	2149-2 MAX	2149-1 MIN	2149-1 MAX	2149 MIN	2149 MAX	UNIT	TEST CONDITIONS
Write Cycle Time	T_{WC}	35		45		55		ns	
Write Time	T_W		30		40		50	ns	①
Write Release Time	T_{WR}	5		5		5		ns	
Data to Write	T_{DW}	20		25		30		ns	
Output 3-State From Write	T_{OTW}		10		15		20	ns	②
Data Hold From Write Time	T_{DH}	5		5		5		ns	
Address to Write Setup Time	T_{AW}	0		0		0		ns	

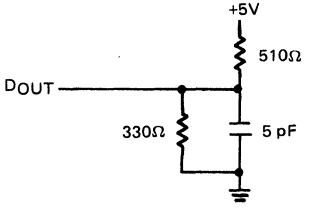
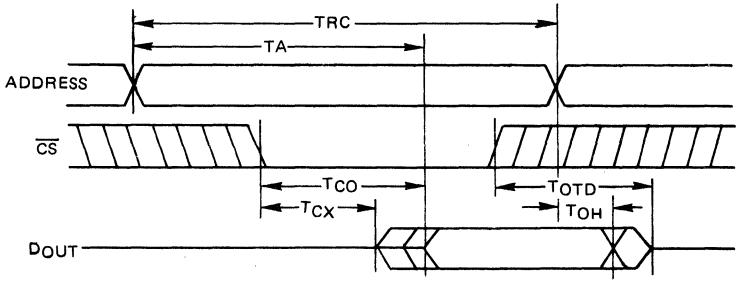


Figure 3

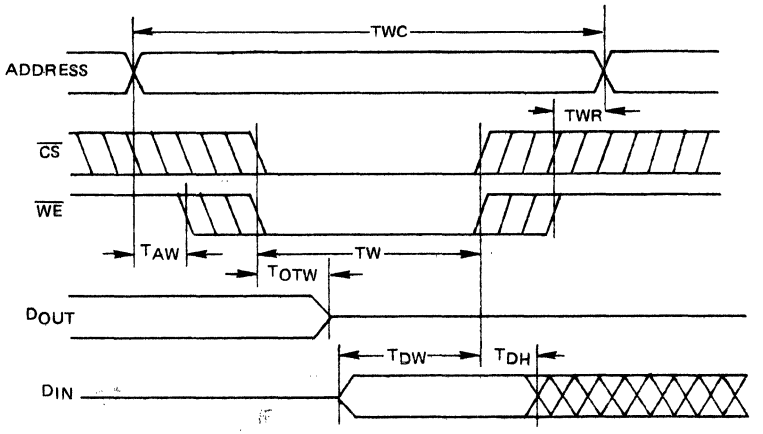
Notes:
① T_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.
② Transition is measured +500 MV from steady state with load of Figure 3. This parameter is sampled and not 100% tested.
③ $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.

TIMING WAVEFORMS

READ CYCLE ① ②

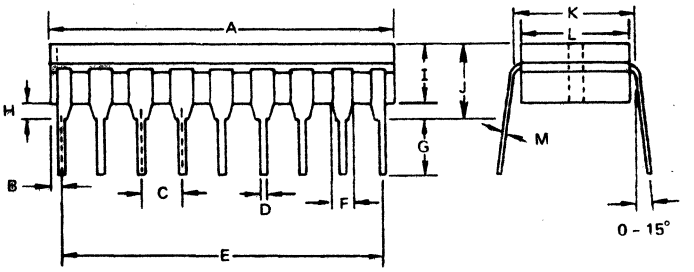


WRITE CYCLE ②



Notes: ① $\overline{WE}$ is high for read cycle.
② $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.

PACKAGE OUTLINE μPD2149D



Ceramic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01