Description

The μPD2167 is a 16,384-word by 1-bit static MOS RAM. Using a scaled-NMOS technology, its design provides the easy-to-use features associated with nonclocked static memories.

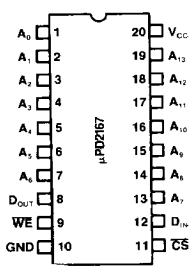
The μPD2167 has a three-state output and offers a standby mode that features an 83% savings in power consumption. The μPD2167 requires a single +5 volt supply and is fully TTL-compatible. It features equal access and cycle times and, because of its fully static operation, it requires no external clocks or timing strobes. It is packaged in a standard 20-pin, 300 mil DIP.

Features

- ☐ 16384 x 1 organization
- ☐ Fully static memory — no clock or timing strobe required
- ☐ Equal access and cycle times
- ☐ Single +5V supply
- ☐ Automatic power-down
- ☐ Standard 20-pin DIP, 300 mil
- ☐ All inputs and output directly TTL-compatible
- ☐ Separate data input and output
- ☐ Three-state output
- ☐ Power dissipation: 180 mA max (active)
  30 mA max (standby)
- ☐ 2 performance ranges:

Device	Access/Cycle Time	Power Supply	
		Active	Standby
μPD2167-3	55ns	180mA	30mA
μPD2167-2	70ns	180mA	30mA

Pin Configuration



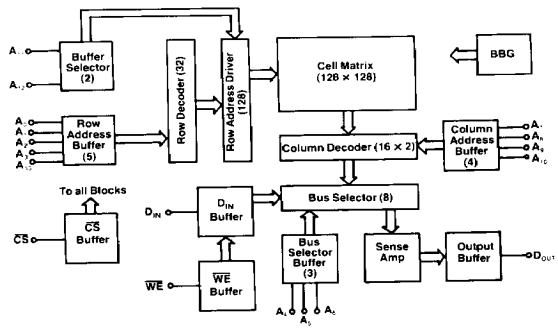
Pin Identification

Pin No.	Symbol	Description
1–7, 13–19	A_0–A_{13}	Address Inputs
8	D_{OUT}	Data Output
9	$\overline{WE}$	Write Enable
10	GND	Ground
11	$\overline{CS}$	Chip Select
12	D_{IN}	Data Input
20	V_{CC}	+5V Power Supply

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Not selected	High-Z	Standby
L	L	Write	High-Z	Active
L	H	Read	D_{OUT}	Active

Block Diagram



Absolute Maximum Ratings*

Temperature under bias	−10°C to +85°C
Storage temperature	−65°C to +150°C
Voltage on any pin with respect to ground	−3.5V to +7V
D.C. output current	20mA
Power dissipation	1.2W

*Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A=25°C, f=1.0 MHz

Parameter	Symbol	Max.	Unit	Test Conditions
Input Capacitance	C_{IN}	5	pF	V_{OUT} = 0V
Output Capacitance	C_{OUT}	6	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested.

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Rev/2

DC Characteristics
T_A=0°C to +70°C, V_{CC} = +5V ± 10%

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
Input load current all input pins	I_{LI}			10	μA	V_{CC} = max, V_{IN} = GND to V_{CC}
Output leakage current	I_{LO}		0.1	50	μA	$\overline{CS}$ = V_{IH}, V_{CC} = max, V_{OUT} = GND to V_{CC}
Operating current	I_{CC}			170	mA	T_A = 25°C | V_{CC} = max, $\overline{CS}$ = V_{IL}, output open
				180	mA	T_A = 0°C
Standby current	I_{SB}			30	mA	V_{CC} = min to max, $\overline{CS}$ = V_{IH}
Peak Power-On current	I_{PO} ①		35	70	mA	V_{CC} = GND to V_{CC} min. $\overline{CS}$ = Lower of V_{CC} or V_{IH} min.
Input low voltage	V_{IL}	−3.0		0.8	V	
Input high voltage	V_{IH}	2.0		6.0	V	
Output low voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4			V	I_{OH} = −4 mA
Output short circuit current	I_{OS1}		−150		mA	V_{OUT} = GND
Output short circuit current	I_{OS2}		150		mA	V_{OUT} = V_{CC}

Note: ① $\overline{CS}$ valid prior to or coincident with address transition

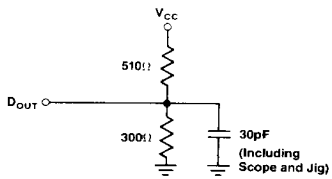


Figure 1. Loading Conditions Test Circuit

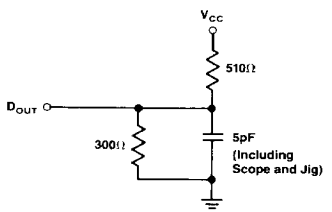


Figure 2. Input Pulse Test Circuit

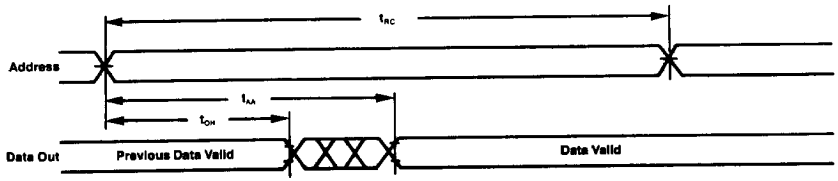
AC Characteristics
T_A=0°C to +70°C, V_{CC} = +5V ±10%

Parameter	Sym	μPD2167-3 Min	μPD2167-3 Typ	μPD2167-3 Max	μPD2167-2 Min	μPD2167-2 Typ	μPD2167-2 Max	Unit	Notes
Read Cycle									
Read cycle time	t_{RC}	55			70			ns	
Address access time	t_{AA}			55			70	ns	①
Chip select access time	t_{ACS}			55			70	ns	②
Output hold from address change	t_{OH}	5			5			ns	
Chip select to output in low-Z	t_{LZ}	10			10			ns	
Chip deselect to output in high-Z	t_{HZ}	0		40	0		40	ns	
Chip select to power-up time	t_{PU}	0			0			ns	
Chip deselect to power-down time	t_{PD}		30			30		ns	
Write Cycle									
Write cycle time	t_{WC}	55			70			ns	
Chip select to end of write	t_{CW}	45			55			ns	
Address valid to end of write	t_{AW}	45			55			ns	
Address setup time	t_{AS}	0			0			ns	
Write pulse	t_{WP}	35			40			ns	
Write recovery time	t_{WR}	10			15			ns	
Data valid to end of write	t_{DW}	25			30			ns	
Data hold time	t_{DH}	10			10			ns	
Write enabled to output in high-Z	t_{WZ}	0		30	0		35	ns	
Output active from end of write	t_{OW}	0			0			ns	

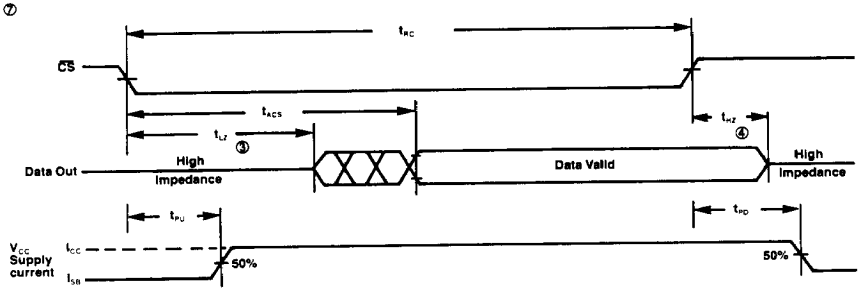
Notes: ① $\overline{CS}$ valid prior to or coincident with address transition
② Address valid prior to or coincident with $\overline{CS}$ transition low

Timing Waveforms

Read Cycle 1 ⑤ ⑥

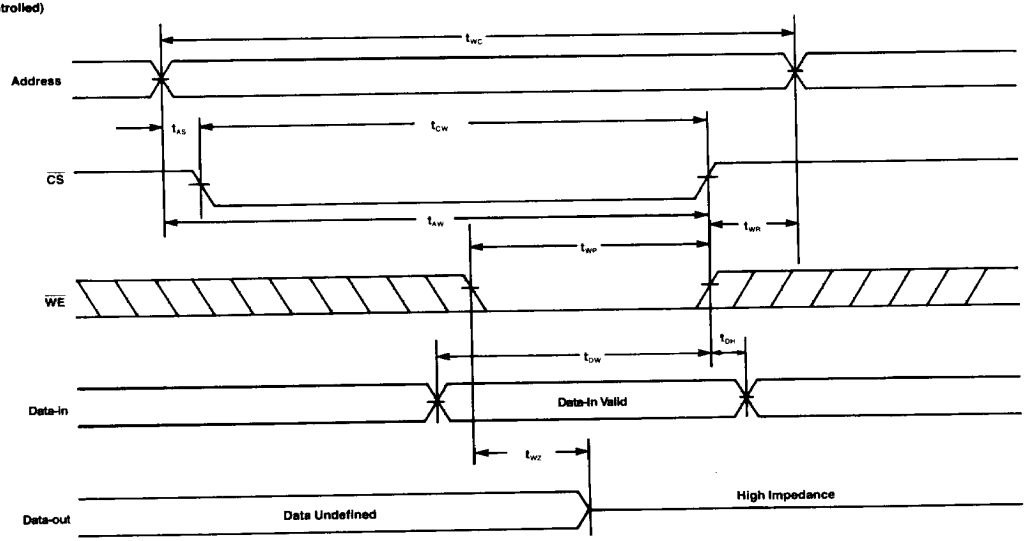


Read Cycle 2 ⑤ ⑦



Notes: ① All Read Cycle timings are referenced from the last valid address to the first address in transition.
② At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
③ Transition is measured +200mV from steady state voltage with specified loading in Figure 2.
④ Transition is measured at V_{OL} +200mV and V_{OH} −200mV with specified loading in Figure 2.
⑤ $\overline{WE}$ is high for Read Cycles.
⑥ Device is continuously selected, $\overline{CS} = V_{IL}$.
⑦ Addresses valid prior to or coincident with $\overline{CS}$ transition low.

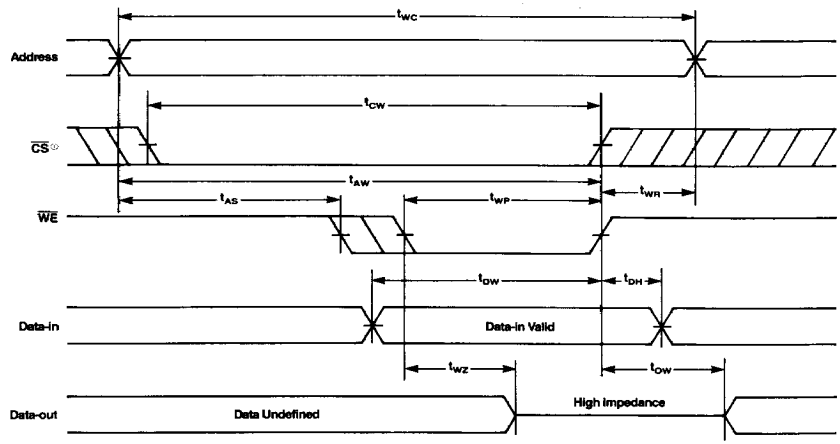
Write Cycle ① ② ③ ④
(CS Controlled)



Notes: ① If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
② All Write Cycle timings are referenced from the last valid address to the first transitioning address.
③ Transition is measured at V_{OL} +200 mV and V_{OH} −200 mV with specified loading in Figure 2.
④ Transition is measured ±200 mV from steady state voltage with specified loading in Figure 2.

Timing Waveforms (Cont.)

Write Cycle
(WE Controlled)



Package Outlines

For information, see Section 9.

Ceramic, μPD2167D