FULLY DECODED 128K BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The NEC μPD23128 is a high speed 128K bit mask programmable Read Only Memory organized as 16,384 words by 8 bits. The μPD23128 is fabricated with N-channel MOS technology.

The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The chip select input is programmable. An active high or low level chip select input can be defined and is fixed during the masking process.

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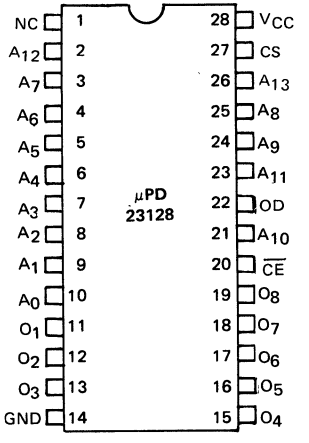
FEATURES

- 16,384 Words x 8 Bits Organization
- Directly TTL Compatible – All Inputs and Outputs
- Single +5V Power Supply
- High Speed – Access Time 250 ns Max.
- Three-State Output – OR-Tie Capability
- One Programmable Chip Select Input for Easy Memory Expansion
- On-Chip Address Fully Decoded
- All Inputs Protected Against Static Charge
- Pin Compatible with 2764
- Available in 28 Pin Ceramic or Plastic Dual-in-Line Package

PIN CONFIGURATION

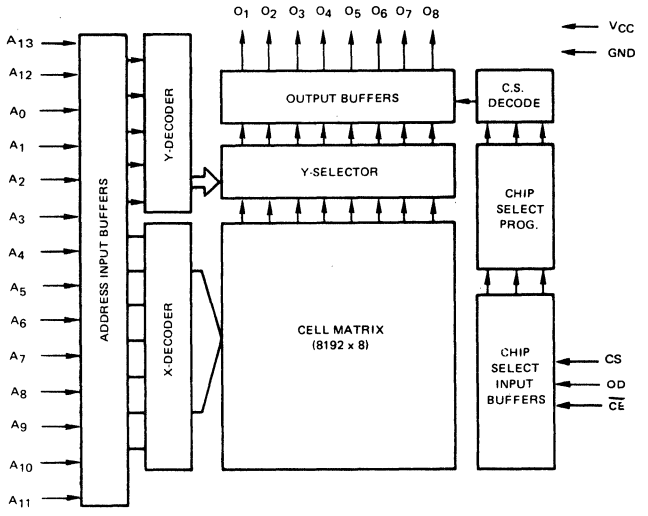


PIN NAMES

$A_0 - A_{13}$	Address Inputs
$O_1 - O_8$	Data Outputs
CS	Programmable Chip Select
OD	Output Disable
$\overline{CE}$	Chip Enable

Rev/1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Supply Voltage On Any Pin . . . . . −0.5 to +7.0 Volts (1)

Note: (1) With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C, V_{CC} = +5V ± 10%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP (1)	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}			+10	μA	$V_{IN} = V_{CC}$
				−10	μA	V_{IN} = 0V
Output Leakage Current	I_{LOH}			+10	μA	Chip Deselected, $V_O = V_{CC}$
Output Leakage Current	I_{LOL}			−10	μA	Chip Deselected, V_O = 0V
Power Supply Current	I_{CC}			100	mA	
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC} + 1.0V	V	
Output "Low" Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output "High" Voltage	V_{OH}	2.2			V	I_{OH} = −400 μA

Note: (1) Typical Values for T_a = 25°C and nominal supply voltages.

CAPACITANCE

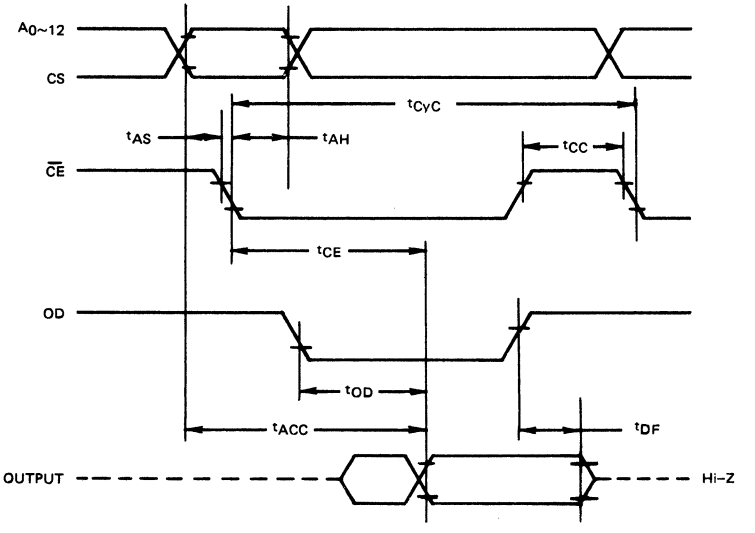
T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}			15	pF	All Pins Except Pin Under Test Tied to AC Ground

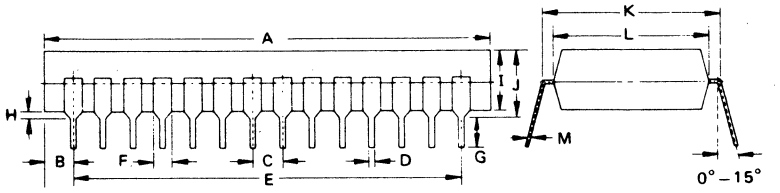
AC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Cycle Time	t_{CYC}	350			ns	
Address Setup Time Referenced to $\overline{CE}$	t_{AS}	0			ns	
Address Hold Time Referenced to $\overline{CE}$	t_{AH}	50			ns	
$\overline{CE}$ Pulse Width	t_{CE}			250	ns	
OD Pulse Width	t_{OD}			120	ns	
Access Time	t_{ACC}			250	ns	t_{AS} = 0 ns
$\overline{CE}$ Precharge Time	t_{CC}	100			ns	
Output Turn-Off Delay	t_{DF}	0		70	ns	

TIMING WAVEFORMS



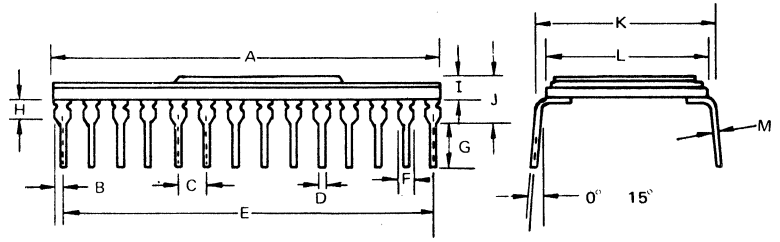
PACKAGE OUTLINE
μPD23128C



Plastic

ITEM	MILLIMETERS	INCHES
A	33 MAX.	1.3 MAX.
B	2.53 MAX.	0.1 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94 ± 0.1	1.1 ± 0.004
F	1.5 MIN.	0.059 MIN.
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24 TYP.	0.6 TYP.
L	13.2 TYP.	0.52 TYP.
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

μPD23128D



Ceramic

ITEM	MILLIMETERS	INCHES
A	30.78 MAX.	1.21 MAX.
B	1.53 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.10 ± 0.004
D	0.46 ± 0.8	0.018 ± 0.03
E	27.94 ± 0.1	1.10 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.02 MIN.	0.04 MIN.
I	3.23 MAX.	0.13 MAX.
J	4.25 MAX.	0.17 MAX.
K	15.24 TYP.	0.60 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.010 ± 0.002