NEC
NEC Electronics Inc.

μPD23C1024E
65,536 x 16-Bit
Mask-Programmable CMOS ROM

Description

The μPD23C1024E is a 65,536-word by 16-bit mask-programmable ROM fabricated with CMOS silicon-gate technology and designed to operate from a single +5-volt power supply. The device has three-state outputs and fully TTL-compatible inputs and outputs, and is packaged in a 600-mil, 40-pin plastic DIP.

Features

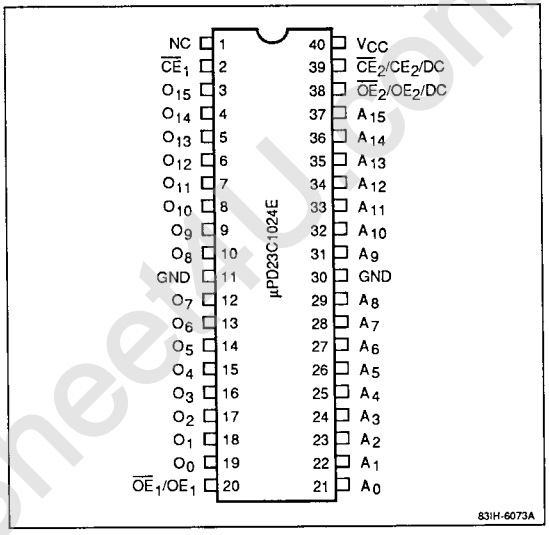
- 65,536-word by 16-bit organization
- Fast access time: 200 ns maximum
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- CMOS process technology
- Fully static operation
- Low power dissipation

Ordering Information

Part Number	Access Time (max)	Package
μPD23C1024EC	200 ns	40-pin plastic DIP

Pin Configuration

40-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0 - A_{15}	Address inputs
O_0 - O_{15}	Data outputs
$\overline{CE}_1$	Chip enable 1
$\overline{CE}_2/CE_2/DC$	Chip enable 2 (Note 1)
$\overline{OE}_1/OE_1$	Output enable 1
$\overline{OE}_2/OE_2/DC$	Output enable 2 (Note 1)
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Notes:

(1) This pin is user-definable as active low, active high, or "don't care."

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Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} +0.3 V
Output voltage, V_O	−0.3 V to V_{CC} +0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

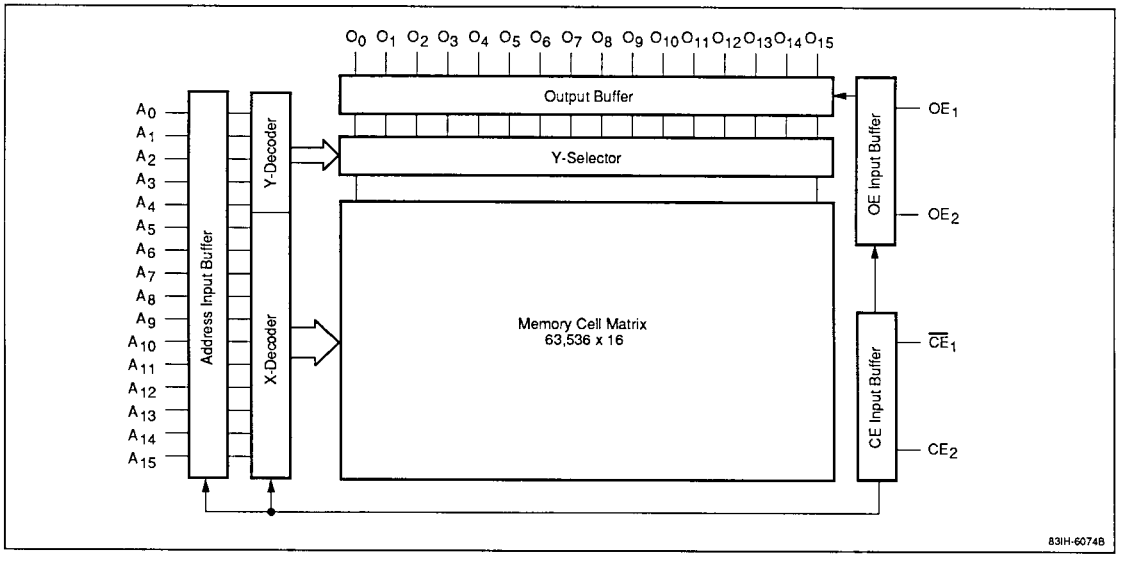
T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			15	pF
Output capacitance	C_O			15	pF

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	−10		70	°C

Block Diagram



Truth Table

$\overline{CE}_1$	CE_2	OE_1	OE_2	Function	Outputs	I_{CC}
V_{IH}	X	X	X	Not Selected	High-Z	Standby
X	Inactive	X	X	Not Selected	High-Z	Standby
V_{IL}	Active	Inactive	X	Selected	High-Z	Active
V_{IL}	Active	X	Inactive	Selected	High-Z	Active
V_{IL}	Active	Active	Active	Read	Data Output	Active

Notes:

(1) X = don't care.

DC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −400 μA
Output voltage, low	V_{OL}		0.4	V	I_{OL} = +2.5 mA
Input leakage current	I_{LI}	−10	10	μA	V_I = 0 V to V_{CC}
Output leakage current	I_{LO}	−10	10	μA	V_O = 0 V to V_{CC} (chip deselected)
Power supply current	I_{CC1}		40	mA	$\overline{CE}_1$ = V_{IL}; CE_2 = active (chip selected)
	I_{CC2}		1.5	mA	$\overline{CE}_1$ = V_{IH} or CE_2 = inactive (chip deselected)
	I_{CC3}		100	μA	$\overline{CE}_1 \geq V_{CC} - 0.2$ V; $CE_2 \leq 0.2$ V (if CE_2 is programmed active high) or $CE_2 \geq V_{CC} - 0.2$ V (if CE_2 is programmed active low)

AC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Address access time	t_{ACC}		200	ns	
Chip enable access time	t_{CE}		200	ns	
Output enable access time	t_{OE}		100	ns	
Output hold time	t_{OH}	0		ns	
Output disable time	t_{DF}	0	70	ns	

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 V and 2.0 V; output load = 1 TTL + 100 pF.

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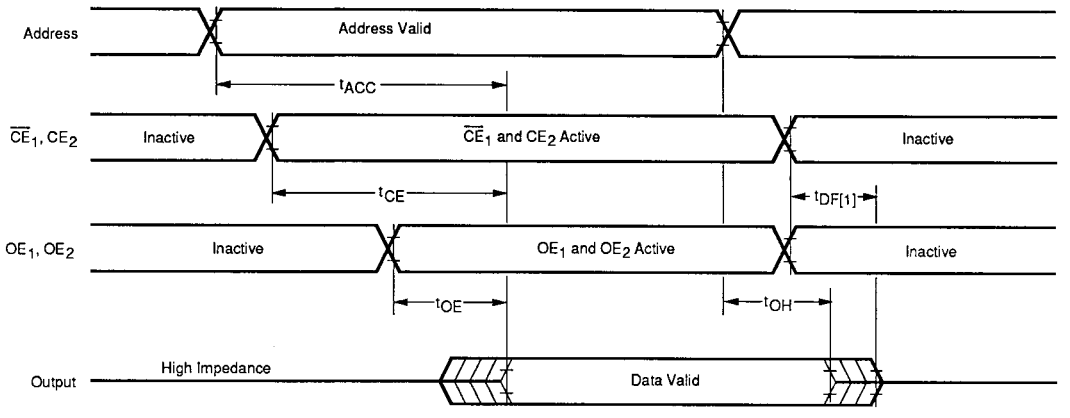
Timing Waveform



Notes:

[1] t_{DF} is specified from $\overline{CE}_1$, CE_2, OE_1, OE_2, whichever goes inactive first.

[2] t_{CE} is specified from $\overline{CE}_1$ or CE_2, whichever goes active last.

[3] t_{OE} is specified from OE_1 or OE_2, whichever goes active last.

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