NEC

MOS INTEGRATED CIRCUIT

μPD23C128040BL, 23C128080BL

128M-BIT MASK-PROGRAMMABLE ROM
16M-WORD BY 8-BIT (BYTE MODE) / 8M-WORD BY 16-BIT (WORD MODE)
PAGE ACCESS MODE

Description

The μPD23C128040BL and μPD23C128080BL are a 134,217,728 bits mask-programmable ROM. The word organization is selectable (BYTE mode : 16,777,216 words by 8 bits, WORD mode : 8,388,608 words by 16 bits).
With 44-pin PLASTIC SOP package products, only WORD mode can be used; it is not possible to switch to BYTE mode.

The active levels of OE (Output Enable Input) can be selected with mask-option.

The μPD23C128040BL and μPD23C128080BL are packed in 48-pin PLASTIC TSOP(I) and 44-pin PLASTIC SOP.

Features

- Word organization

  16,777,216 words by 8 bits (BYTE mode) **Note**

  8,388,608 words by 16 bits (WORD mode) **Note**

  Note With 44-pin PLASTIC SOP package products, only WORD mode can be used.
  It is not possible to switch to BYTE mode.

- Page access mode

  BYTE mode : 8 byte random page access (μPD23C128040BL)
  16 byte random page access (μPD23C128080BL)

  WORD mode : 4 word random page access (μPD23C128040BL)
  8 word random page access (μPD23C128080BL)

- Operating supply voltage : V_{CC} = 2.7 to 3.6 V

Operating supply voltage V_{CC}	Access time / Page access time ns (MAX.)	Power supply current (Active mode) mA (MAX.)		Standby current (CMOS level input) μA (MAX.)
		μPD23C128040BL	μPD23C128080BL	
3.0 V ± 0.3 V	120 / 25	50	70	30
3.3 V ± 0.3 V	100 / 25	55	75	

Document No. M16048EJ2V0DS00 (2nd edition)
Date Published February 2003 NS CP (K)
Printed in Japan

The mark ★ shows major revised points.

Ordering Information

Part Number	Package
μPD23C128040BLGY-xxx-MJH	48-pin PLASTIC TSOP(I) (12x18) (Normal bent)
μPD23C128040BLGY-xxx-MKH	48-pin PLASTIC TSOP(I) (12x18) (Reverse bent)
μPD23C128040BLGX-xxx	44-pin PLASTIC SOP (15.24 mm (600))
μPD23C128080BLGY-xxx-MJH	48-pin PLASTIC TSOP(I) (12x18) (Normal bent)
μPD23C128080BLGY-xxx-MKH	48-pin PLASTIC TSOP(I) (12x18) (Reverse bent)
μPD23C128080BLGX-xxx	44-pin PLASTIC SOP (15.24 mm (600))

(xxx : ROM code suffix No.)

Pin Configurations

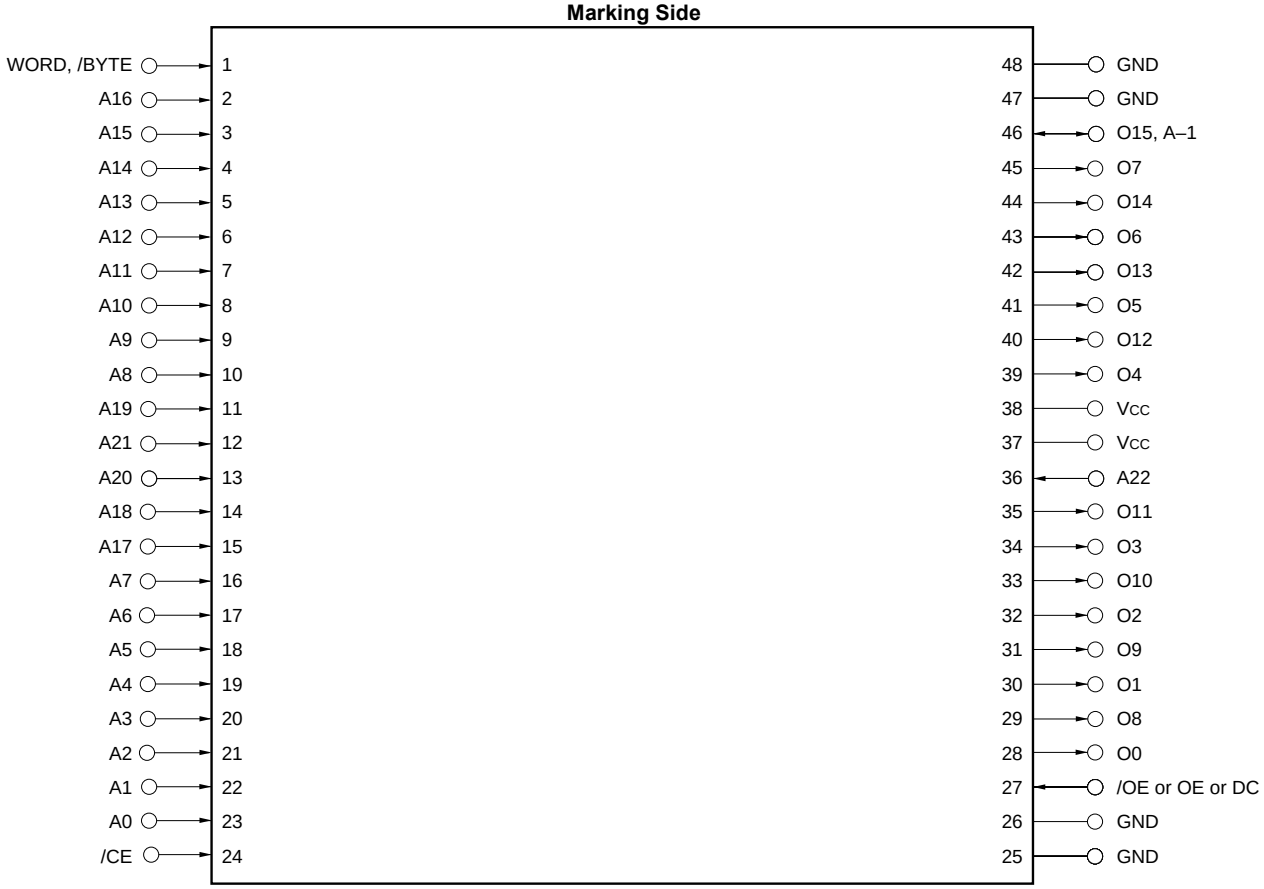
/xxx indicates active low signal.

48-pin PLASTIC TSOP(I) (12 x 18) (Normal bent)

[μPD23C128040BLGY-xxx-MJH]

[μPD23C128080BLGY-xxx-MJH]

Marking Side



A0 to A22	:	Address inputs
O0 to O7, O8 to O14	:	Data outputs
O15, A–1	:	Data output 15 (WORD mode), LSB Address input (BYTE mode)
WORD, /BYTE	:	Mode select
/CE	:	Chip Enable
/OE or OE	:	Output Enable
V_{CC}	:	Supply voltage
GND	:	Ground
DC	:	Don't Care

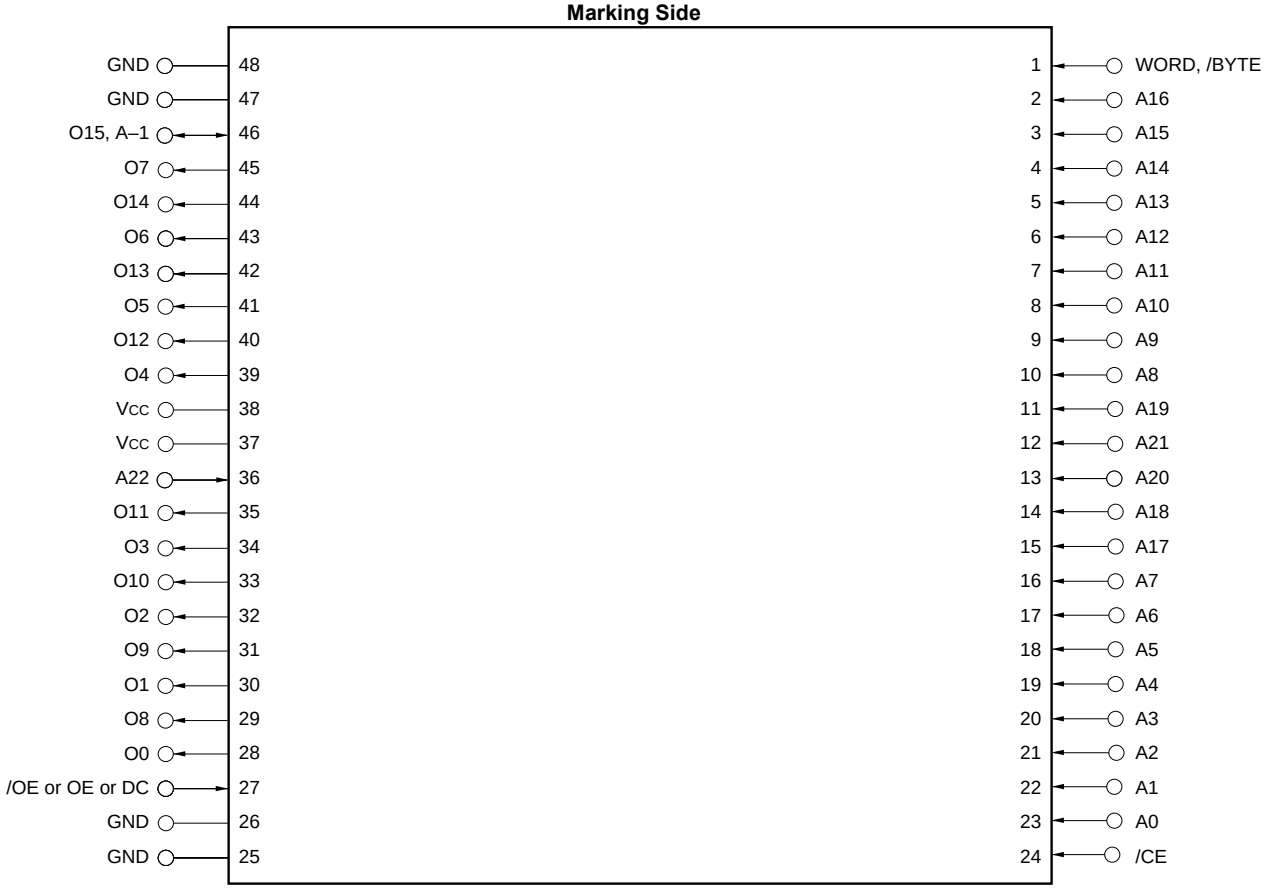
Remark Refer to **Package Drawings** for the 1-pin index mark.

48-pin PLASTIC TSOP(I) (12 x 18) (Reverse bent)

[μPD23C128040BLGY-xxx-MKH]

[μPD23C128080BLGY-xxx-MKH]

Marking Side



A0 to A22	:	Address inputs
O0 to O7, O8 to O14	:	Data outputs
O15, A–1	:	Data output 15 (WORD mode), LSB Address input (BYTE mode)
WORD, /BYTE	:	Mode select
/CE	:	Chip Enable
/OE or OE	:	Output Enable
VCC	:	Supply voltage
GND	:	Ground
DC	:	Don't Care

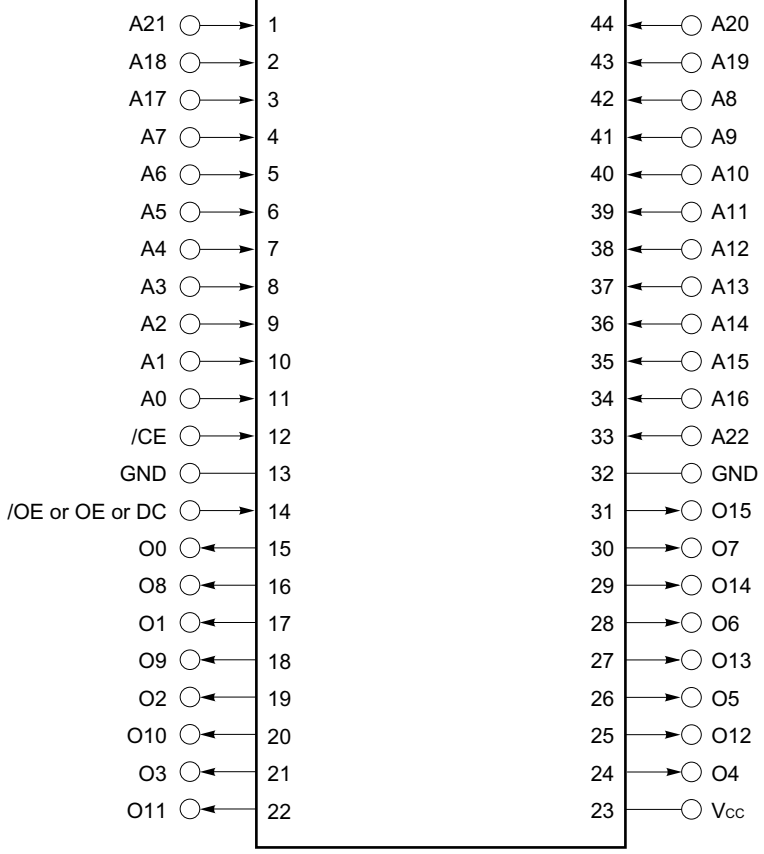
Remark Refer to **Package Drawings** for the 1-pin index mark.

44-pin PLASTIC SOP (15.24 mm (600))

[μPD23C128040BLGX-xxx]

[μPD23C128080BLGX-xxx]

Marking Side



A0 to A22	:	Address inputs
O0 to O15	:	Data outputs
/CE	:	Chip Enable
/OE or OE	:	Output Enable
V_{CC}	:	Supply voltage
GND	:	Ground
DC	:	Don't Care

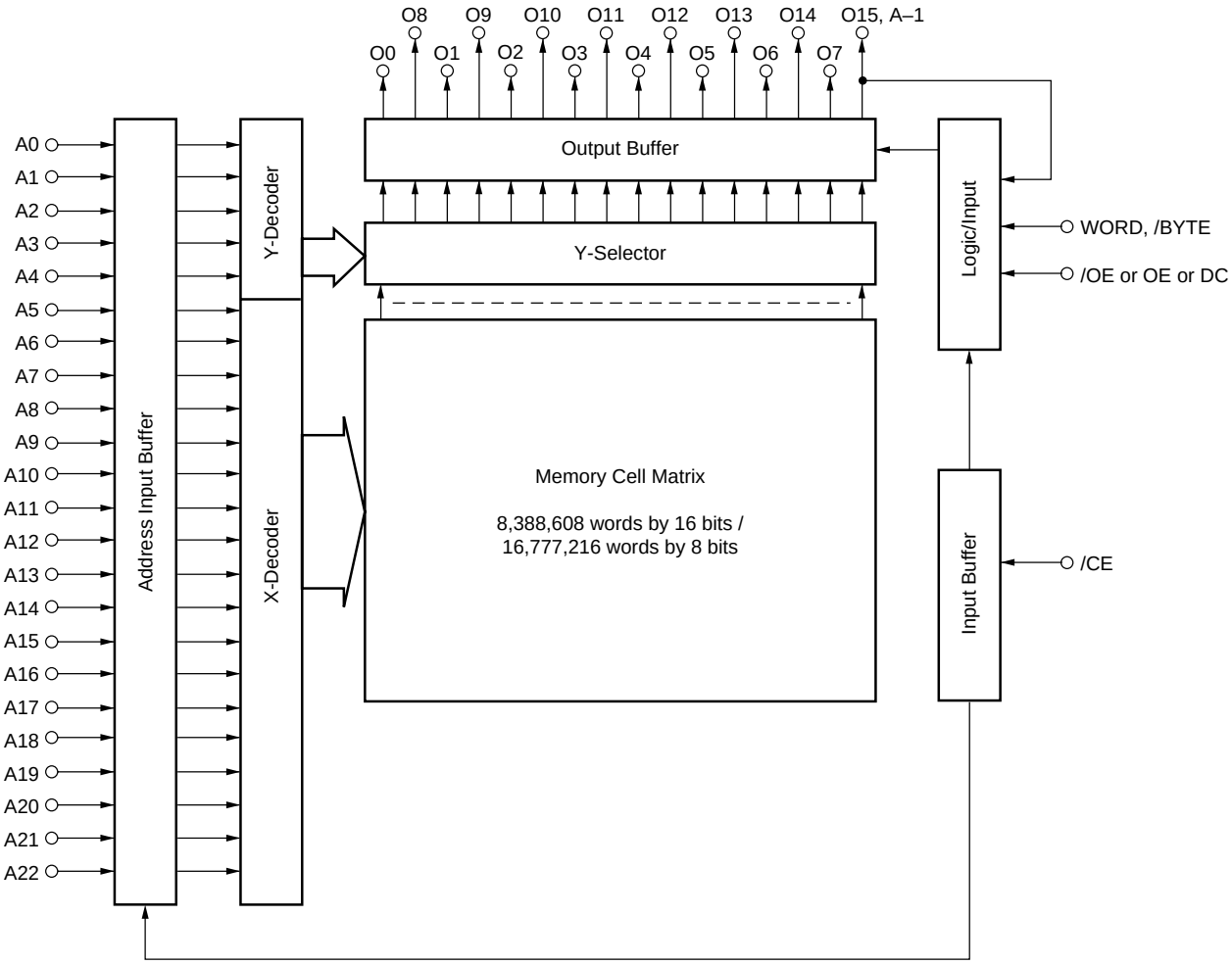
Remarks 1. Refer to **Package Drawings** for the 1-pin index mark.

2. With 44-pin PLASTIC SOP package products, only WORD mode (8,388,608 words x 16 bits) can be used. There is no mode select (WORD, /BYTE) pin.

Input / Output Pin Functions

Pin name	Input / Output	Function
WORD, /BYTE	Input	The pin for switching WORD mode and BYTE mode. **High level** : WORD mode (8M-word by 16-bit) **Low level** : BYTE mode (16M-word by 8-bit)
A0 to A22 (Address inputs)	Input	Address input pins. A0 to A22 are used differently in the WORD mode and the BYTE mode. **WORD mode (8M-word by 16-bit)** A0 to A22 are used as 23 bits address signals. **BYTE mode (16M-word by 8-bit)** A0 to A22 are used as the upper 23 bits of total 24 bits of address signal. (The least significant bit (A–1) is combined to O15.)
O0 to O7, O8 to O14 (Data outputs)	Output	Data output pins. O0 to O7, O8 to O14 are used differently in the WORD mode and the BYTE mode. **WORD mode (8M-word by 16-bit)** The lower 15 bits of 16 bits data outputs to O0 to O14. (The most significant bit (O15) combined to A–1.) **BYTE mode (16M-word by 8-bit)** 8 bits data outputs to O0 to O7 and also O8 to O14 are high impedance.
O15, A–1 (Data output 15, LSB Address input)	Output, Input	O15, A–1 are used differently in the WORD mode and the BYTE mode. **WORD mode (8M-word by 16-bit)** The most significant output data bus (O15). **BYTE mode (16M-word by 8-bit)** The least significant address bus (A–1).
/CE (Chip Enable)	Input	Chip activating signal. When the OE is active, output states are following. **High level** : High-Z **Low level** : Data out
/OE or OE or DC (Output Enable, Don't Care)	Input	Output enable signal. The active level of OE is mask option. The active level of OE can be selected from high active, low active and Don't care at order.
V_{CC}	–	Supply voltage
GND	–	Ground

Block Diagram



Mask Option

The active levels of output enable pin (/OE or OE or DC) are mask programmable and optional, and can be selected from among " 0 " " 1 " " x " shown in the table below.

Option	/OE or OE or DC	OE active level
0	/OE	L
1	OE	H
x	DC	Don't care

Operation modes for each option are shown in the tables below.

Operation mode (Option : 0)

/CE	/OE	Mode	Output state
L	L	Active	Data out
	H		High-Z
H	H or L	Standby	High-Z

Operation mode (Option : 1)

/CE	OE	Mode	Output state
L	L	Active	High-Z
	H		Data out
H	H or L	Standby	High-Z

Operation mode (Option : x)

/CE	DC	Mode	Output state
L	H or L	Active	Data out
H	H or L	Standby	High-Z

Remark L : Low level input
H : High level input

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.3 to +4.6	V
Input voltage	V_I		–0.3 to V_{CC}+0.3	V
Output voltage	V_O		–0.3 to V_{CC}+0.3	V
Operating ambient temperature	T_A		–10 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (T_A = 25 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			10	pF
Output capacitance	C_O				12	pF

DC Characteristics (T_A = –10 to +70 °C, V_{CC} = 2.7 to 3.6 V)

Parameter	Symbol	Test conditions			MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}				2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}	V_{CC} = 3.0 V ± 0.3 V			–0.3		+0.5	V
		V_{CC} = 3.3 V ± 0.3 V			–0.3		+0.8	
High level output voltage	V_{OH}	I_{OH} = –100 μA			2.4			V
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA					0.4	V
Input leakage current	I_{LI}	V_I = 0 V to V_{CC}			–10		+10	μA
Output leakage current	I_{LO}	V_O = 0 V to V_{CC}, Chip deselected			–10		+10	μA
Power supply current	I_{CC1}	/CE = VIL (Active mode) , I_O = 0 mA	μPD23C128040BL	V_{CC} = 3.0 V ± 0.3 V			50	mA
				V_{CC} = 3.3 V ± 0.3 V			55	
			μPD23C128080BL	V_{CC} = 3.0 V ± 0.3 V			70	
				V_{CC} = 3.3 V ± 0.3 V			75	
Standby current	I_{CC3}	/CE = V_{CC} – 0.2 V (Standby mode)					30	μA

AC Characteristics (T_A = –10 to +70 °C, V_{CC} = 2.7 to 3.6 V)

	Parameter	Symbol	Test condition	V_{CC} = 3.0 V ± 0.3 V			V_{CC} = 3.3 V ± 0.3 V			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
	Address access time	t_{ACC}				120			100	ns
	Page access time	t_{PAC}				25			25	ns
★	Address skew time	t_{SKEW}	**Note**			10			10	ns
	Chip enable access time	t_{CE}				120			100	ns
	Output enable access time	t_{OE}				25			25	ns
	Output hold time	t_{OH}		0			0			ns
	Output disable time	t_{DF}		0		20	0		20	ns
	WORD, /BYTE access time	t_{WB}				120			100	ns

★ **Note** t_{SKEW} indicates the following three types of time depending on the condition.

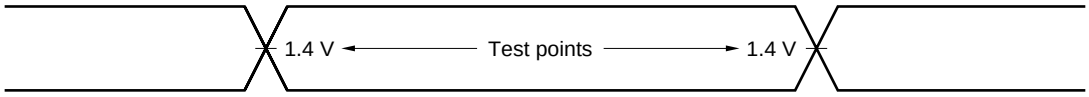
1) When switching /CE from high level to low level, t_{SKEW} is the time from the /CE low level input point until the next address is determined.
2) When switching /CE from low level to high level, t_{SKEW} is the time from the address change start point to the /CE high level input point.
3) When /CE is fixed to low level, t_{SKEW} is the time from the address change start point until the next address is determined.

Since specs are defined for t_{SKEW} only when /CE is active, t_{SKEW} is not subject to limitations when /CE is switched from high level to low level following address determination, or when the address is changed after /CE is switched from low level to high level.

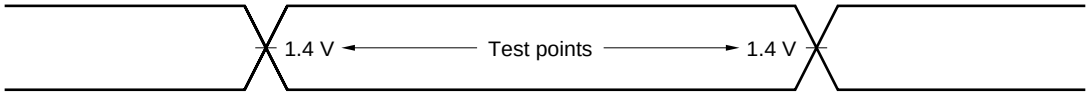
Remark t_{DF} is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.

AC Test Conditions

Input waveform (Rise / Fall time ≤ 5 ns)



Output waveform



Output load

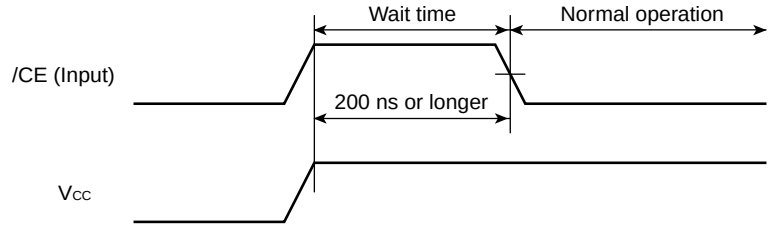
1TTL + 100 pF

★ **Cautions on power application**

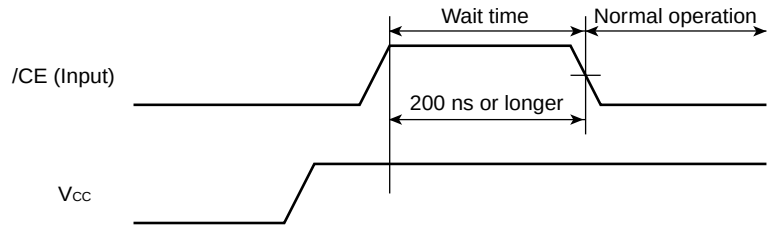
To ensure normal operation, always apply power using /CE following the procedure shown below.

1) Input a high level to /CE during and after power application.
2) Hold the high level input to /CE for 200 ns or longer (wait time).
3) Start normal operation after the wait time has elapsed.

Power Application Timing Chart 1 (When /CE is made high at power application)

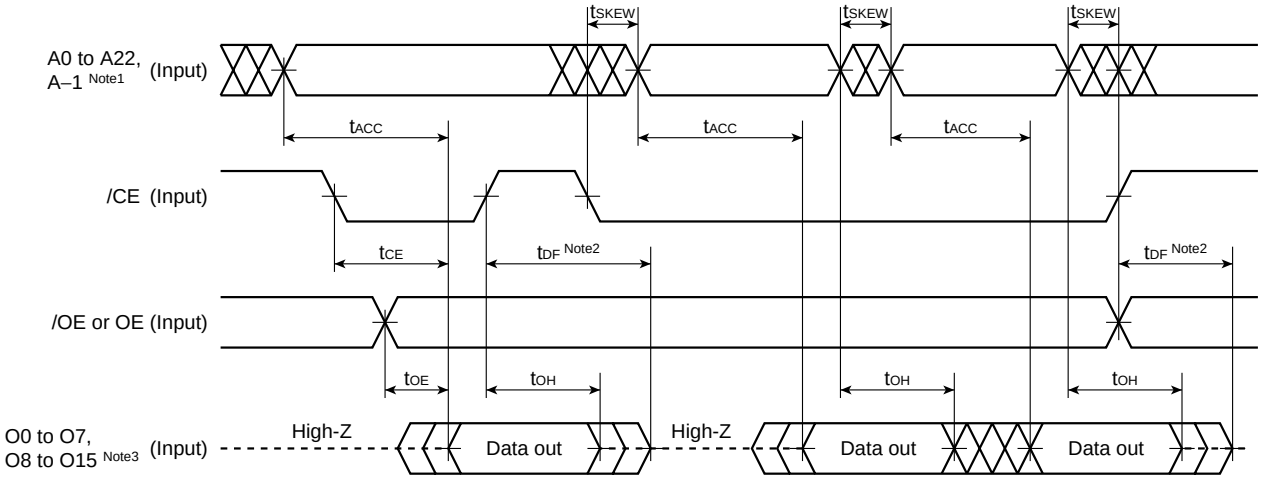


Power Application Timing Chart 2 (When /CE is made high after power application)



Caution Other signals can be either high or low during the wait time.

★ **Read Cycle Timing Chart 1**

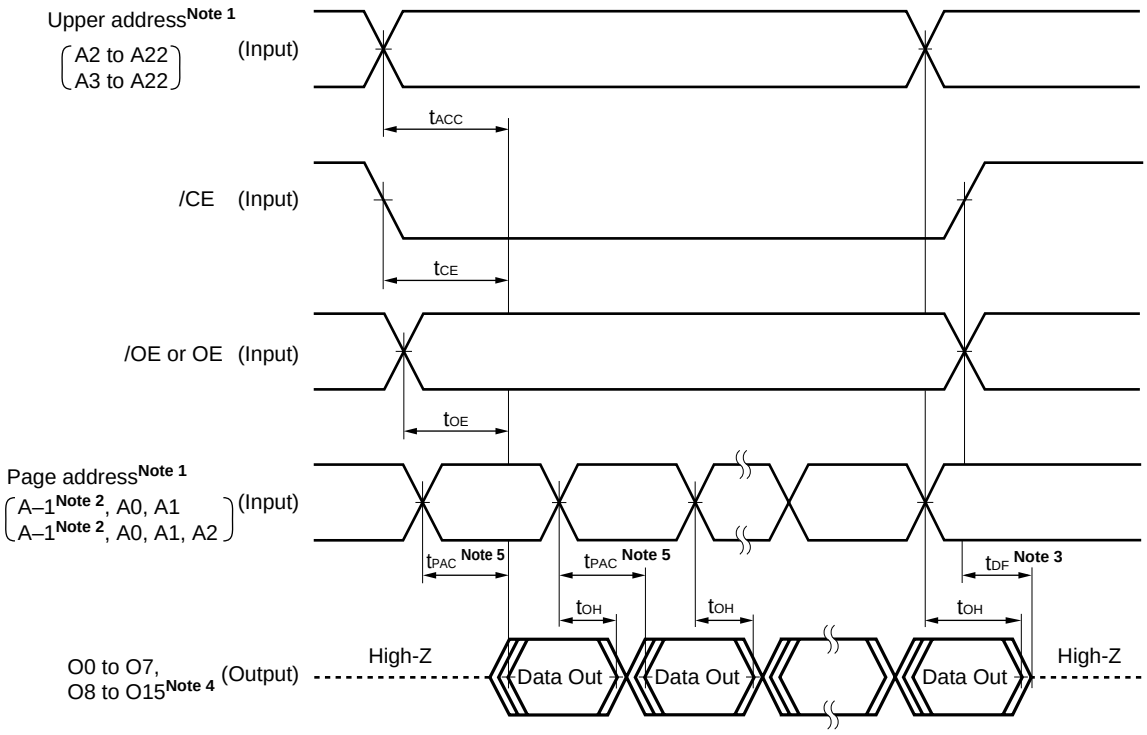


Notes 1. During WORD mode, A–1 is O15.

2. t_{DF} is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.

3. During BYTE mode, O8 to O14 are high impedance and O15 is A–1.

Read Cycle Timing Chart 2 (Page Access Mode)



Notes 1. The address differs depending on the product as follows.

Part Number	Upper address	Page address
μPD23C128040BL	A2 to A22	A–1, A0, A1
μPD23C128080BL	A3 to A22	A–1, A0, A1, A2

2. During WORD mode, A–1 is O15.

3. t_{DF} is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.

4. During BYTE mode, O8 to O14 are high impedance and O15 is A–1.

5. The definition of page access time is as follows.

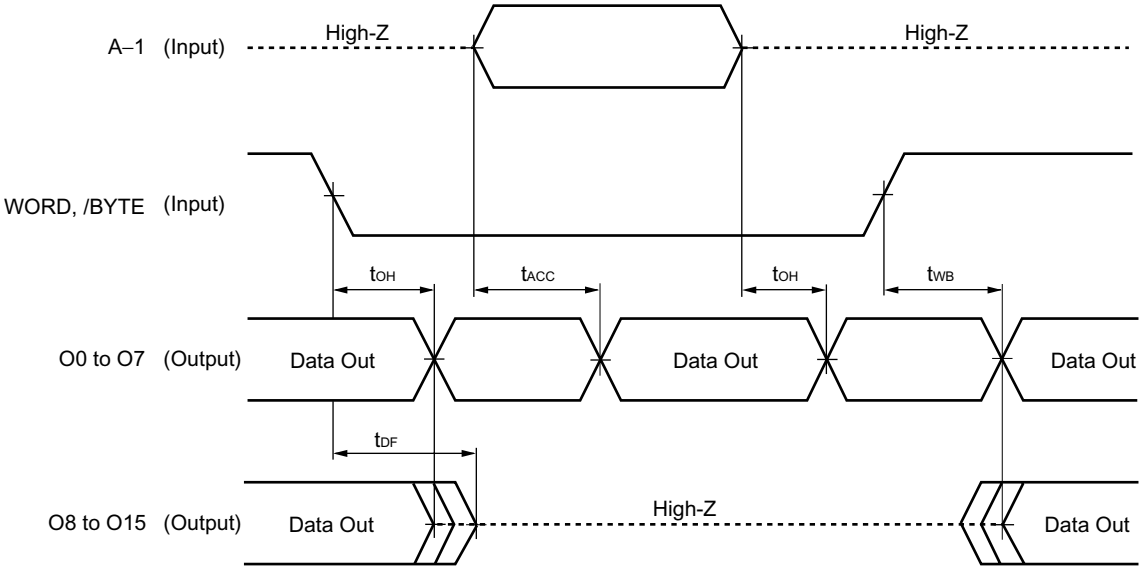
[μPD23C128040BL]

Page access time	Upper address (A2 to A22) inputs condition	/CE input condition	/OE or OE input condition
t_{PAC}	Before $t_{ACC} - t_{PAC}$	Before $t_{CE} - t_{PAC}$	Before stabilizing of page address (A–1, A0, A1)

[μPD23C128080BL]

Page access time	Upper address (A3 to A22) inputs condition	/CE input condition	/OE or OE input condition
t_{PAC}	Before $t_{ACC} - t_{PAC}$	Before $t_{CE} - t_{PAC}$	Before stabilizing of page address (A–1, A0, A1, A2)

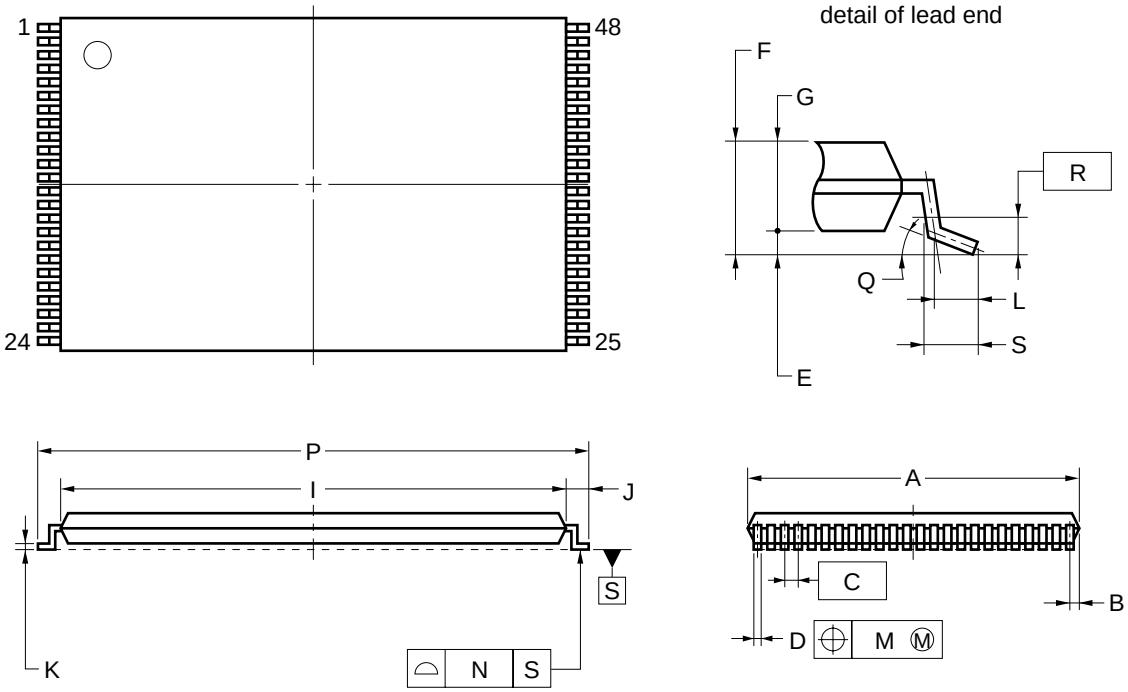
WORD, /BYTE Switch Timing Chart



Remark Chip Enable (/CE) and Output Enable (/OE or OE) : Active.

Package Drawings

48-PIN PLASTIC TSOP(I) (12x18)



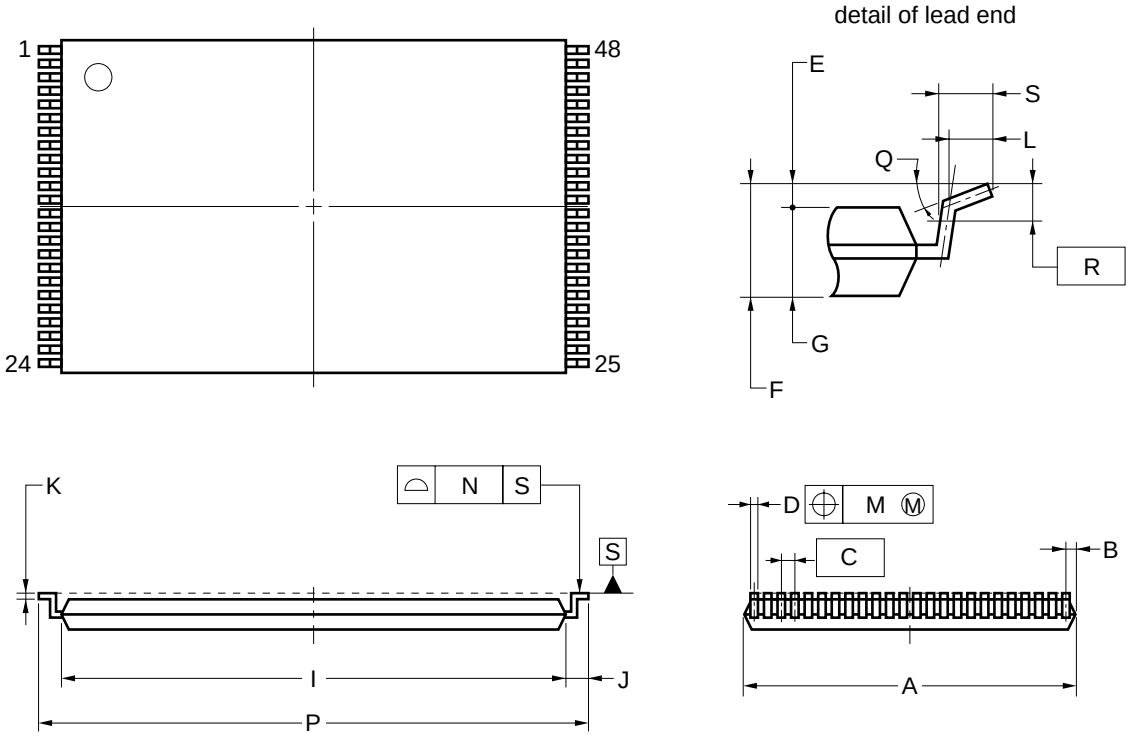
NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	16.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	18.0±0.2
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S48GY-50-MJH1-1

48-PIN PLASTIC TSOP(I) (12x18)



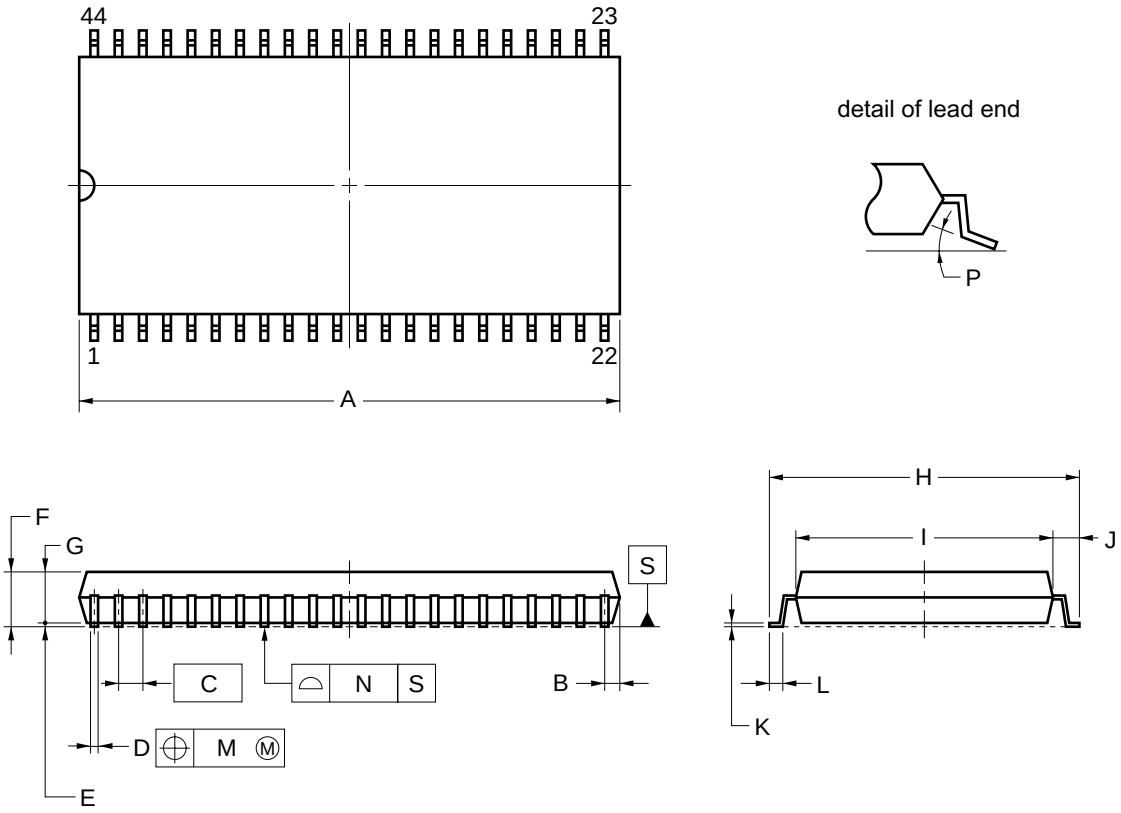
NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	16.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	18.0±0.2
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S48GY-50-MKH1-1

44-PIN PLASTIC SOP (15.24 mm (600))



NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	$27.83^{+0.4}_{-0.05}$
B	0.78 MAX.
C	1.27 (T.P.)
D	$0.42^{+0.08}_{-0.07}$
E	0.15±0.1
F	3.0 MAX.
G	2.7±0.05
H	16.04±0.3
I	13.24±0.1
J	1.4±0.2
K	$0.22^{+0.08}_{-0.07}$
L	0.8±0.2
M	0.12
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P44GX-50-600A-4

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD23C128040BL and μPD23C128080BL.

Types of Surface Mount Device

μPD23C128040BLGY-MJH : 48-pin PLASTIC TSOP(I) (12 x 18) (Normal bent)
μPD23C128040BLGY-MKH : 48-pin PLASTIC TSOP(I) (12 x 18) (Reverse bent)
μPD23C128040BLGX : 44-pin PLASTIC SOP (15.24 mm (600))
μPD23C128080BLGY-MJH : 48-pin PLASTIC TSOP(I) (12 x 18) (Normal bent)
μPD23C128080BLGY-MKH : 48-pin PLASTIC TSOP(I) (12 x 18) (Reverse bent)
μPD23C128080BLGX : 44-pin PLASTIC SOP (15.24 mm (600))

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
2nd edition/ Feb. 2003	Throughout	Throughout	Modification		Preliminary Data Sheet → Data Sheet
	p.10	p.10	Addition	AC Characteristics	Address skew time (t_{SKEW}) Note
	p.11	–	Addition		Cautions on power application
	p.12	p.11	Modification		Read Cycle Timing Chart 1

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF THE APPLIED WAVEFORM OF INPUT PINS AND THE UNUSED INPUT PINS FOR CMOS

Note:

Input levels of CMOS devices must be fixed. CMOS devices behave differently than Bipolar or NMOS devices. If the input of a CMOS device stays in an area that is between V_{IL} (MAX.) and V_{IH} (MIN.) due to the effects of noise or some other irregularity, malfunction may result. Therefore, not only the input waveform is fixed, but also the waveform changes, it is important to use the CMOS device under AC test conditions. For unused input pins in particular, CMOS devices should not be operated in a state where nothing is connected, so input levels of CMOS devices must be fixed to high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

These commodities, technology or software, must be exported in accordance with the export administration regulations of the exporting country. Diversion contrary to the law of that country is prohibited.

- **The information in this document is current as of February, 2003. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets or data books, etc., for the most up-to-date specifications of NEC Electronics products. Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Electronics. NEC Electronics assumes no responsibility for any errors that may appear in this document.
- NEC Electronics does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC Electronics products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Electronics or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of a customer's equipment shall be done under the full responsibility of the customer. NEC Electronics assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC Electronics endeavors to enhance the quality, reliability and safety of NEC Electronics products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC Electronics products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.
- NEC Electronics products are classified into the following three quality grades: "Standard", "Special" and "Specific".
  The "Specific" quality grade applies only to NEC Electronics products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of an NEC Electronics product depend on its quality grade, as indicated below. Customers must check the quality grade of each NEC Electronics product before using it in a particular application.
  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.
  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).
  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC Electronics products is "Standard" unless otherwise expressly specified in NEC Electronics data sheets or data books, etc. If customers wish to use NEC Electronics products in applications not intended by NEC Electronics, they must contact an NEC Electronics sales representative in advance to determine NEC Electronics' willingness to support a given application.

(Note)
(1) "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.
(2) "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).