

### 64M-BIT MASK-PROGRAMMABLE ROM

### 8M-WORD BY 8-BIT (BYTE MODE) / 4M-WORD BY 16-BIT (WORD MODE)

#### Description

The  $\mu$ PD23C64000JL is a 67,108,864 bits mask-programmable ROM. The word organization is selectable (BYTE mode : 8,388,608 words by 8 bits, WORD mode : 4,194,304 words by 16 bits).

The active levels of OE (Output Enable Input) can be selected with mask-option.

The  $\mu$ PD23C64000JL is packed in 48-pin PLASTIC TSOP (I) and 44-pin PLASTIC SOP.

#### Features

- Word organization  
8,388,608 words by 8 bits (BYTE mode)  
4,194,304 words by 16 bits (WORD mode)
- Operating supply voltage :  $V_{CC} = 2.7$  to  $3.6$  V

Operating supply voltage $V_{CC}$	Package	Access time ns (MAX.)	Power supply current (Active mode) mA (MAX.)	Standby current (CMOS level input) $\mu$ A (MAX.)
3.0 V $\pm$ 0.3 V	TSOP (I)	100	40	30
	SOP	120	35	
3.3 V $\pm$ 0.3 V	TSOP (I)	90	55	
	SOP	100	50	

**Remark** The access time and power supply current vary depending on the package type.

#### Ordering Information

Part number	Package
$\mu$ PD23C64000JLGY-xxx-MJH	48-pin PLASTIC TSOP (I) (12 $\times$ 18) (Normal bent)
$\mu$ PD23C64000JLGY-xxx-MKH	48-pin PLASTIC TSOP (I) (12 $\times$ 18) (Reverse bent)
$\mu$ PD23C64000JLGX-xxx	44-pin PLASTIC SOP (15.24 mm (600))

(xxx : ROM code suffix No.)

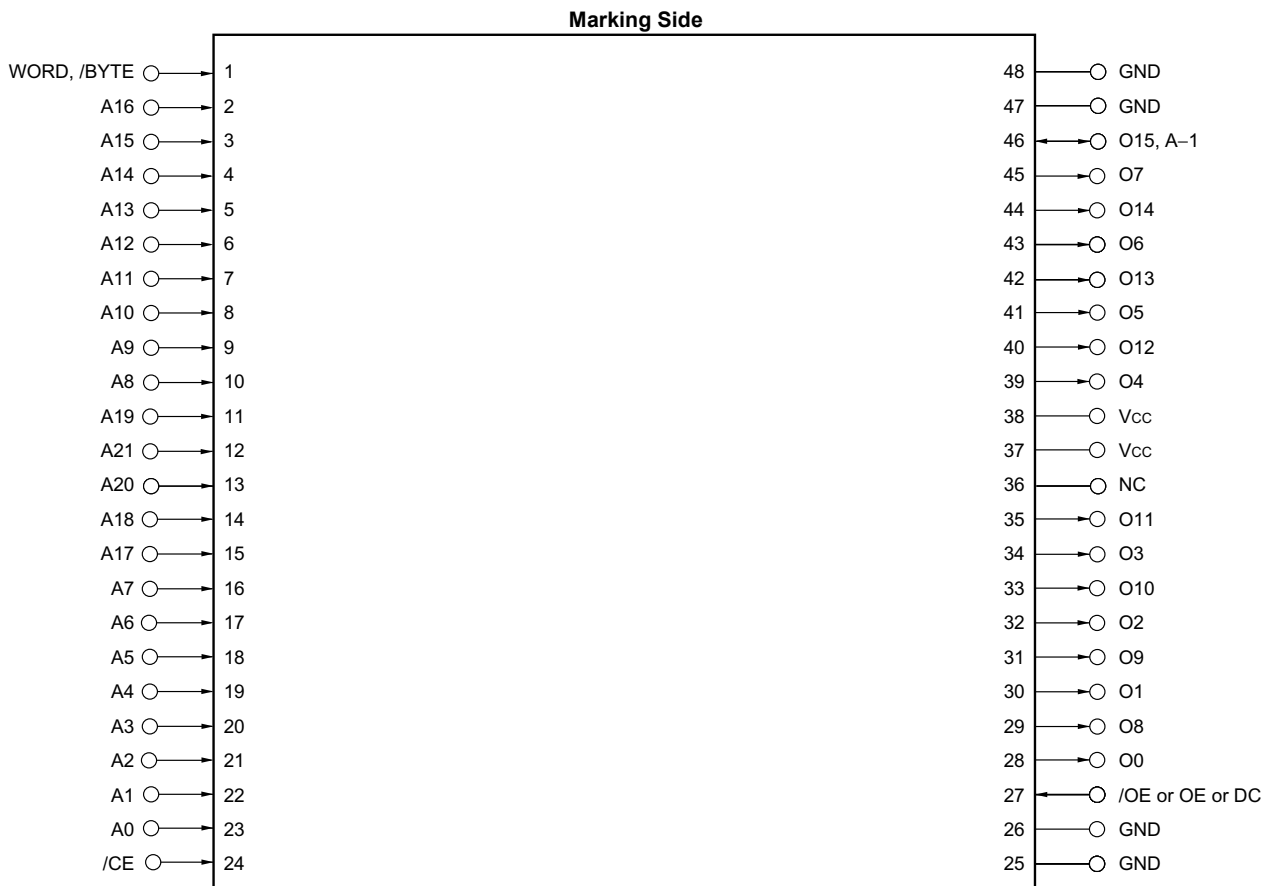
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**Pin Configurations**

/xxx indicates active low signal.

**48-pin PLASTIC TSOP (I) (12 × 18) (Normal bent)**

[ μPD23C64000JLGY-xxx-MJH ]

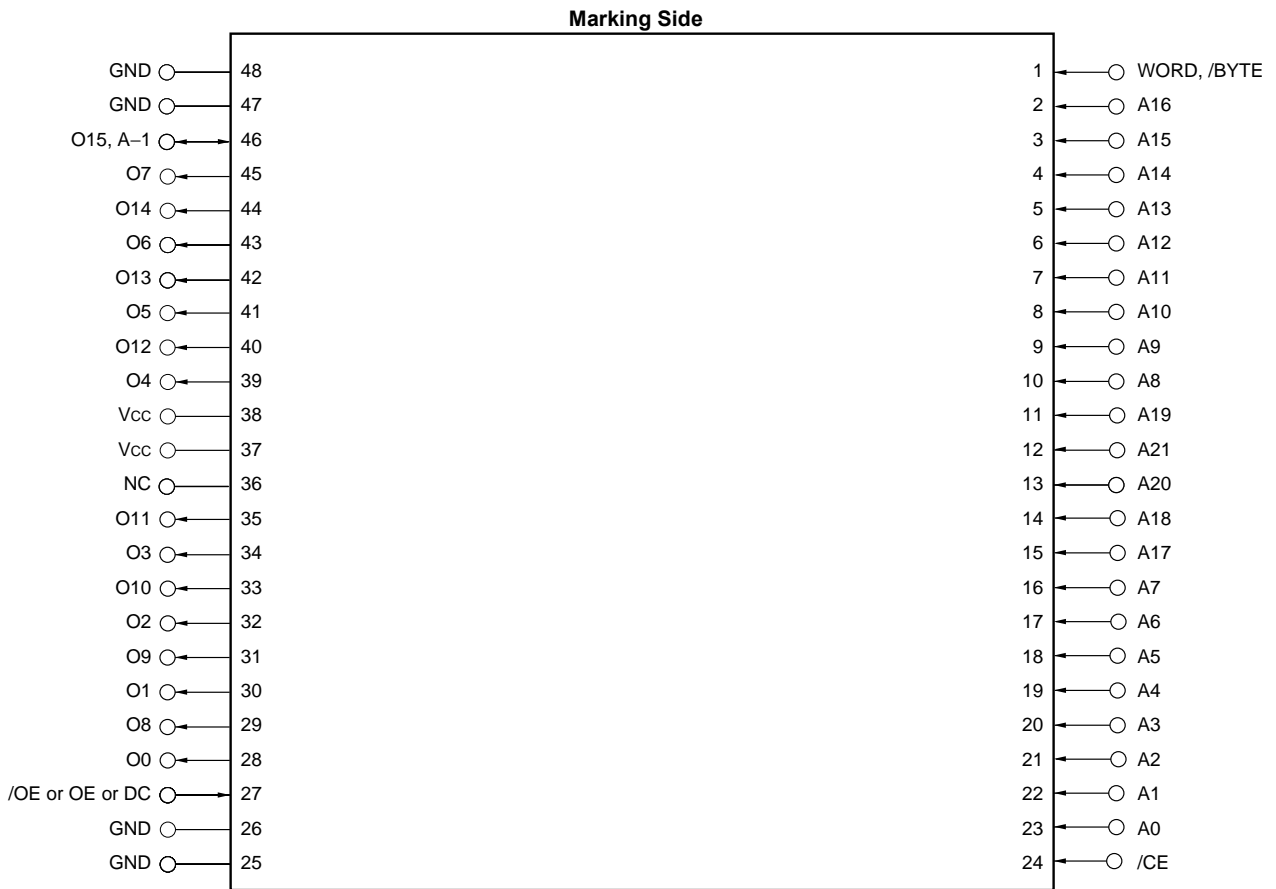


- A0 to A21 : Address inputs
- O0 to O7, O8 to O14 : Data outputs
- O15, A-1 : Data output 15 (WORD mode),  
LSB Address input (BYTE mode)
- WORD, /BYTE : Mode select
- /CE : Chip Enable
- /OE or OE : Output Enable
- Vcc : Supply voltage
- GND : Ground
- NC <sup>Note</sup> : No Connection
- DC : Don't Care

**Note** Some signals can be applied because this pin is not connected to the inside of the chip.

**Remark** Refer to **Package Drawings** for the 1-pin index mark.

48-pin PLASTIC TSOP (I) (12 × 18) (Reverse bent)  
 [ μPD23C64000JLGY-xxx-MKH ]



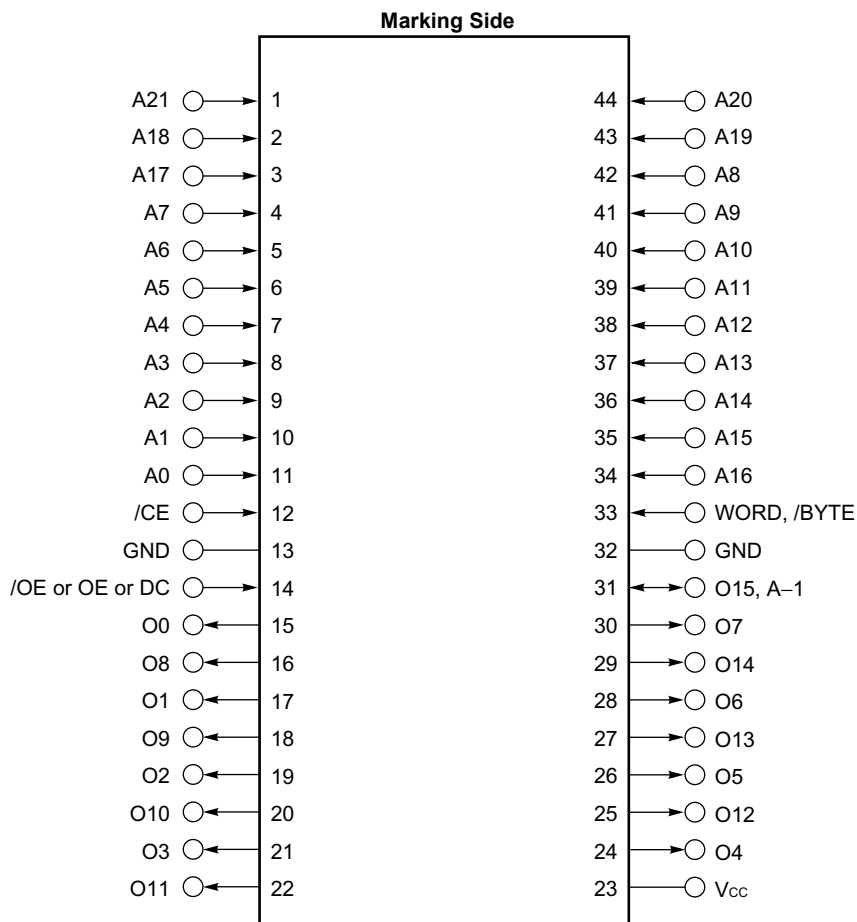
- A0 to A21 : Address inputs
- O0 to O7, O8 to O14 : Data outputs
- O15, A-1 : Data Output 15 (WORD mode),  
LSB Address input (BYTE mode)
- WORD, /BYTE : Mode select
- /CE : Chip Enable
- /OE or OE : Output Enable
- Vcc : Supply voltage
- GND : Ground
- NC <sup>Note</sup> : No Connection
- DC : Don't Care

**Note** Some signals can be applied because this pin is not connected to the inside of the chip.

**Remark** Refer to **Package Drawings** for the 1-pin index mark.

44-pin PLASTIC SOP (15.24 mm (600))

[ μPD23C64000JLGX-xxx ]



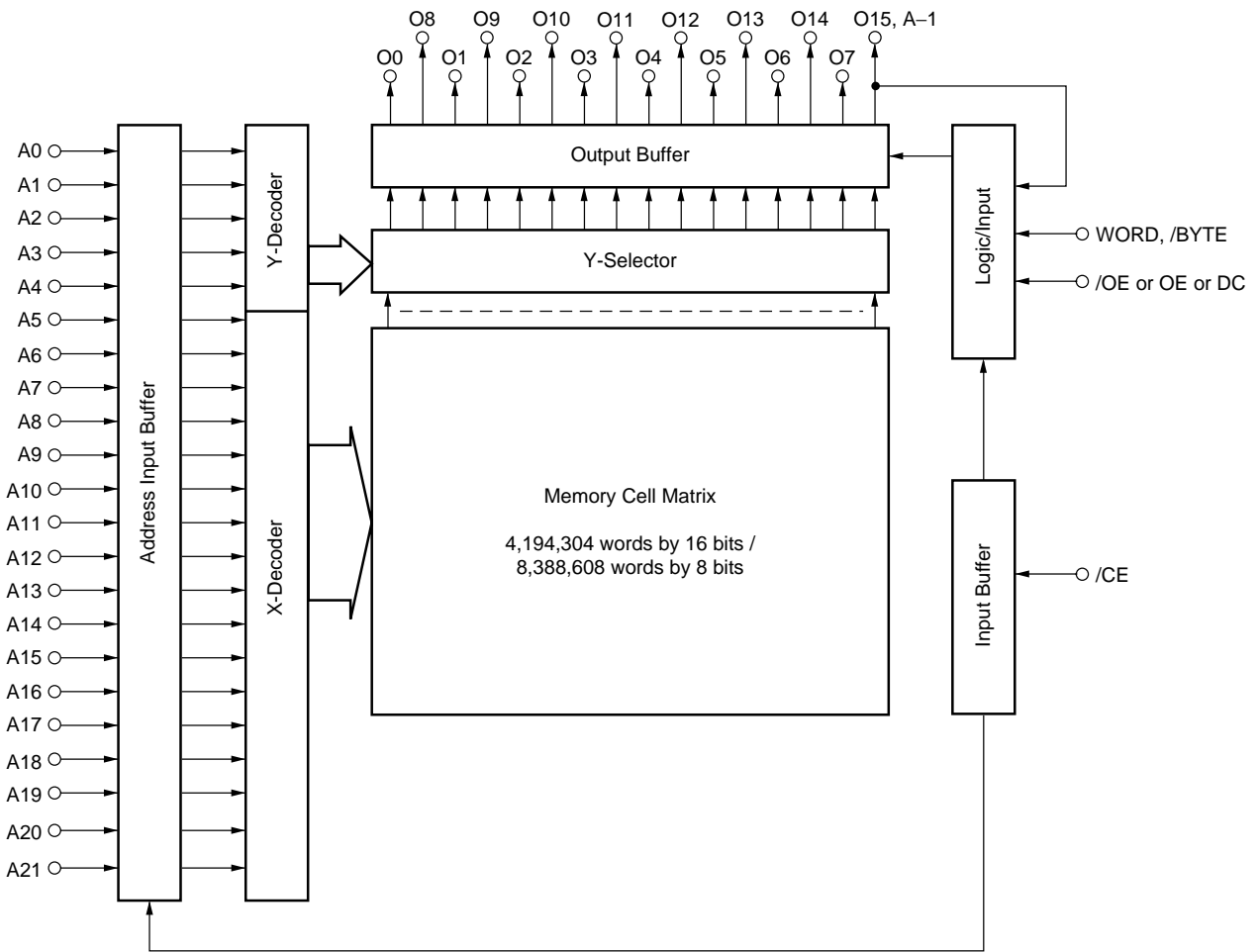
- A0 to A21 : Address inputs
- O0 to O7, O8 to O14 : Data outputs
- O15, A-1 : Data Output 15 (WORD mode),  
LSB Address input (BYTE mode)
- WORD, /BYTE : Mode select
- /CE : Chip Enable
- /OE or OE : Output Enable
- Vcc : Supply voltage
- GND : Ground
- DC : Don't Care

**Remark** Refer to **Package Drawings** for the 1-pin index mark.

## Input / Output Pin Functions

Pin name	Input / Output	Function
WORD, /BYTE	Input	The pin for switching WORD mode and BYTE mode. <b>High level</b> : WORD mode (4M-word by 16-bit) <b>Low level</b> : BYTE mode (8M-word by 8-bit)
A0 to A21 (Address inputs)	Input	Address input pins. A0 to A21 are used differently in the WORD mode and the BYTE mode. <b>WORD mode (4M-word by 16-bit)</b> A0 to A21 are used as 22 bits address signals. <b>BYTE mode (8M-word by 8-bit)</b> A0 to A21 are used as the upper 22 bits of total 23 bits of address signal. (The least significant bit (A-1) is combined to O15.)
O0 to O7, O8 to O14 (Data outputs)	Output	Data output pins. O0 to O7, O8 to O14 are used differently in the WORD mode and the BYTE mode. <b>WORD mode (4M-word by 16-bit)</b> The lower 15 bits of 16 bits data outputs to O0 to O14. (The most significant bit (O15) combined to A-1.) <b>BYTE mode (8M-word by 8-bit)</b> 8 bits data outputs to O0 to O7 and also O8 to O14 are high impedance.
O15, A-1 (Data output 15, LSB Address input)	Output, Input	O15, A-1 are used differently in the WORD mode and the BYTE mode. <b>WORD mode (4M-word by 16-bit)</b> The most significant output data bus (O15). <b>BYTE mode (8M-word by 8-bit)</b> The least significant address bus (A-1).
/CE (Chip Enable)	Input	Chip activating signal. When the OE is active, output states are following. <b>High level</b> : High-Z <b>Low level</b> : Data out
/OE or OE or DC (Output Enable, Don't Care)	Input	Output enable signal. The active level of OE is mask option. The active level of OE can be selected from high active, low active and Don't care at order.
V <sub>cc</sub>	–	Supply voltage
GND	–	Ground
NC	–	Not internally connected (The signal can be connected).

Block Diagram



**Mask Option**

The active levels of output enable pin (/OE or OE or DC) are mask programmable and optional, and can be selected from among "0" "1" "×" shown in the table below.

Option	/OE or OE or DC	OE active level
0	/OE	L
1	OE	H
×	DC	Don't care

Operation modes for each option are shown in the tables below.

Operation mode (Option : 0)

/CE	/OE	Mode	Output state
L	L	Active	Data out
	H		High-Z
H	H or L	Standby	High-Z

Operation mode (Option : 1)

/CE	OE	Mode	Output state
L	L	Active	High-Z
	H		Data out
H	H or L	Standby	High-Z

Operation mode (Option : ×)

/CE	DC	Mode	Output state
L	H or L	Active	Data out
H	H or L	Standby	High-Z

**Remark** L : Low level input  
 H : High level input

**Electrical Specifications**

**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V <sub>CC</sub>		-0.3 to +4.6	V
Input voltage	V <sub>I</sub>		-0.3 to V <sub>CC</sub> + 0.3	V
Output voltage	V <sub>O</sub>		-0.3 to V <sub>CC</sub> + 0.3	V
Operating ambient temperature	T <sub>A</sub>		-10 to +70	°C
Storage temperature	T <sub>stg</sub>		-65 to +150	°C

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Capacitance (T<sub>A</sub> = 25 °C)**

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>I</sub>	f = 1 MHz			10	pF
Output capacitance	C <sub>O</sub>				12	pF

**DC Characteristics (T<sub>A</sub> = -10 to +70 °C, V<sub>CC</sub> = 2.7 to 3.6 V)**

Parameter	Symbol	Test condition		MIN.	TYP.	MAX.	Unit
High level input voltage	V <sub>IH</sub>			2.0		V <sub>CC</sub> + 0.3	V
Low level input voltage	V <sub>IL</sub>	V <sub>CC</sub> = 3.0 V ± 0.3 V		-0.3		+0.5	V
		V <sub>CC</sub> = 3.3 V ± 0.3 V		-0.3		+0.8	
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -100 μA		2.4			V
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA				0.4	V
Input leakage current	I <sub>LI</sub>	V <sub>I</sub> = 0 V to V <sub>CC</sub>		-10		+10	μA
Output leakage current	I <sub>LO</sub>	V <sub>O</sub> = 0 V to V <sub>CC</sub> , Chip deselected		-10		+10	μA
Power supply current	I <sub>CC1</sub>	/CE = V <sub>IL</sub> (Active mode), I <sub>O</sub> = 0 mA	V <sub>CC</sub> = 3.0 V ± 0.3 V	TSOP (I)		40	mA
				SOP		35	
		V <sub>CC</sub> = 3.3 V ± 0.3 V	TSOP (I)		55		
			SOP		50		
Standby current	I <sub>CC3</sub>	/CE = V <sub>CC</sub> - 0.2 V (Standby mode)				30	μA



**AC Characteristics (T<sub>A</sub> = -10 to +70 °C, V<sub>CC</sub> = 2.7 to 3.6 V)**

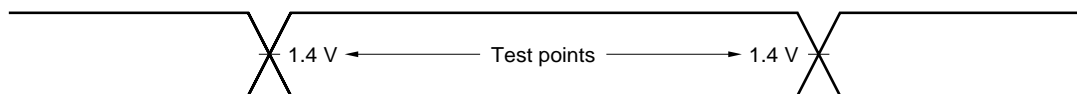
Parameter	Symbol	Test condition	V <sub>CC</sub> = 3.0 V ± 0.3 V			V <sub>CC</sub> = 3.3 V ± 0.3 V			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Address access time	t <sub>ACC</sub>	TSOP (I)			100			90	ns
		SOP			120			100	
★ Address skew time	t <sub>SKEW</sub>	<b>Note</b>			10			10	ns
Chip enable access time	t <sub>CE</sub>	TSOP (I)			100			90	ns
		SOP			120			100	
Output enable access time	t <sub>OE</sub>				25			25	ns
Output hold time	t <sub>OH</sub>		0			0			ns
Output disable time	t <sub>DF</sub>		0		25	0		25	ns
WORD, /BYTE access time	t <sub>WB</sub>	TSOP (I)			100			90	ns
		SOP			120			100	

- ★ **Note** t<sub>SKEW</sub> indicates the following three types of time depending on the condition.
- 1) When switching /CE from high level to low level, t<sub>SKEW</sub> is the time from the /CE low level input point until the next address is determined.
  - 2) When switching /CE from low level to high level, t<sub>SKEW</sub> is the time from the address change start point to the /CE high level input point.
  - 3) When /CE is fixed to low level, t<sub>SKEW</sub> is the time from the address change start point until the next address is determined.
- Since specs are defined for t<sub>SKEW</sub> only when /CE is active, t<sub>SKEW</sub> is not subject to limitations when /CE is switched from high level to low level following address determination, or when the address is changed after /CE is switched from low level to high level.

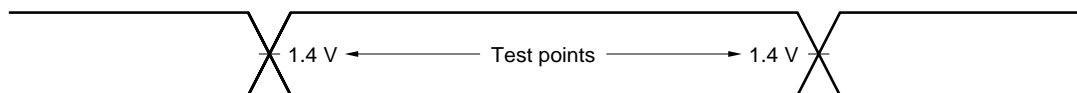
**Remark** t<sub>DF</sub> is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.

**AC Test Conditions**

**Input waveform (Rise / Fall Time ≤ 5 ns)**



**Output waveform**



**Output load**

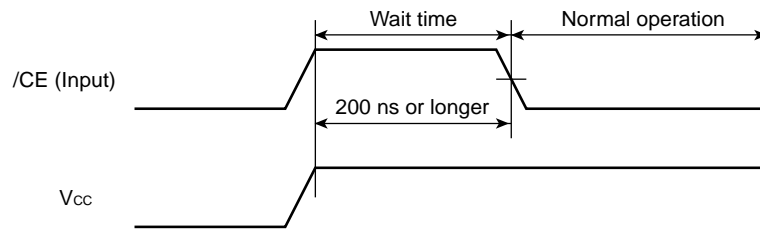
1 TTL + 100 pF

★ **Cautions on power application**

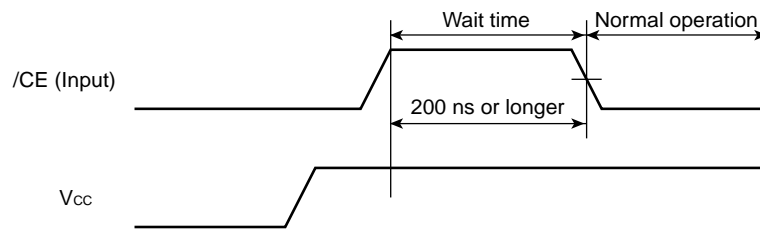
To ensure normal operation, always apply power using /CE following the procedure shown below.

- 1) Input a high level to /CE during and after power application.
- 2) Hold the high level input to /CE for 200 ns or longer (wait time).
- 3) Start normal operation after the wait time has elapsed.

**Power Application Timing Chart 1 (When /CE is made high at power application)**

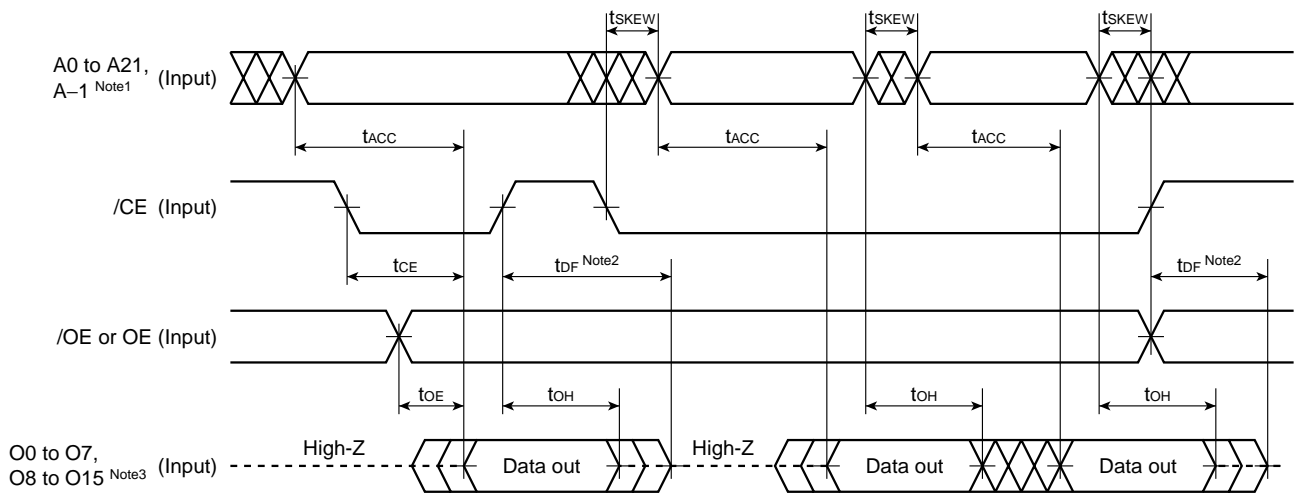


**Power Application Timing Chart 2 (When /CE is made high after power application)**



**Caution** Other signals can be either high or low during the wait time.

★ Read Cycle Timing Chart

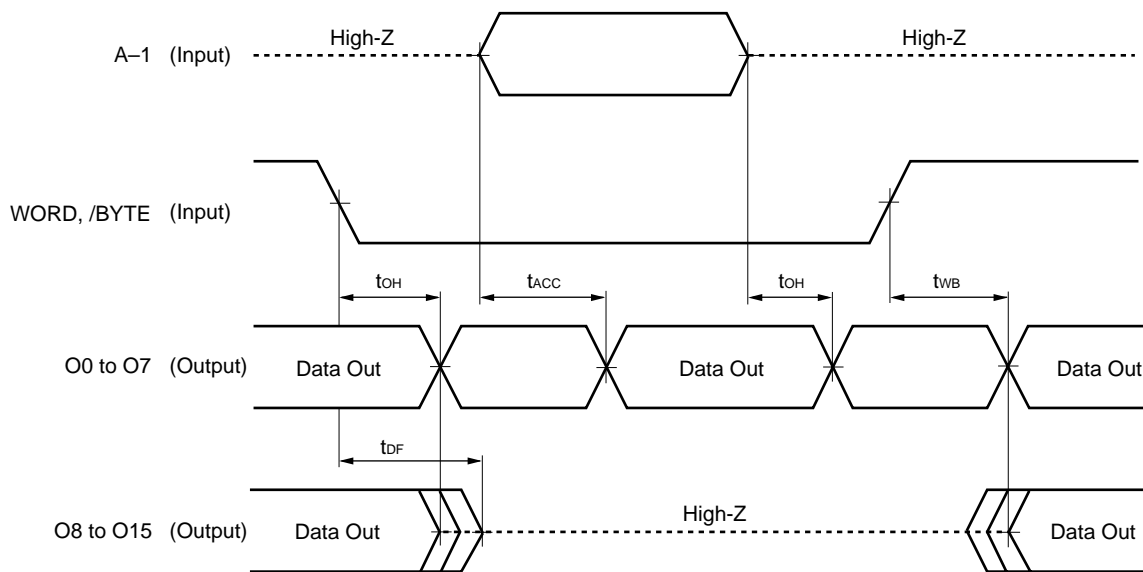


**Notes 1.** During WORD mode, A-1 is O15.

**2.**  $t_{DF}$  is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.

**3.** During BYTE mode, O8 to O14 are high impedance and O15 is A-1.

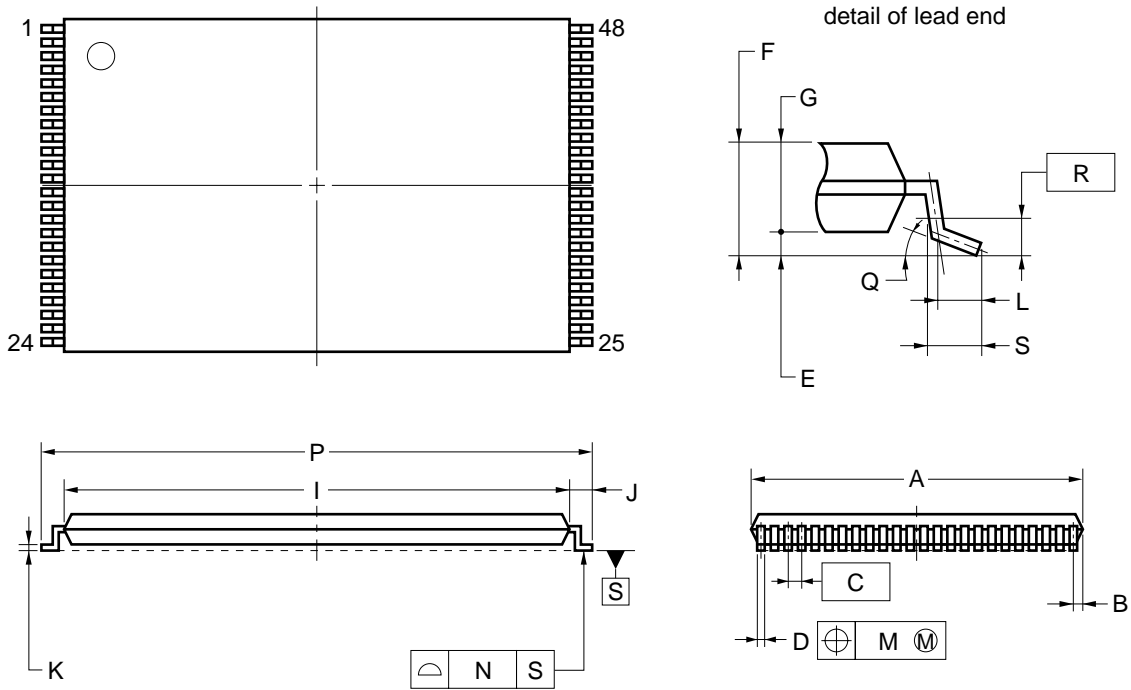
**WORD, /BYTE Switch Timing Chart**



**Remark** Chip Enable (/CE) and Output Enable (/OE or OE) : Active.

Package Drawings

48-PIN PLASTIC TSOP(I) (12x18)



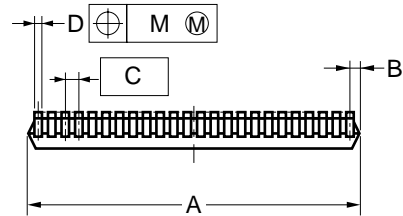
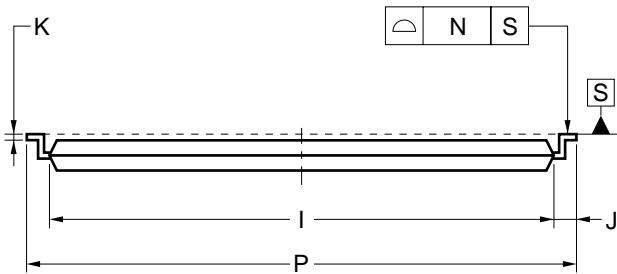
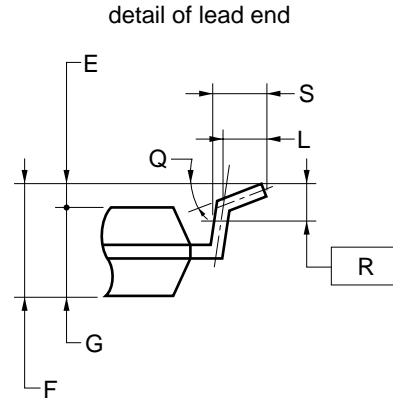
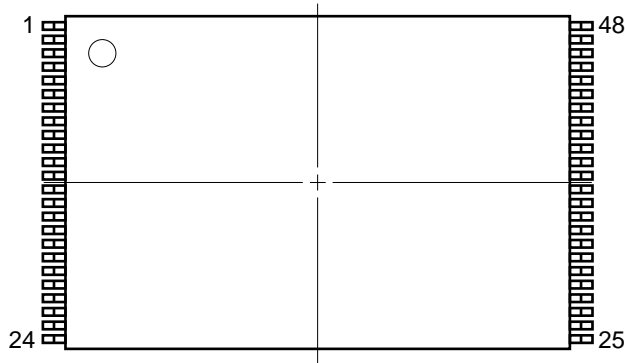
NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	16.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	18.0±0.2
Q	3° <sup>+5°</sup> <sub>-3°</sub>
R	0.25
S	0.60±0.15

S48GY-50-MJH1-1

48-PIN PLASTIC TSOP(I) (12x18)



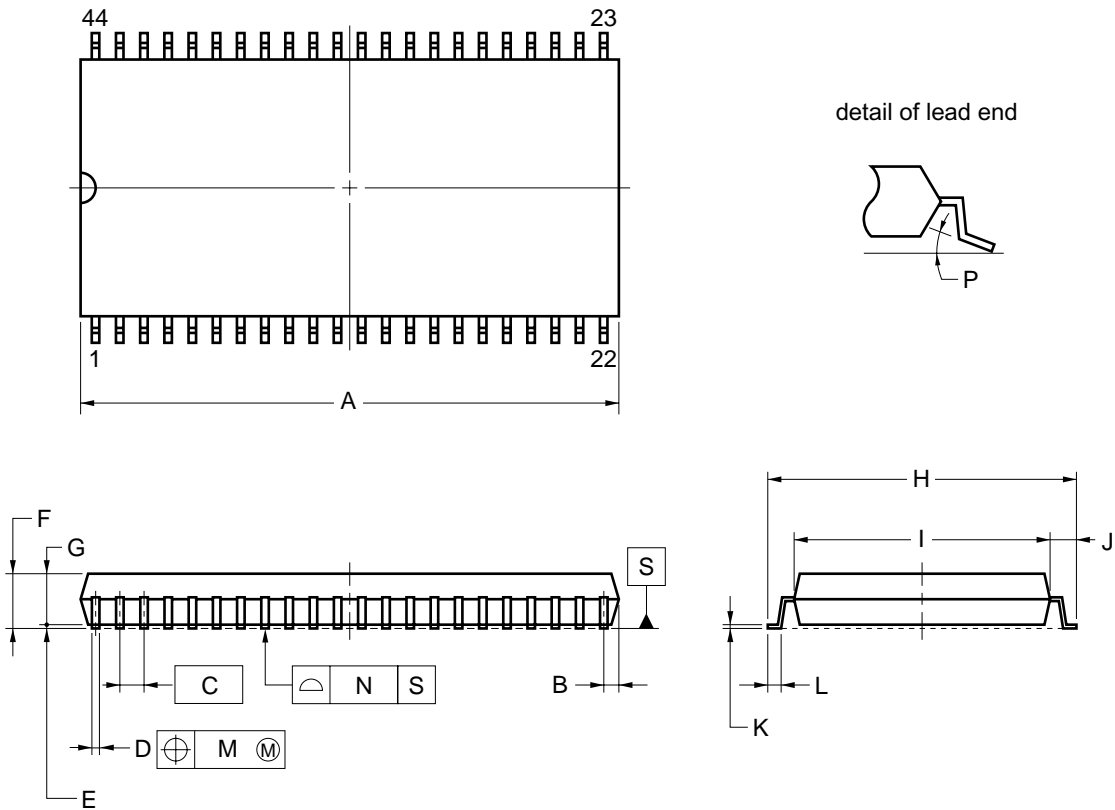
NOTES

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ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	16.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	18.0±0.2
Q	3°+5° -3°
R	0.25
S	0.60±0.15

S48GY-50-MKH1-1

44-PIN PLASTIC SOP (15.24 mm (600))



**NOTE**

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	27.83 <sup>+0.4</sup> <sub>-0.05</sub>
B	0.78 MAX.
C	1.27 (T.P.)
D	0.42 <sup>+0.08</sup> <sub>-0.07</sub>
E	0.15±0.1
F	3.0 MAX.
G	2.7±0.05
H	16.04±0.3
I	13.24±0.1
J	1.4±0.2
K	0.22 <sup>+0.08</sup> <sub>-0.07</sub>
L	0.8±0.2
M	0.12
N	0.10
P	3° <sup>+7°</sup> <sub>-3°</sub>

P44GX-50-600A-4

## Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the  $\mu$ PD23C64000JL.

## Types of Surface Mount Device

$\mu$ PD23C64000JLGY-xxx-MJH : 48-pin PLASTIC TSOP (I) (12 × 18) (Normal bent)

$\mu$ PD23C64000JLGY-xxx-MKH : 48-pin PLASTIC TSOP (I) (12 × 18) (Reverse bent)

$\mu$ PD23C64000JLGX-xxx : 44-pin PLASTIC SOP (15.24 mm (600))

**Revision History**

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
4th edition/ Feb. 2003	p.9	p.9	Addition	AC Characteristics	Address skew time ( $t_{SKEW}$ ) Note
	p.10	—	Addition		Cautions on power application
	p.11	p.10	Modification		Read Cycle Timing Chart



[MEMO]

[MEMO]

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF THE APPLIED WAVEFORM OF INPUT PINS AND THE UNUSED INPUT PINS FOR CMOS**

Note:

Input levels of CMOS devices must be fixed. CMOS devices behave differently than Bipolar or NMOS devices. If the input of a CMOS device stays in an area that is between  $V_{IL}$  (MAX.) and  $V_{IH}$  (MIN.) due to the effects of noise or some other irregularity, malfunction may result. Therefore, not only the input waveform is fixed, but also the waveform changes, it is important to use the CMOS device under AC test conditions. For unused input pins in particular, CMOS devices should not be operated in a state where nothing is connected, so input levels of CMOS devices must be fixed to high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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