NEC

NEC Electronics U.S.A. Inc

microcomputer division

65 3559 RCS 003554 0816 NEC

μPD2732A-2 μPD2732A, μPD2732A-3 32,768- (4K x 8) BIT UV ERASABLE PROM

Description

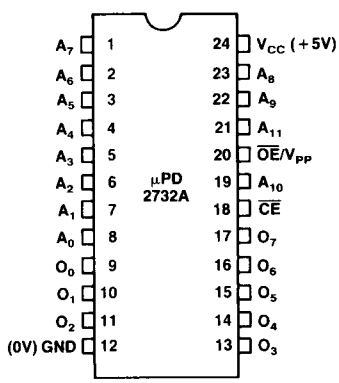
The μPD2732A is a 32,768- (4,096 x 8) bit ultraviolet erasable and electrically programmable read-only memory (EPROM). It operates from a single +5V supply, making it ideal for microprocessor applications. It features an output enable control and offers a standby mode with an attendant 75% savings in power consumption.

A distinctive feature of the μPD2732A is a separate output enable control ($\overline{OE}$) from the chip enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple-bus microprocessor systems. The μPD2732A features fast, simple one-pulse programming controlled by TTL-level signals. Total programming time for all 32,768 bits is only 210 seconds.

Features

- ☐ Ultraviolet erasable and electrically programmable
- ☐ Access time — 200ns max
- ☐ Single location programming
- ☐ Programmable with single pulse
- ☐ Low power dissipation: 125mA max active current
  30mA max standby current
- ☐ Input/Output TTL-compatible for reading and programming
- ☐ Single +5V power supply
- ☐ 24-pin ceramic DIP
- ☐ 21V programming

Pin Configuration



Handle With Care

Single Copy

Pin Names

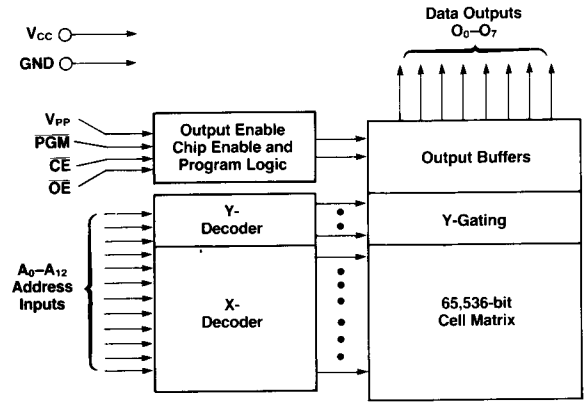
A_0–A_{11}	Addresses
$\overline{OE}$	Output Enable
O_0–O_7	Data Outputs
$\overline{CE}$	Chip Enable

Mode Selection

Pins / Mode	CE	$\overline{OE}/V_{PP}$	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

Table 1 — Mode Selection

Block Diagram



Absolute Maximum Ratings*

T_a = 25°C

Operating Temperature	−10°C to +80°C
Storage Temperature	−65°C to +125°C
Output Voltage	−0.3V to +6V
Input Voltage	−0.3V to +6.5V
Supply Voltage V_{CC}	−0.3V to +6V
Supply Voltage V_{PP}	−0.3V to +22V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°C; f = 1MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance Except $\overline{OE}/V_{PP}$	C_{IN1}		4	6	pF	V_{IN} = 0V
$\overline{OE}/V_{PP}$ Input Capacitance	C_{IN2}			20	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}			12	pF	V_{OUT} = 0V

DC Characteristics

Read Mode and Standby Mode

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

Parameter		Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output High Voltage		V_{OH}	2.4			V	I_{OH} = −400μA
Output Low Voltage		V_{OL}			0.45	V	I_{OL} = 2.1mA
Input High Voltage		V_{IH}	2.0		V_{CC} + 1	V	
Input Low Voltage		V_{IL}	−0.1		0.8	V	
Output Leakage Current		I_{LO}			10	μA	V_{OUT} = 5.25V
Input Leakage Current	except $\overline{OE}/V_{PP}$	I_{LI1}			10	μA	V_{IN} = 5.25V
	$\overline{OE}/V_{PP}$	I_{LI2}			10	μA	V_{IN} = 5.25V
V_{CC} Current	Standby	I_{CC1}			30	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}/V_{PP}$ = V_{CC}
	Active	I_{CC2}			125	mA	$\overline{OE}/V_{PP}$ = $\overline{CE}$ = V_{IL}

DC Characteristics (Cont.)

Program, Program Verify, and Program Inhibit Modes

T_a = 25°C ± 5°C; V_{CC} = +5V ± 5%; V_{PP} = +21V ± 0.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0		V_{CC} + 1	V	
Input Low Voltage	V_{IL}	−0.1		0.8	V	
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1mA
V_{CC} Current	I_{CC}		85	125	mA	
V_{PP} Current	I_{PP}			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$

AC Characteristics

Read Mode and Standby Mode

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

Parameter	Symbol	Limits 2732A-2 Min	Typ	Max	2732A Min	Typ	Max	2732A-3 Min	Typ	Max	Unit	Test Conditions
Address to Output Delay	t_{ACC}			200			250			300	ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
CE to Output Delay	t_{CE}			200			250			300	ns	$\overline{OE} = V_{IL}$
Output Enable to Output Delay	t_{OE}			70			100			150	ns	$\overline{CE} = V_{IL}$
Output Enable High to Output Float	t_{DF}			60			90			130	ns	$\overline{CE} = V_{IH}$
Address to Output Hold	t_{OH}	0			0			0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

Test Conditions —
Output Load: 1 TTL gate and C_L = 100pF
Input Rise and Fall Times: 20ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Levels:
Inputs: 1.0V and 2.0V
Outputs: 0.8V and 2.0V

Program, Program Verify, and Program Inhibit Modes

T_a = 25°C ± 5°C; V_{CC} = +5V ± 5%; V_{PP} = +21V ± 0.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address Setup Time	t_{AS}	2			μs	
OE Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	0			μs	
OE Hold Time	t_{OEH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Output Enable to Output Float Delay	t_{DF}	0		130	ns	
Data Valid from CE	t_{DV}			1	μs	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$
Program Pulse Width	t_{PW}	45	50	55	ms	
Program Pulse Rise Time	t_{PRT}	50			ns	
V_{PP} Recovery Time	t_{VR}	2			μs	

Test Conditions —
Input Pulse Levels: 0.8V to 2.2V
Input Timing Reference Levels: 1.0V and 2.0V
Output Timing Reference Levels: 0.8V and 2V
Input Rise and Fall Times: 20ns

Function

The μPD2732A operates from a single +5V power supply, making it ideal for microprocessor applications.

Programming of the μPD2732A is achieved with a single 50ms TTL pulse. Total programming time for all 32,768 bits is only 210 seconds. Due to the simplicity of the programming requirements, devices on boards and in systems may be easily programmed without any special programmer.

The μPD2732A features a Standby mode which reduces the power dissipation from a maximum active power dissipation of 656mW to a maximum standby power dissipation of 158mW. This results in a 75% savings with no increase in access time.

Erasure of the μPD2732A programmed data can be attained when exposed to light with wavelengths shorter than approximately 4,000 Angstroms (Å). It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD2732A. Consequently, if the μPD2732A is to be exposed to these types of lighting conditions for long periods of time, its window should be masked to prevent unintentional erasure.

The recommended erasure procedure for the μPD2732A is exposure to ultraviolet light with wavelengths of 2,537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be not less than 15W-sec/cm^2. The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12,000μW/cm^2 power rating.

During erasure, the μPD2732A should be placed within 1 inch of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

Operation

The five operation modes of the μPD2732A are listed in Table 1. In the Read mode the only power supply required is a +5V supply. During programming, all inputs are TTL levels except for $\overline{OE}/V_{PP}$ which is pulsed from TTL level to 21V.

Read Mode

When $\overline{CE}$ and $\overline{OE}/V_{PP}$ are at a low (0) level, read is set and data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

Standby Mode

The μPD2732A is placed in a Standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$ input. In this mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ input. The active power dissipation is reduced by 75% from 656mW to 158mW.

Program Mode

Programming begins by erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The μPD2732A is placed in the Program mode by applying a high (1) level TTL signal to the $\overline{CE}$ and with $\overline{OE}/V_{PP}$ at +21V. The data to be programmed is applied to the output pins in 8-bit parallel form at TTL levels.

Any location can be programmed at any time, either individually, sequentially, or at random.

When multiple μPD2732As are connected in parallel, except for $\overline{CE}$, individual μPD2732As can be programmed by applying a low (0) level TTL pulse to the $\overline{CE}$ input of the desired μPD2732A to be programmed.

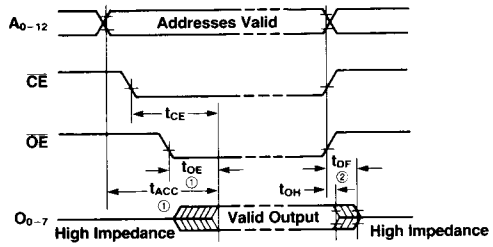
Programming of multiple μPD2732As in parallel with the same data is easily accomplished. All the like inputs are tied together and programmed by applying a low (0) level TTL pulse to the $\overline{CE}$ inputs.

Program Inhibit Mode

Programming multiple μPD2732As in parallel with different data is easier with the Program Inhibit mode. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel μPD2732As may be common. Programming is accomplished by applying the TTL-level program pulse to the $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at +21V. A high (1) level applied to the $\overline{CE}$ of the other μPD2732A will inhibit it from being programmed.

Timing Waveforms

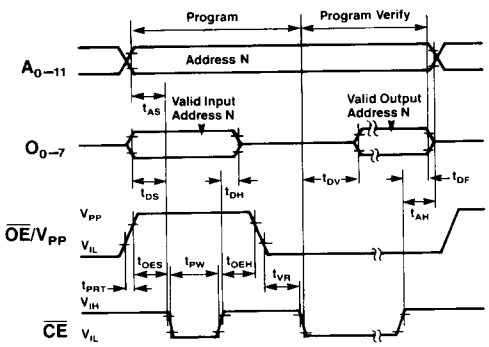
Read Mode



Notes: ① $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Program Mode ①



Note: ① 0.1μF capacitor must be connected between $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.

Program Verify Mode

A verify should be performed on the programmed bits to determine that the data was correctly programmed. The program verify can be performed with $\overline{CE}$ and $\overline{OE}/V_{PP}$ at low (0) levels.

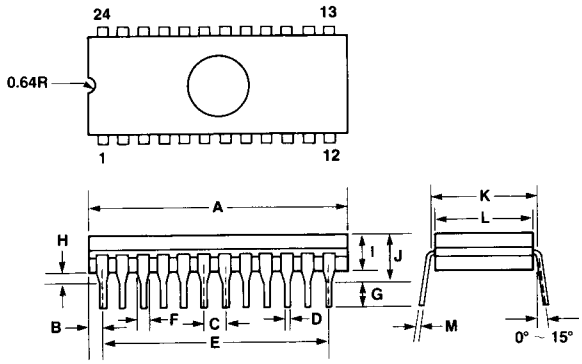
Output Deselect

The data outputs of two or more μPD2732As may be wire-ORed together to the same data bus. In order to prevent bus contention problems between devices, all but the selected μPD2732As should be deselected by raising the $\overline{OE}/V_{PP}$ input to a TTL high.

Window Label

An opaque window label is provided unattached for the convenience of the user. The window label filters ultra-violet light frequencies, thus preventing accidental erasure or long-term degradation caused by ambient light or sunlight.

Package Outline μPD2732AD (Cerdip)



Item	Millimeters	Inches
A	33.02 Max	1.3 Max
B	2.54	0.1
C	2.54 ± 0.25	0.1 ± 0.01
D	0.5 ± 0.10	0.020 ± 0.004
E	27.94	1.10
F	1.3	0.05
G	2.54 Min	0.1 Min
H	0.51 Min	0.020 Min
I	5.08 Max	0.20 Max
J	5.59 Max	0.22 Max
K	15.24	0.60
L	14.66	0.58
M	0.25 ± 0.05	0.010 ± 0.002

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2732DS - REV 1-4-83 - 8K/16K