

## Description

The μPD27C1001A is a 1,048,576-bit ultraviolet erasable and electrically programmable read-only memory (EPROM) fabricated with double-polysilicon CMOS technology for a substantial savings in both operating and standby power. The device is organized as 131,072 words by 8 bits and operates from a single +5-volt power supply.

The μPD27C1001A has both page and single-location programming features, three-state outputs, fully TTL-compatible inputs and outputs, and a program voltage ( $V_{PP}$ ) of 12.5 volts.

The μPD27C1001A is available in a 32-cerdip with a quartz window.

## Features

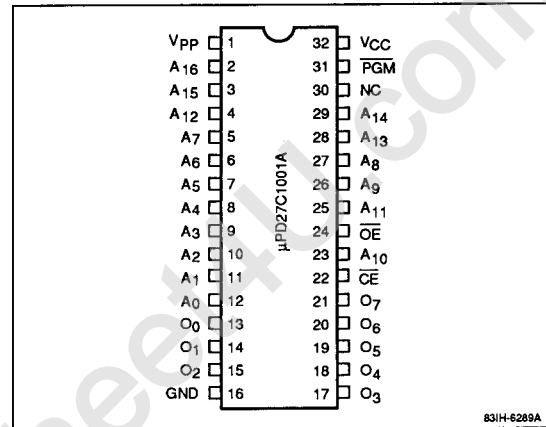
- 131,072-word x 8-bit organization
- Ultraviolet erasable and electrically programmable
- High-speed byte or page programming
- Low power dissipation
  - 40 mA active (max)
  - 100 μA standby (max)
- TTL-compatible I/O for reading and programming
- Single +5-volt power supply
- Double-polysilicon CMOS technology
- 32-pin cerdip packaging
- JEDEC-compatible pinout

## Ordering Information

Part Number	Access Time (max)	Package
μPD27C1001AD-12	120 ns	32-pin cerdip with a quartz window
D-15	150 ns	
D-20	200 ns	

## Pin Configuration

### 32-Pin Cerdip



## Pin Identification

Symbol	Function
$A_0 - A_{16}$	Address inputs
$O_0 - O_7$	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PGM}$	Program
GND	Ground
$V_{CC}$	+5-volt power supply
$V_{PP}$	Program voltage
NC	No connection

**Absolute Maximum Ratings**

Power supply voltage, $V_{CC}$	-0.6 to +7.0 V
Input voltage, $V_{IN}$	-0.6 to +7.0 V
Input voltage, $A_9$	-0.6 to +13.5 V
Output voltage, $V_{OUT}$	-0.6 to +7.0 V
Operating temperature, $T_{OPR}$	-10 to 80°C
Storage temperature, $T_{STG}$	-65 to 125°C
Program voltage, $V_{PP}$	-0.6 to +13.5 V

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

**Capacitance**

$T_A = 25^\circ\text{C}$ ;  $f = 1 \text{ MHz}$ ;  $V_{IN}$  and  $V_{OUT} = 0 \text{ V}$

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	$C_I$			14	pF
Output capacitance	$C_O$			16	pF

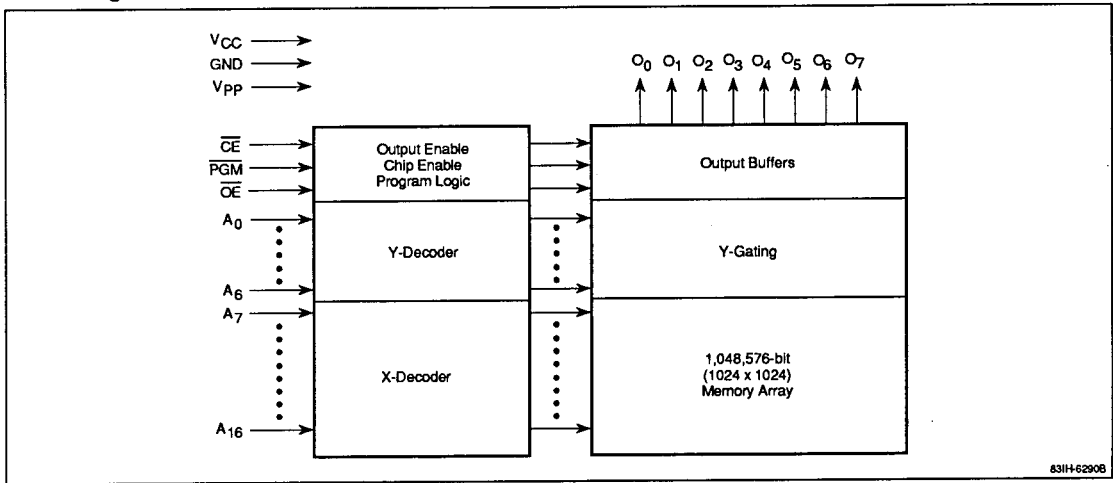
**Truth Table**

Function	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	$V_{PP}$	$V_{CC}$	Output
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	+5.0 V	+5.0 V	$D_{OUT}$
Output disable	$V_{IL}$	$V_{IH}$	X	+5.0 V	+5.0 V	High-Z
Standby	$V_{IH}$	X	X	+5.0 V	+5.0 V	High-Z
Page data latch	$V_{IH}$	$V_{IL}$	$V_{IH}$	+12.5 V	+6.5 V	$D_{IN}$
Page program	$V_{IH}$	$V_{IH}$	$V_{IL}$	+12.5 V	+6.5 V	High-Z
Byte program	$V_{IL}$	$V_{IH}$	$V_{IL}$	+12.5 V	+6.5 V	$D_{IN}$
Program verify	$V_{IL}$	$V_{IL}$	$V_{IH}$	+12.5 V	+6.5 V	$D_{OUT}$
Program inhibit	X	$V_{IL}$	$V_{IL}$	+12.5 V	+6.5 V	High-Z
	X	$V_{IH}$	$V_{IH}$			

**Notes:**

- (1) X can be either  $V_{IL}$  or  $V_{IH}$ .
- (2) In read operation,  $\overline{PGM}$  must be sent to  $V_{IH}$  at all times, or switched from  $V_{IL}$  to  $V_{IH}$  at least 2 μs before  $\overline{OE}$  or  $\overline{CE}$  goes to  $V_{IH}$ .

## Block Diagram



**Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
<b>Read Operation or Standby</b>					
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
	V <sub>PP</sub>	V <sub>CC</sub> - 0.6	V <sub>CC</sub>	V <sub>CC</sub> + 0.6	V
Input voltage, high	V <sub>IH</sub>	2.0		V <sub>CC</sub> + 0.3	V
Input voltage, low	V <sub>IL</sub>	-0.3		0.8	V
Operating temperature	T <sub>A</sub>	0		70	°C
<b>Programming Operation</b>					
Supply voltage	V <sub>CC</sub>	6.25	6.5	6.75	V
	V <sub>PP</sub>	12.2	12.5	12.8	V
Input voltage, high	V <sub>IH</sub>	2.4		V <sub>CC</sub> + 0.3	V
Input voltage, low	V <sub>IL</sub>	-0.3		0.8	V
Operating temperature	T <sub>A</sub>	20	25	30	°C

**DC Characteristics**

T<sub>A</sub> = 0 to +70°C; V<sub>CC</sub> = +5.0 V ± 10%; V<sub>PP</sub> = V<sub>CC</sub>

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Read Operation or Standby</b>						
Output voltage, high	V <sub>OH1</sub>	2.4			V	I <sub>OH</sub> = -400 μA
	V <sub>OH2</sub>	V <sub>CC</sub> - 0.7			V	I <sub>OH</sub> = -100 μA
Output voltage, low	V <sub>OL</sub>			0.45	V	I <sub>OL</sub> = 2.1 mA
Output leakage current	I <sub>LO</sub>	-10		10	μA	V <sub>OUT</sub> = 0 V to V <sub>CC</sub> ; $\overline{OE}$ = V <sub>IH</sub>
Input leakage current	I <sub>LI</sub>	-10		10	μA	V <sub>IN</sub> = 0 V to V <sub>CC</sub>
V <sub>PP</sub> current	I <sub>PP</sub>		1	100	μA	V <sub>PP</sub> = V <sub>CC</sub>
V <sub>CC</sub> current (active)	I <sub>CCA1</sub>			15	mA	$\overline{CE}$ = V <sub>IL</sub> ; V <sub>IN</sub> = V <sub>IH</sub>
				40	mA	f = 8.4 MHz; I <sub>OUT</sub> = 0 mA; t <sub>ACC</sub> = 120 ns
				30	mA	f = 6.7 MHz; I <sub>OUT</sub> = 0 mA; t <sub>ACC</sub> = 150 ns
				25	mA	f = 5 MHz; I <sub>OUT</sub> = 0 mA; t <sub>ACC</sub> = 200 ns
V <sub>CC</sub> current (standby)	I <sub>CCS1</sub>			1	mA	$\overline{CE}$ = V <sub>IH</sub> min
	I <sub>CCS2</sub>		1	100	μA	$\overline{CE}$ = V <sub>CC</sub> ; V <sub>IN</sub> = 0 V to V <sub>CC</sub>

**DC Characteristics (cont)**

T<sub>A</sub> = 25 ± 5°C; V<sub>CC</sub> = +6.5 V ± 0.25; V<sub>PP</sub> = +12.5 V ± 0.3

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Programming Operation</b>						
Output voltage, high	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = -400 μA
Output voltage, low	V <sub>OL</sub>			0.45	V	I <sub>OL</sub> = 2.1 mA
Input leakage current	I <sub>LI</sub>	-10		10	μA	V <sub>IN</sub> = 0 V to V <sub>CC</sub>
V <sub>PP</sub> current	I <sub>PP</sub>			50	mA	$\overline{CE}$ = $\overline{PGM}$ = V <sub>IL</sub>
V <sub>CC</sub> current	I <sub>CC</sub>			30	mA	

### AC Characteristics

$T_A = 0 \text{ to } +70^\circ\text{C}$ ;  $V_{CC} = +5.0 \text{ V} \pm 10\%$ ;  $V_{PP} = V_{CC} \pm 0.6 \text{ V}$

Parameter	Symbol	μPD27C1001A-12		μPD27C1001A-15		μPD27C1001A-20		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
<b>Read Operation or Standby</b>									
Address to output delay	$t_{ACC}$		120		150		200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	$t_{CE}$		120		150		200	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	$t_{OE}$		70		70		75	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to output float	$t_{DF}$	0	50	0	50	0	60	ns	$\overline{CE} = V_{IL}$ or $\overline{OE} = V_{IL}$
Address to output hold	$t_{OH}$	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

### AC Characteristics (cont)

$T_A = 25 \pm 5^\circ\text{C}$ ;  $V_{CC} = +6.5 \pm 0.25 \text{ V}$ ;  $V_{PP} = +12.5 \pm 0.3 \text{ V}$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Page Programming Operation</b>						
Address setup time	$t_{AS}$	2			μs	
$\overline{CE}$ setup time	$t_{CES}$	2			μs	
Data setup time	$t_{DS}$	2			μs	
Address hold time	$t_{AH}$	2			μs	
	$t_{AHL}$	2			μs	
	$t_{AHV}$	0			μs	
Data hold time	$t_{DH}$	2			μs	
$\overline{OE}$ to output float time	$t_{DF}$	0		130	ns	
$V_{PP}$ setup time	$t_{VPS}$	2			μs	
$V_{CC}$ setup time	$t_{VCS}$	2			μs	
Program pulse width	$t_{PW}$	0.095	0.1	0.105	ms	
$\overline{OE}$ setup time	$t_{OES}$	2			μs	
$\overline{OE}$ to output delay	$t_{OE}$			150	ns	
$\overline{OE}$ pulse width during data latch	$t_{LW}$	1			μs	
PGM setup time	$t_{PGMS}$	2			μs	
$\overline{CE}$ hold time	$t_{CEH}$	2			μs	
OE hold time	$t_{OEH}$	2			μs	

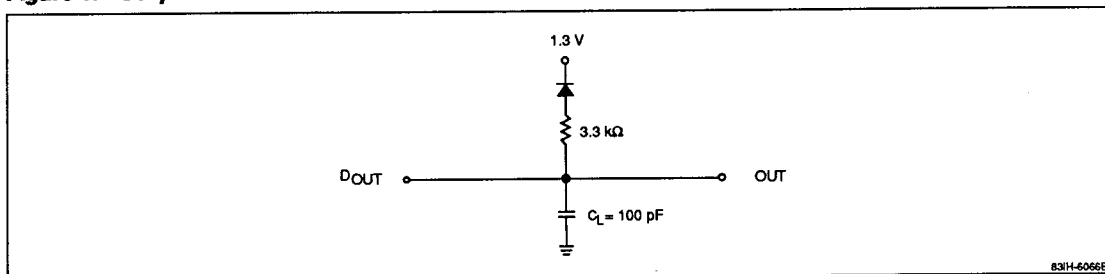
AC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Byte Programming Operation</b>						
Address setup time	$t_{AS}$	2			μs	
$\overline{OE}$ setup time	$t_{OES}$	2			μs	
Data setup time	$t_{DS}$	2			μs	
Address hold time	$t_{AH}$	2			μs	
Data hold time	$t_{DH}$	2			μs	
$\overline{OE}$ to output float time	$t_{DF}$	0		130	ns	
$V_{PP}$ setup time	$t_{VPS}$	2			μs	
$V_{CC}$ setup time	$t_{VCS}$	2			μs	
Program pulse width	$t_{PW}$	0.095	0.1	0.105	ms	
$\overline{OE}$ setup time	$t_{CES}$	2			μs	
$\overline{OE}$ to output delay	$t_{OE}$			150	ns	

Notes:

- (1) Input pulse levels = 0.45 to 2.4 V; input and output timing reference levels = 0.8 and 2.0 V; input rise and fall times ≤ 20 ns. See figure 1 for output load.

Figure 1. Output Load



831H-6066B

## Programming Operation

Begin programming by erasing all data; this sets all bits high. The μPD27C1001A is originally shipped in this condition. Address the first byte or page location and apply valid data at the eight output pins. Raise  $V_{CC}$  to  $+6.5 \pm 0.25$  V; then raise  $V_{PP}$  to  $+12.5 \pm 0.3$  V.

### Byte Programming

$\overline{CE}$  should be set low and  $\overline{OE}$  high to start programming at the initial byte address. Apply a 0.1 ms program pulse to  $\overline{PGM}$  as shown in the byte programming portion of the timing waveforms. Set  $\overline{OE}$  low to verify the eight bits prior to making a program/no program decision. If the byte is not programmed, apply another 0.1-ms pulse to  $\overline{PGM}$ , up to a maximum of 10 times, and input the next address. If the bits are not programmed in 10 tries, reject the device as a program failure. After all addresses are programmed, lower both  $V_{CC}$  and  $V_{PP}$  to  $+5.0$  V  $\pm 10\%$  and verify all data again.

### Page Programming

For page programming,  $\overline{CE}$  and  $\overline{PGM}$  should be set high.  $\overline{OE}$  pulses low four times to latch each of the 4 data bytes onto the page. Subsequently,  $\overline{CE}$  and  $\overline{OE}$  should be set high and a 0.1-ms program pulse applied to  $\overline{PGM}$  as shown in the page programming portion of the timing waveforms. Verify the data prior to making a program/no program decision. If all four bytes of page data are not programmed, apply another 0.1-ms pulse to  $\overline{PGM}$ , up to a maximum of 10 times, and input the next page address. If the page is not programmed in 10 tries, reject the device as a program failure. After all addresses are programmed, lower both  $V_{CC}$  and  $V_{PP}$  to  $+5.0$  V  $\pm 10\%$  and verify all data again.

## Program Inhibit

Use the program inhibit option to program multiple μPD27C1001As connected in parallel. All like inputs (except  $\overline{CE}$ , but including  $\overline{OE}$ ) may be common. Program individual devices by applying a low-level TTL pulse to the  $\overline{CE}$  input of the device to be programmed. Applying a high level to the  $\overline{CE}$  input of the other devices prevents them from being programmed.

## Program Verification

To verify that the device is correctly programmed, normal read cycles can be executed with a high logic level applied to the  $\overline{PGM}$  pin and a low logic level applied to the  $\overline{CE}$  and  $\overline{OE}$  pins of the device to be verified. The  $\overline{CE}$  and  $\overline{OE}$  pins of all other devices should be set high.

## Program Erasure

Erase data on the μPD27C1001A by exposing it to light with a wavelength shorter than 400 nm. Exposure to direct sunlight or fluorescent light could also erase the data. Consequently, mask the window to prevent unintentional erasure by ultraviolet rays. Opaque labels are supplied with every device.

Data is typically erased by ultraviolet rays of 254 nm. A lighting level of 15 W-sec/cm<sup>2</sup> (min) is required to completely erase written data (ultraviolet ray intensity multiplied by exposure time).

An ultraviolet lamp rated at 12,000 μW/cm<sup>2</sup> takes approximately 20 minutes to complete erasure. Place the μPD27C1001A within 2.5 cm of the lamp tubes. Remove any filter on the lamp.

Timing Waveforms

Page Programming Cycle

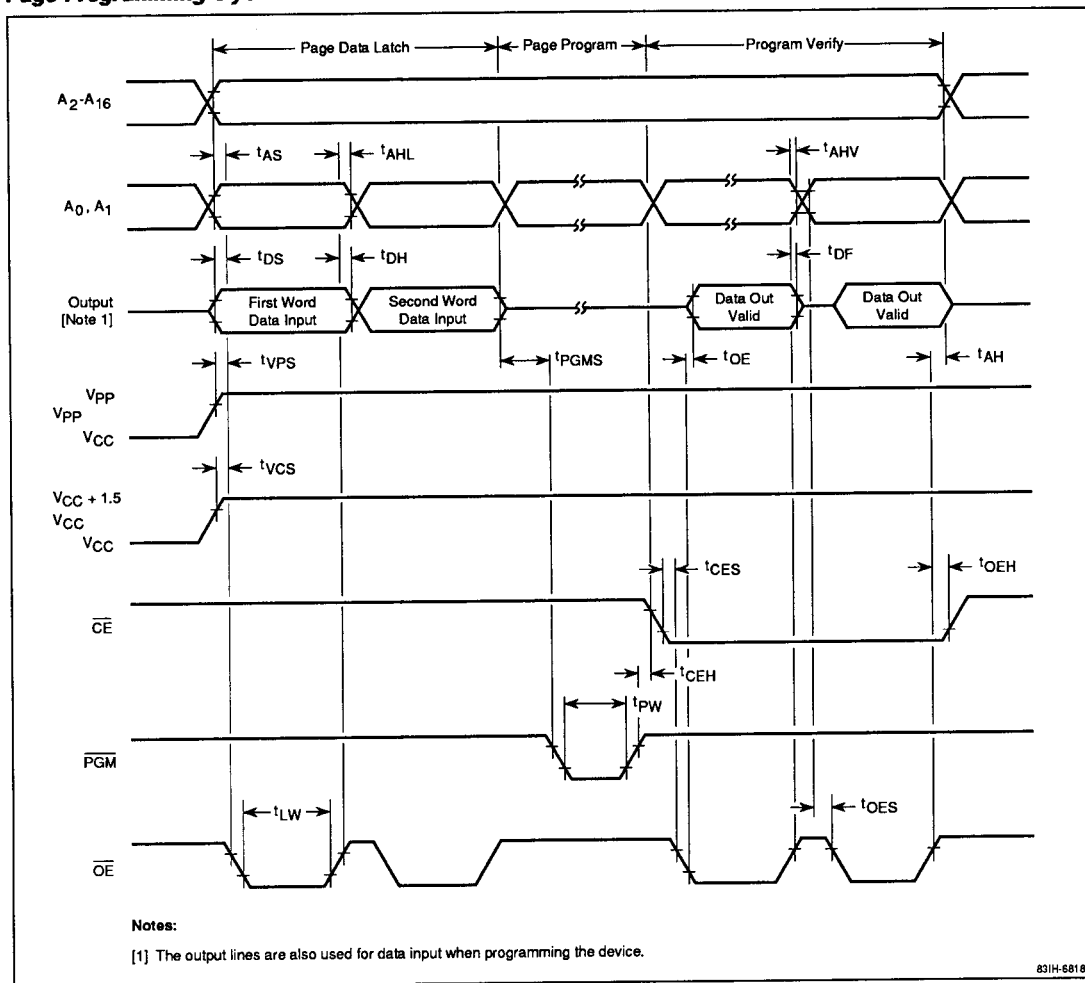
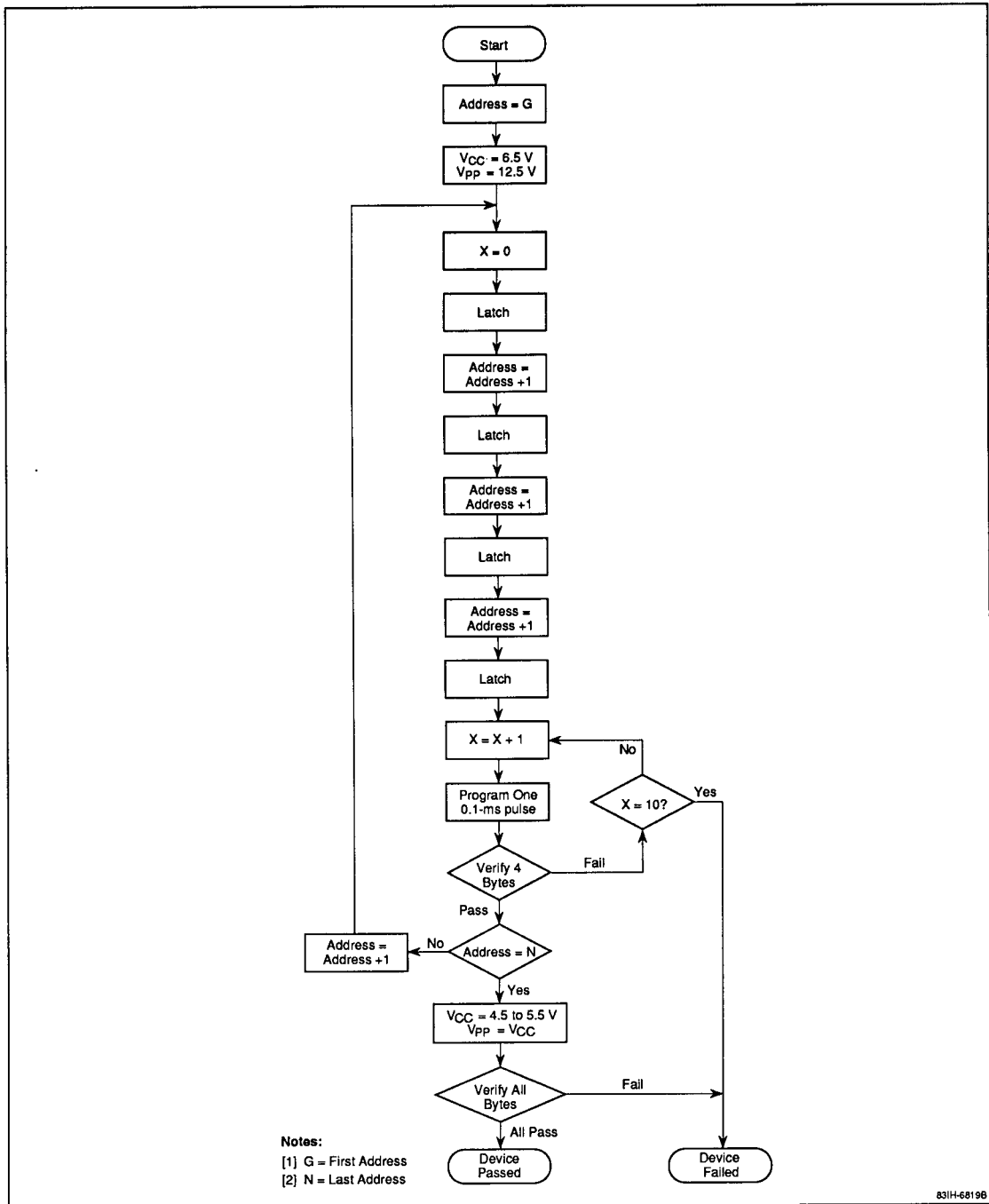




Figure 2. Page Programming Flowchart



Timing Waveforms (cont)

Byte Programming Cycle

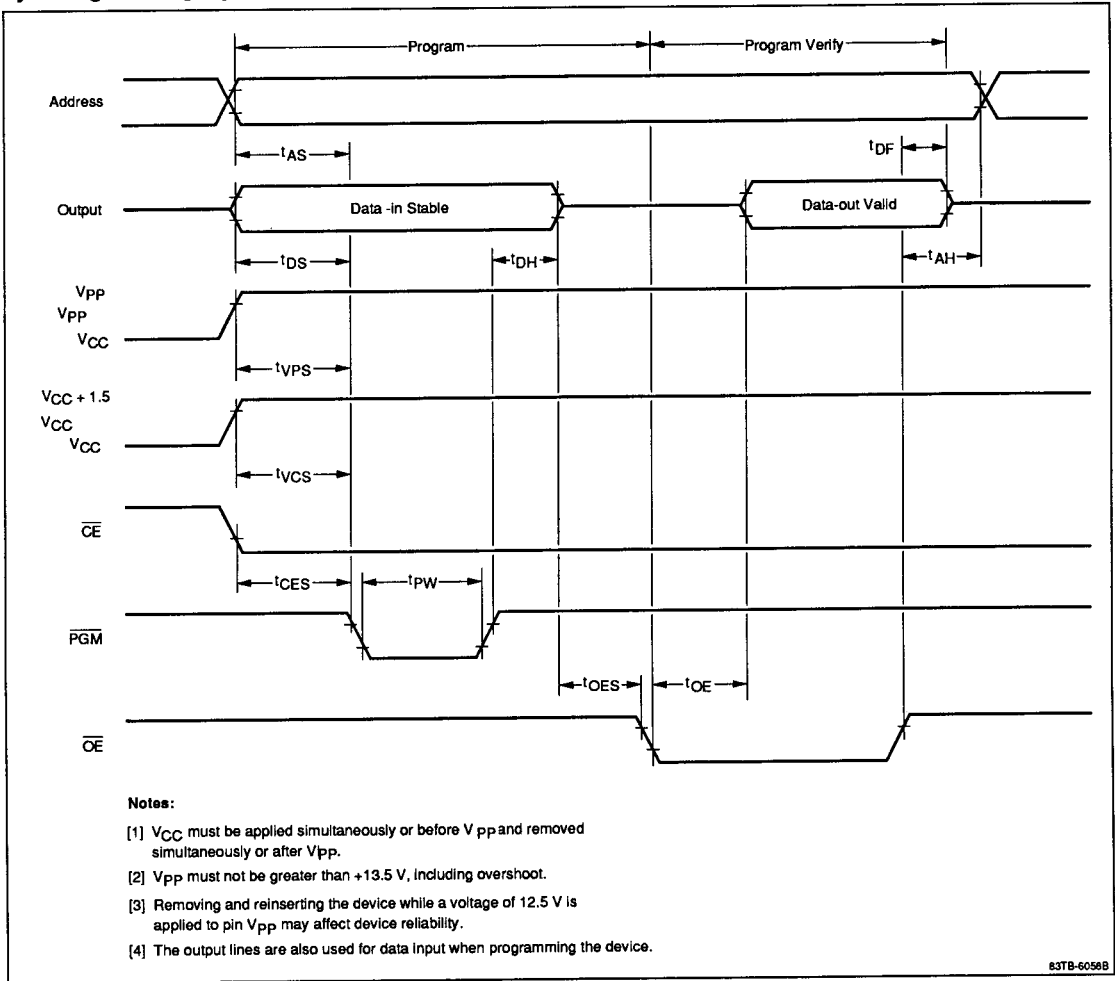
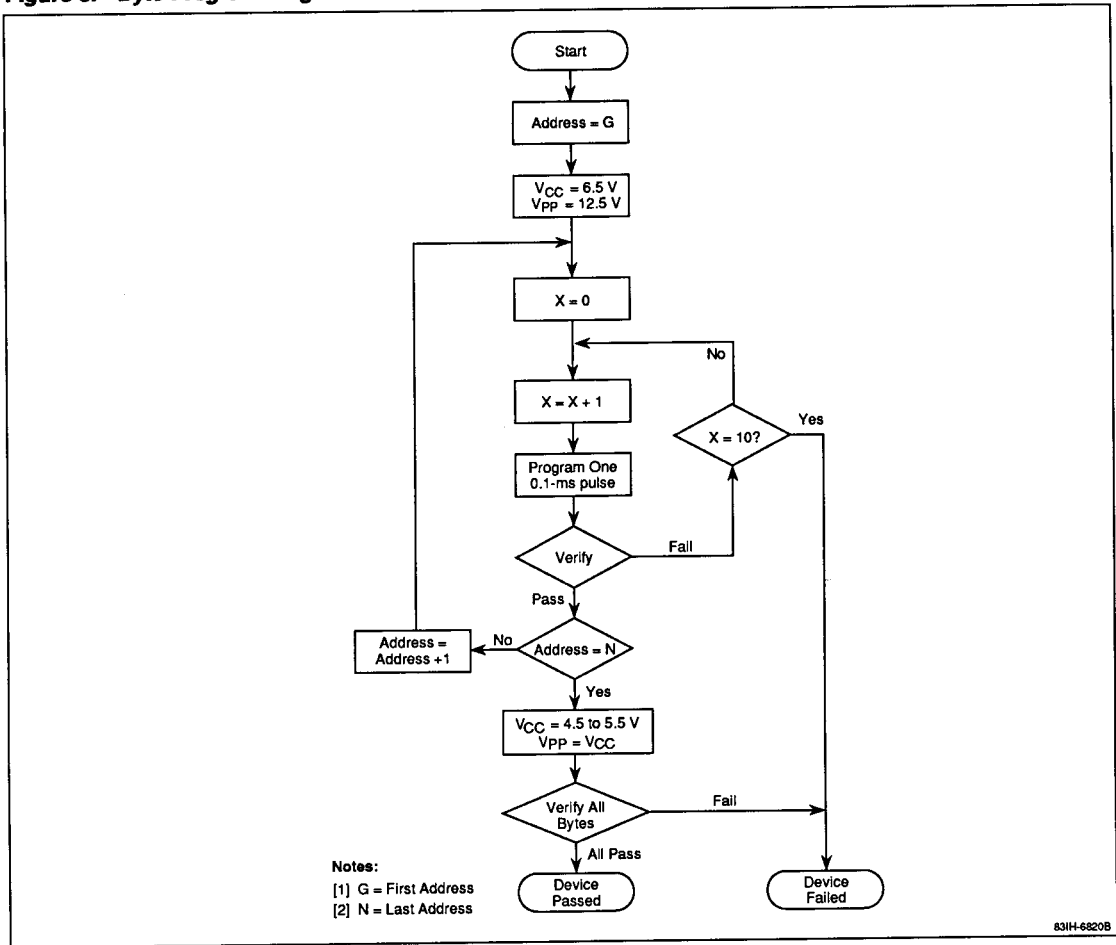


Figure 3. Byte Programming Flowchart



Timing Waveforms

Read Cycle

