

**NEC**

ELECTRONICS

DATA SHEET

**MOS INTEGRATED CIRCUIT** **$\mu$ PD3593****2 048-BIT CCD LINEAR IMAGE SENSOR WITH PERIPHERAL CIRCUITS**

The  $\mu$ PD3593 is a 2048-bit high sensitivity CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal.

The  $\mu$ PD3593 has an output amplifier which has wide output range, and which can switch gain. Therefore easy to get signal level which is easy to process from low illumination to high illumination, and it is easy to apply to many purposes.

With internal generation circuit of driving signal and internal driver, the  $\mu$ PD3593 performs only with two basic clock inputs. No special driving circuit is required. In addition, analog signal processor convert and output independent CCD register in every bit to continuous video signal. So it is easy to interface to A/D converter or Bi-level converter.

**FEATURES**

- Valid photocell 2 048-bit
- Photocell's pitch 14  $\mu$ m
- CCD output 4 steps selectable gain (2, 4, 8, 16 times)
- Peak response wavelength 550 nm (green)
- Resolution 8 dot/mm across the shorter side of a B4-size (257 x 364 mm) sheet
- Power supply +12 V, +5 V
- Drive clock level CMOS 5 V clock input x 2
- High speed scan 1 ms/line
- Built-in circuit
  - Timing generator
  - CCD clock driver
  - Optical black clamp circuit
  - Sample and hold circuit
  - 4-step variable gain amplifier

**ORDERING INFORMATION**

Part Number	Package	Quality Grade
$\mu$ PD3593D	22-pin ceramic DIP (CERDIP) (400 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

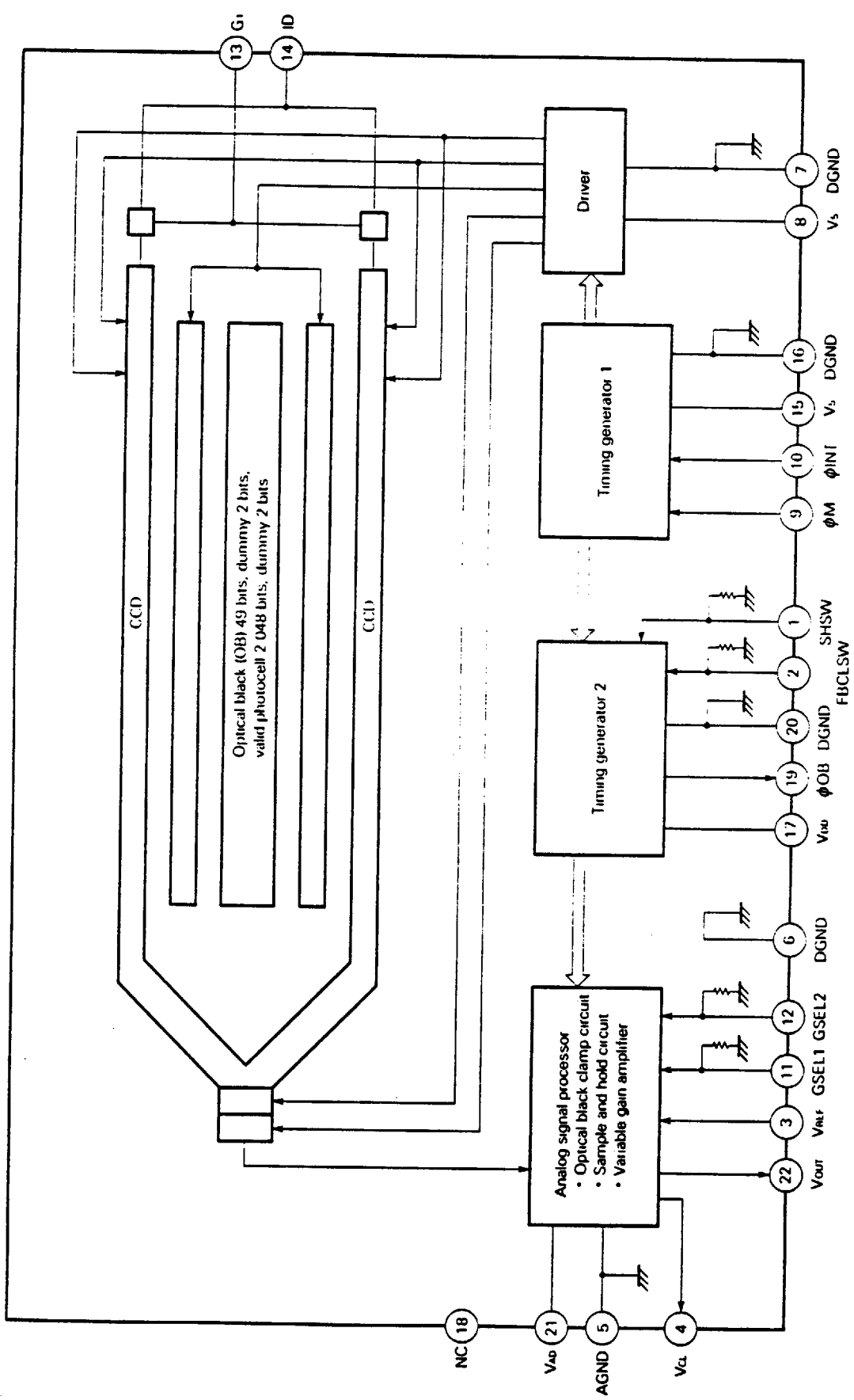
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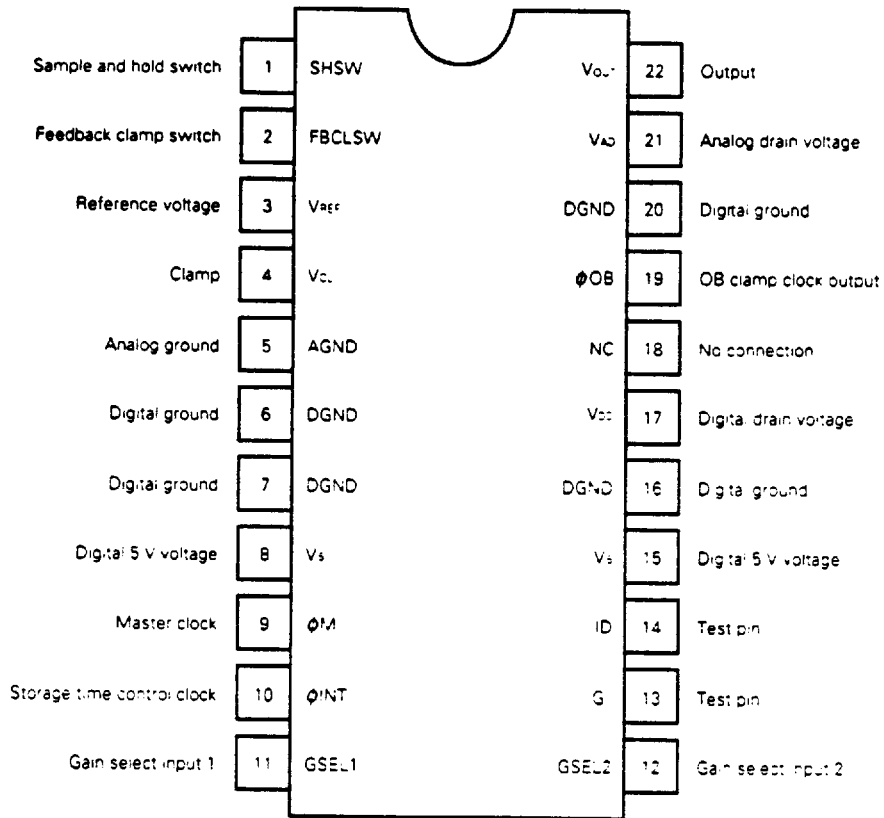
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2 BLOCK DIAGRAM



**PIN CONFIGURATION (Top View)**



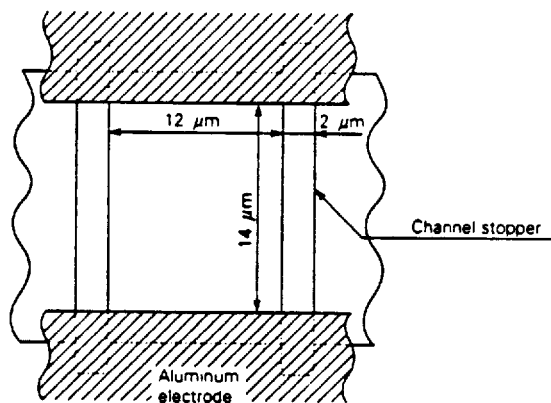
Function of SHSW pin

SHSW	Sample and hold circuit
V <sub>s</sub>	Stop
0 V	Operate

Function of FBCLSW pin

FBCLSW	Feedback clamp circuit
V <sub>s</sub>	Stop
0 V	Operate

**PHOTOCELL STRUCTURE DIAGRAM**



**PIN FUNCTIONS**

Pin No.	Symbol	Functions
1	SHSW	Internal sample and hold enable pin. Low level input: Internal sample and hold circuit operates. High level input: Internal sample and hold circuit stops and signal from CCD is output just as it is. This pin is connected internally to pull-down resistor (refer to electrical characteristics to obtain pull-down resistance). Therefore, when internal sample and hold circuit is used, this pin can be left unconnected.
2	FBCLSW	Internal optical black clamp enable pin. Low level input: Internal optical black clamp circuit operates. High level input: Internal optical black clamp circuit stops. This pin is connected internally to pull-down resistor (refer to electrical characteristics to obtain pull-down resistance). Therefore, when internal optical black clamp circuit is used, this pin can be left unconnected.
<p>Optical black clamp equivalent circuit</p>		
<p>Connecting external capacitor to V<sub>cl</sub> (pin 4), fix hold time according to the charge time.</p>		
3	V <sub>REF</sub>	Reference voltage input pin for internal optical black clamp circuit.
4	V <sub>cl</sub>	Connected to capacitor which sets hold time constant for internal optical black clamp circuit. Leak path resistance of internal capacitor (about 250 pF) will be 2 or 3 MΩ, therefore, when charge time is needed more than 1 ms, use external capacitor. When optical black clamp level precision is needed, this pin is input pin of feed back signal from external high precision comparator. Refer to parameter of clamp error in electrical characteristics to obtain dispersion of clamp level when internal comparator is used.
5	AGND	Ground pin for analog signal processing unit (optical black clamp circuit, sample and hold circuit).
6	DGND	Ground pin for digital circuits (timing generator unit).
7	DGND	Ground pin for digital circuits (driver unit).
8	V <sub>s</sub>	+5 V power supply pin for digital circuits.

Pin No.	Symbol	Functions															
9	$\phi M$	Master clock input pin. Data rate is 1/2 of master clock frequency.															
10	$\phi INT$	Control clock input pin to set charge time. By inputting this signal, optical black signal is output from 26 clock pulses after $\phi M$ (Refer to timing chart to obtain detailed timing).															
11 12	GSEL1 GSEL2	By combining these 2 pins, output amplifier circuit gain can be selected.															
<table border="1"> <thead> <tr> <th>GSEL1</th> <th>GSEL2</th> <th>output amplifier circuit gain</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>2 times</td> </tr> <tr> <td>L</td> <td>H</td> <td>4 times</td> </tr> <tr> <td>H</td> <td>L</td> <td>8 times</td> </tr> <tr> <td>H</td> <td>H</td> <td>16 times</td> </tr> </tbody> </table>			GSEL1	GSEL2	output amplifier circuit gain	L	L	2 times	L	H	4 times	H	L	8 times	H	H	16 times
GSEL1	GSEL2	output amplifier circuit gain															
L	L	2 times															
L	H	4 times															
H	L	8 times															
H	H	16 times															
<p>These pins are connected internally to pull-down resistor (refer to electrical characteristics to obtain pull-down resistance). Therefore, when using at input low level, this pin can be left unconnected.</p>																	
13	G <sub>1</sub>	Test pin. Connect to digital ground.															
14	ID	Test pin. Connect to +5 V power supply.															
15	V <sub>s</sub>	+5 V power supply pin for digital circuit.															
16	DGND	Ground pin for digital circuit (timing generator unit).															
17	V <sub>DD</sub>	+12 V power supply pin for digital circuit.															
18	NC	Non connect pin. Leave this pin unconnected or connect to digital GND.															
19	$\phi OB$	Output pin for optical black clamp pulse. CMOS output under 5 V operation.															
20	DGND	Ground pin for digital circuit (timing generator unit).															
21	V <sub>AD</sub>	+12 V power supply pin for analog circuit.															
22	V <sub>out</sub>	Output pin. Refer to timing chart to obtain detailed output timing.															

ABSOLUTE MAXIMUM RATINGS ( $T_a = +25\text{ }^\circ\text{C}$ )

Parameter	Symbol	Ratings	Unit
Analog drain voltage	$V_{AD}$	-0.3 ~ +15	V
Digital drain voltage	$V_{DD}$	-0.3 ~ +15	V
Test pin ID voltage	$V_{ID}$	-0.3 ~ +15	V
Digital 5 V voltage	$V_s$	-0.3 ~ +7	V
Reference voltage	$V_{REF}$	-0.3 ~ +7	V
Clamp pin input voltage	$V_{CL}$	-0.3 ~ +7	V
Sample and hold switch	$V_{SHSW}$	$V_s$	V
Feedback clamp switch	$V_{FBCLSW}$	$V_s$	V
Master clock voltage	$V_{OM}$	$V_s$	V
Storage time control clock voltage	$V_{OINT}$	$V_s$	V
Gain select input voltage 1	$V_{GSEL1}$	$V_s$	V
Gain select input voltage 2	$V_{GSEL2}$	$V_s$	V
Operating ambient temperature	$T_{OPT}$	-25 ~ +60	$^\circ\text{C}$
Storage temperature	$T_{STG}$	-40 ~ +100	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ( $T_a = -25$  to  $+60\text{ }^\circ\text{C}$ )

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Analog drain voltage	$V_{AD}$	11.4	12.0	12.6	V
Digital drain voltage	$V_{DD}$	11.4	12.0	12.6	V
Test pin ID voltage	$V_{ID}$	11.4	12.0	12.6	V
Digital 5 V voltage	$V_s$	4.5	5.0	5.5	V
Reference voltage	$V_{REF}$	4.0	4.5	5.0	V
Master clock $\phi M$ signal high level	$V_{OMH}$	4.5	$V_s$	$V_s$	V
Master clock $\phi M$ signal low level	$V_{OML}$	-0.3	0	0.5	V
Storage time control clock $\phi INT$ signal high level	$V_{OINTH}$	4.5	$V_s$	$V_s$	V
Storage time control clock $\phi INT$ signal low level	$V_{OINTL}$	-0.3	0	0.5	V
Gain select input voltage GSEL 1,2 signal high level	$V_{GSELH}$	4.5	$V_s$	$V_s$	V
Gain select input voltage GSEL 1,2 signal low level (Note 1)	$V_{GSELL}$	-0.3	0	0.5	V
Sample and hold switch SHSW signal high level	$V_{SHH}$	4.5	$V_s$	$V_s$	V
Sample and hold switch SHSW signal low level (Note 1)	$V_{SHL}$	-0.3	0	0.5	V
Feedback clamp switch FBCLSW signal high level	$V_{FBCLH}$	4.5	$V_s$	$V_s$	V
Feedback clamp switch FBCLSW signal low level (Note 1)	$V_{FBCLL}$	-0.3	0	0.5	V
Hold capacitor (Note 2)	$C_{CL}$	—	0.001	0.01	$\mu\text{F}$
Master clock $\phi M$ frequency	$f_{OM}$	0.5	2	4	MHz

Note 1. Gain select pin (GSEL 1, 2), sample and hold switch pin (SHSW), feedback clamp switch pin (FBCLSW) are pull down to GND internally with 50 k $\Omega$  ~ 200 k $\Omega$  resistor.

2. Control voltage hold capacitor depending on storage time ( $T_{INT}$ ).

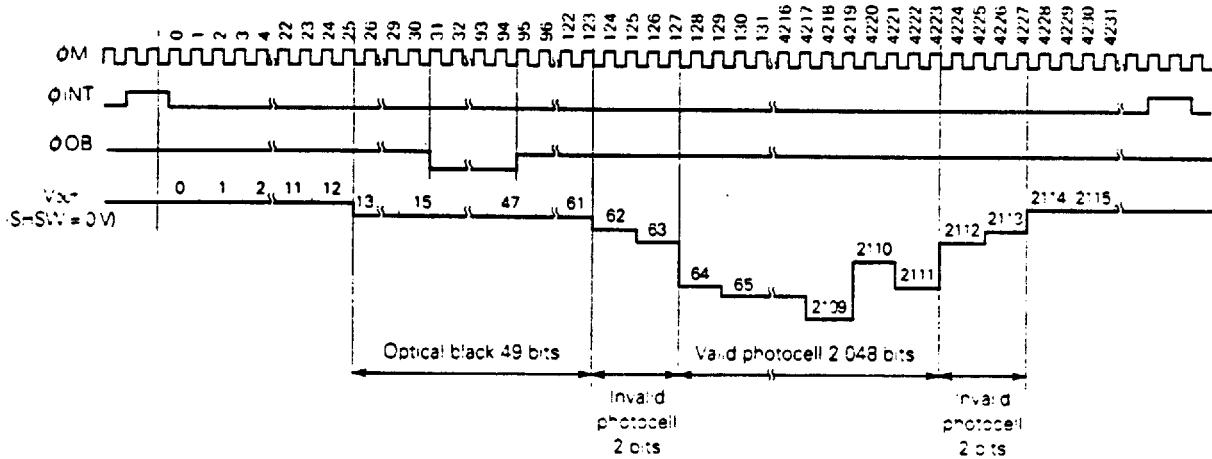
## ELECTRICAL CHARACTERISTICS

$T_a = +25\text{ }^\circ\text{C}$ ,  $V_{AD} = V_{DD} = 12\text{ V}$ ,  $V_s = 5\text{ V}$ ,  $f_{PM} = 2\text{ MHz}$ , data rate = 1 MHz, storage time = 10ms  
input signal clock = 5 V<sub>PP</sub>,  $V_{REF} = 4.5\text{ V}$ , light source = 3200 K halogen lamp + C500 (infrared cut filter)

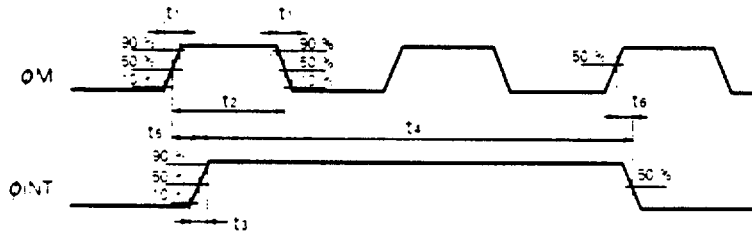
Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit	Built-in amplifier gain
			GSEL1	GSEL2					
Saturation voltage	$V_{SAT}$	Daylight color fluorescent lamp	—	—	2	3	—	V	
Saturation exposure	SE	Daylight color fluorescent lamp	0	0	—	0.114	—	lx·s	x2
			0	1	—	0.051	—		
			1	0	—	0.027	—		
			1	1	—	0.012	—		
Photo response non-uniformity	PRNU	$V_{OUT} = 500\text{ mV}$	0	0	—	$\pm 4$	$\pm 8$	%	x2
Average dark signal	ADS	$T_c = 25\text{ }^\circ\text{C}$ Note, $T_{INT} = 10\text{ ms}$ light shielding	0	0	—	1	5	mV	x2
			0	1	—	2	10		
			1	0	—	4	20		
			1	1	—	8	40		
Dark signal non-uniformity	DSNU	$T_c = 25\text{ }^\circ\text{C}$ Note, $T_{INT} = 10\text{ ms}$ light shielding	0	0	-5	$\pm 1$	+5	mV	x2
			0	1	-10	$\pm 2$	+10		
			1	0	-20	$\pm 4$	+20		
			1	1	-40	$\pm 8$	+40		
Power consumption	$P_w$	$V_{DD} = V_{DD} = 12\text{ V}$ $V_s = 5\text{ V}$ , $f_{OM} = 2\text{ MHz}$	0	0	150	230	350	mW	
			1	1	80	120	180		
Output impedance	$Z_o$		0	0	—	1	2	k $\Omega$	
Response	$R_f$	Daylight color fluorescent lamp	0	0	18.5	26.4	34.3	V <sub>ix</sub> ·s	x2
			0	1	—	59.4	—		
			1	0	—	110	—		
			1	1	—	248	—		
Response peak wavelength			—	—	—	550	—	nm	
Image lag	IL	$V_{OUT} = 1\text{ V}$	0	0	—	2	5	%	x2
Reference voltage input current	$I_{REF}$		0	0	—	0.001	0.1	mA	
Transfer efficiency	TTE	$V_{OUT} = 500\text{ mV}$	0	0	92	98	—	%	x2
Sample and hold noise	SHN	light shielding	0	0	—	15	30	mV	x2
Clamp error	$V_{ERR}$	light shielding $V_{REF} = 4.5\text{ V}$	0	0	-100	0	+100	mV	x2
Clock input capacitance Master clock input pin Storage time control clock input pin	$C_{\phi}$		—	—	—	5	10	pF	
Pull down resistor Gain select input pin Sample and hold switch pin Feedback clamp switch pin	$R_{PD}$	$V_{IN} = 5\text{ V}$	—	—	50	100	200	k $\Omega$	
Register imbalance	RI	$V_{OUT} = 500\text{ mV}$	0	0	—	—	3	%	x2
Dynamic range	DR	$V_{SAT}/DSNU$	0	0	—	3000	—	times	x2
			0	1	—	1500	—		
			1	0	—	750	—		
			1	1	—	375	—		

Note  $T_c$  = Case temperature

**TIMING CHART**



**Timing Chart for OM and QINT**



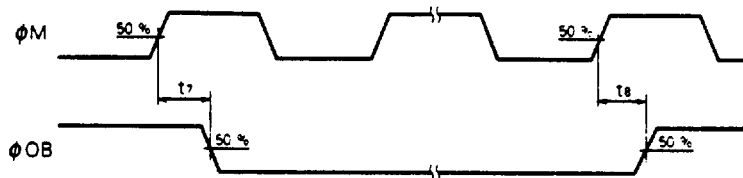
**Recommended Timing**

(Unit: ns)

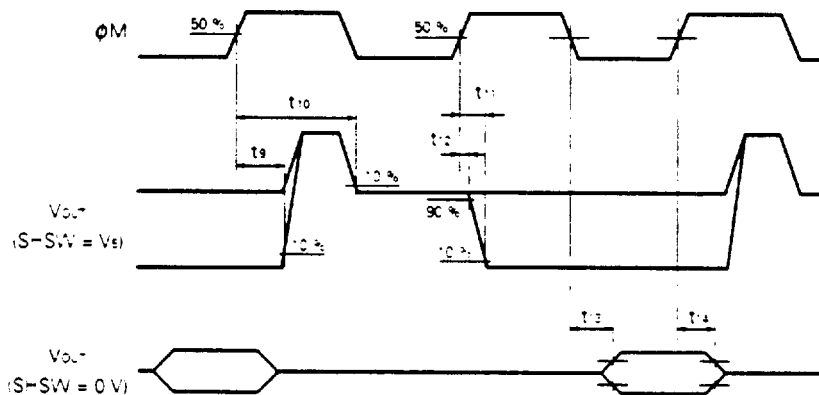
Parameter	MIN.	TYP.	MAX.
t1	0	20	100
t2	125	250	1000
t3	0	20	100
t4	—	4t2	—
t5	-30	0	t2
t6	-t2	0	t2



$\phi$ OB Signal Delay from  $\phi$ M



$V_{out}$  Signal Delay from  $\phi$ M



Signal Delay Time ( $V_{out} = 500$  mV, output amplifier gain:  $\times 2$ )

(Unit: ns)

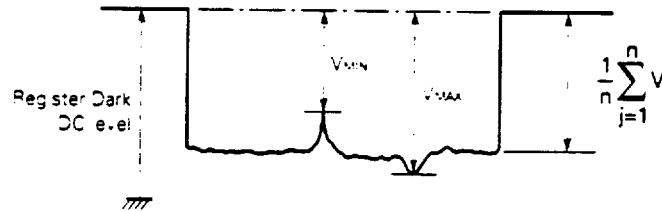
Parameter	MIN.	TYP.	MAX.
$t_7$	200	280	370
$t_8$	150	220	290
$t_9$	40	60	80
$t_{10}$	160	230	300
$t_{11}$	66	95	125
$t_{12}$	40	60	80
$t_{13}$		80	120
$t_{14}$		50	100

**DEFINITIONS OF CHARACTERISTIC ITEMS**

1. Saturation voltage:  $V_{SAT}$   
Output signal voltage at which the response linearity is lost.
2. Saturation exposure: SE  
Product of intensity of illumination ( $I_x$ ) and storage time ( $s$ ) when saturation of output voltage occurs.
3. Photo response non-uniformity: PRNU  
The peak/bottom ratio to the average output voltage of all the valid bits calculated by the following formula.

$$PRNU (\%) = \left[ \frac{V_{MAX. \text{ or } V_{MIN.}}}{\frac{1}{n} \sum_{j=1}^n V_j} - 1 \right] \times 100$$

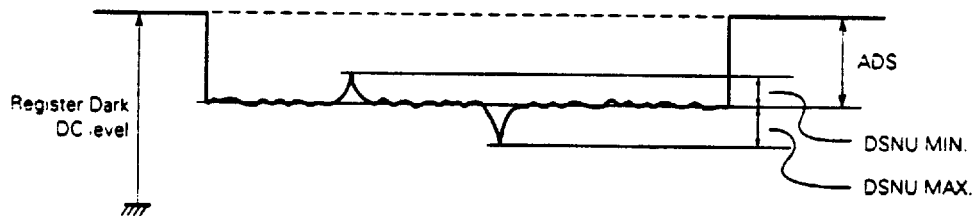
$n$  : Number of valid bits  
 $V_j$  : Output voltage of each bit



4. Average dark signal: ADS  
Output average voltage in light shielding

$$ADS(mV) = \frac{1}{n} \sum_{j=1}^n V_j$$

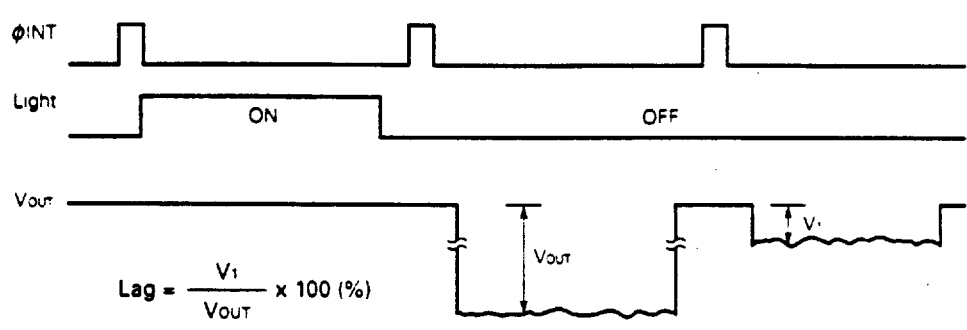
5. Dark signal non-uniformity: DSNU  
The difference between peak or bottom output voltage in light shielding and ADS.



6. Output impedance:  $Z_o$   
Output pin impedance viewed from outside.
7. Response: R  
Output voltage divided by exposure ( $I_x \cdot s$ ).  
Note that the response varies with the light source.

8. Image Lag: IL

The rate between the last output voltage and the next one after read out the data of a line.



9. Register Imbalance: RI

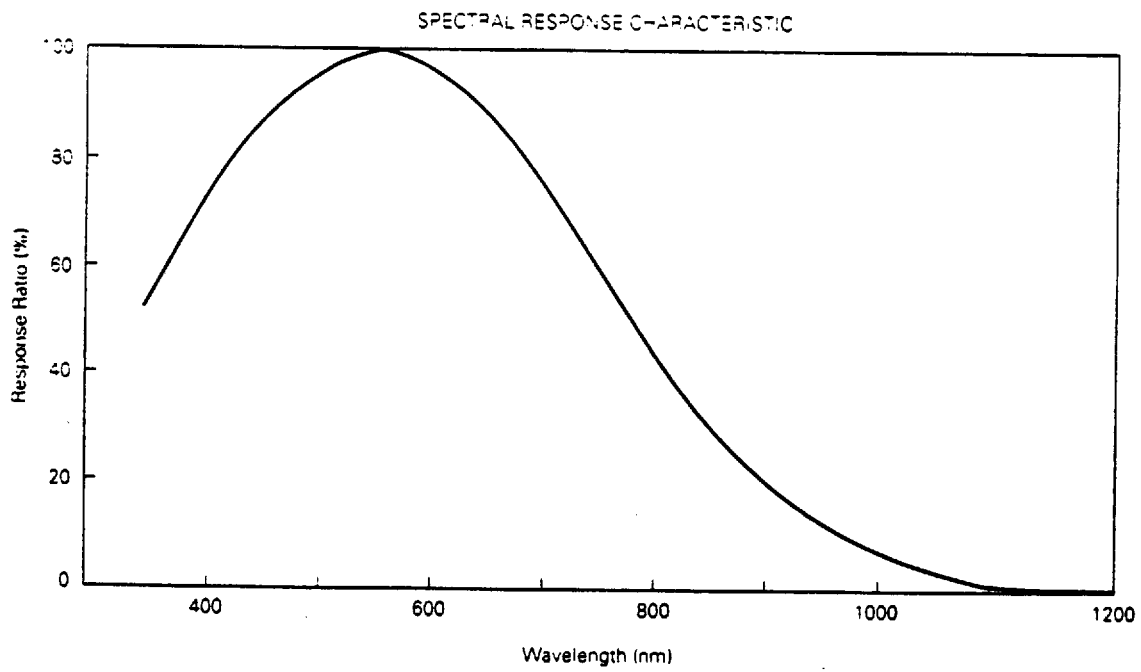
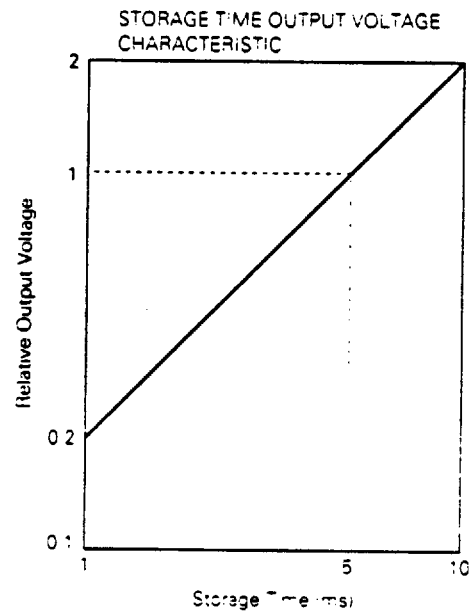
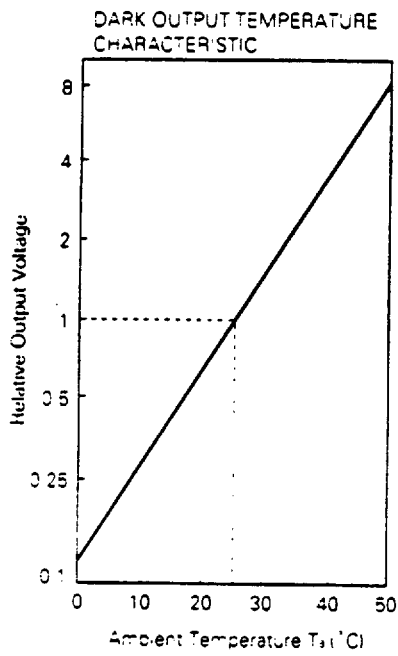
The rate of the average voltage which is the difference between the output voltage of Odd and Even bits, against the average output voltage of all the valid bits.

$$RI = \frac{\frac{1}{n} \sum_{j=1}^n |V_j - V_{j+1}|}{\frac{1}{n} \sum_{j=1}^n V_j} \times 100 (\%)$$

10. Clamp Error:  $V_{ERR}$

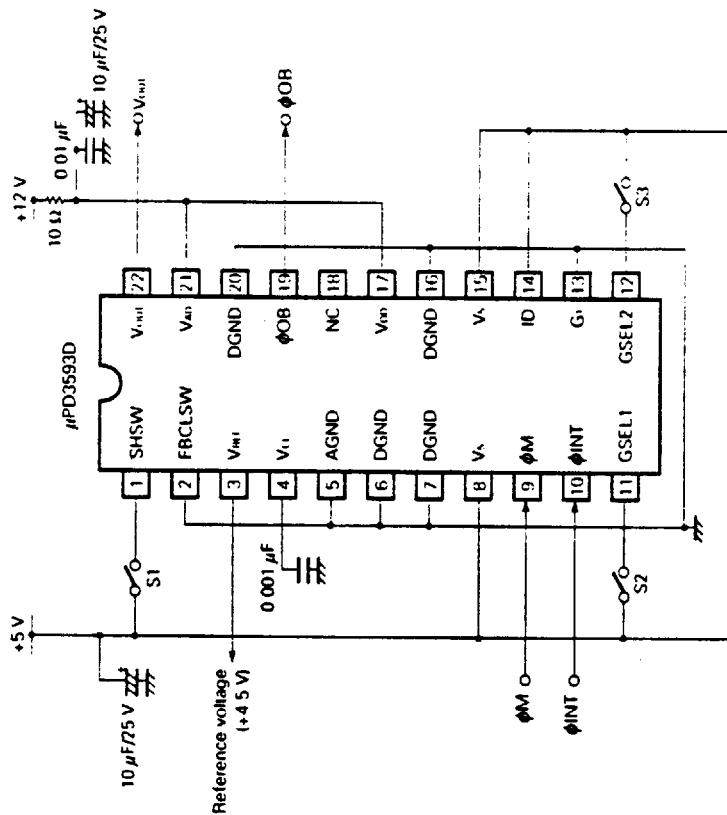
$V_{ERR} = OB \text{ unit offset voltage} - V_{REF}$

STANDARD CHARACTERISTIC CURVES (T<sub>a</sub> = 25 °C)

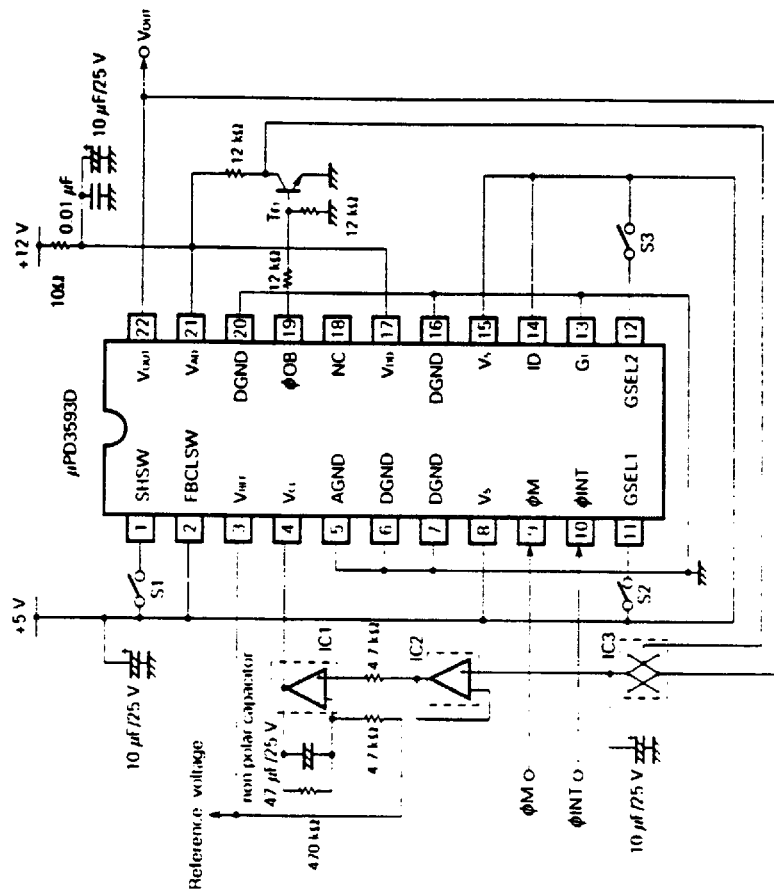


APPLICATION EXAMPLES

Example 1: With internal feedback clamp



Example 2: Without internal feedback clamp



S1: Sample and hold circuit use/unuse select switch

[OFF; Use ON; Unuse]

S2, S3: Output amplifier gain select switch

IC1, IC2: Low offset, low input current

IC3: µPD4066

Tr1: 2SC945

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

PACKAGE DIMENSIONS (Unit: mm)

