NEC

MOS INTEGRATED CIRCUIT

μPD3719

10600 PIXELS × 3 COLOR CCD LINEAR IMAGE SENSOR

The μPD3719 is a color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The μPD3719 has 3 rows of 10600 pixels, and each row has a single-sided readout type of charge transfer register. It has reset feed-through level clamp circuits and voltage amplifiers. Moreover, a large dynamic range is realized by using a large saturation voltage and a low-noise amplifier. Therefore, it is suitable for 1200 dpi/A4 professional color image scanners and so on.

FEATURES

- Valid photocell : 10600 pixels × 3
- Photocell's pitch : 7 μm
- Line spacing : 70 μm (10 lines) Red line-Green line, Green line-Blue line
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance 10^7 lx•hour)
- Resolution : 48 dot/mm A4 (210 × 297 mm) size (shorter side)
  1200 dpi US letter (8.5" × 11") size (shorter side)
- Drive clock level : CMOS output under 5 V operation
- Data rate : 2 MHz MAX.
- Power supply : +15 V
- On-chip circuits : Reset feed-through level clamp circuits
  Voltage amplifiers

ORDERING INFORMATION

Part Number	Package
μPD3719D	CCD linear image sensor 36-pin ceramic DIP (600 mil)

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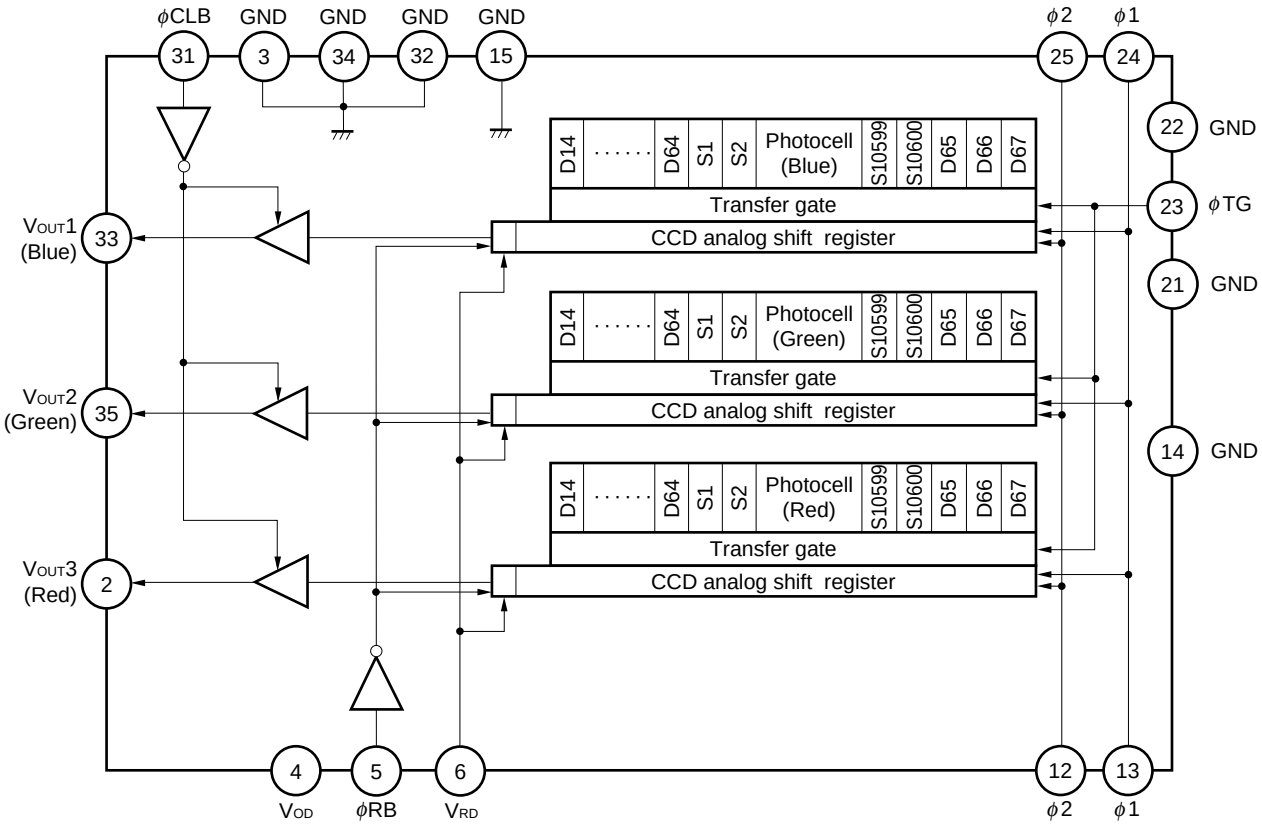
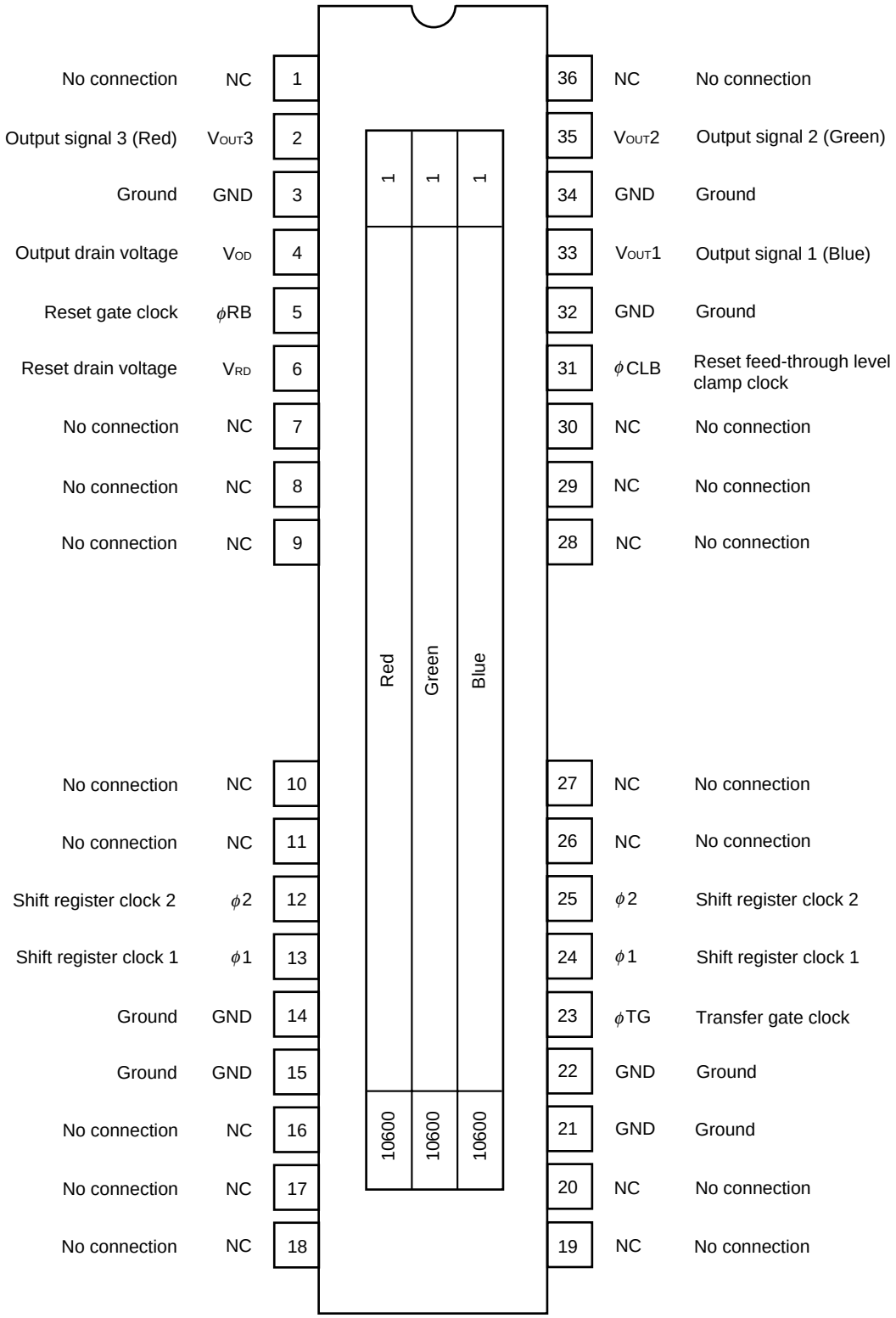
Printed in Japan

BLOCK DIAGRAM

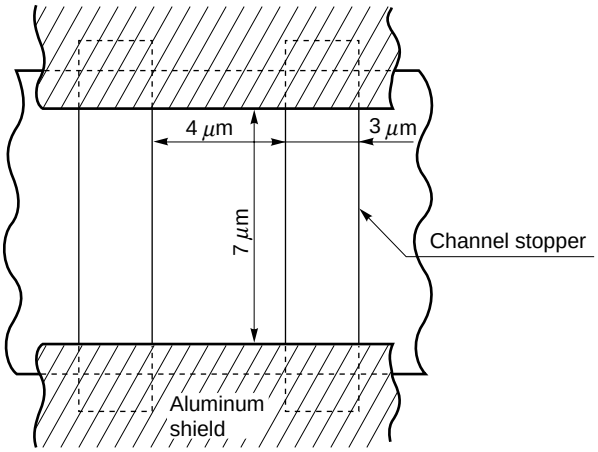


PIN CONFIGURATION (Top View)

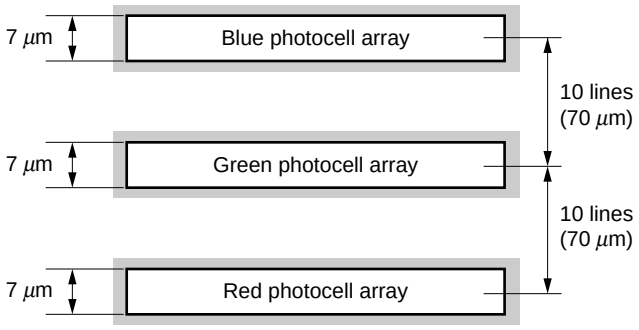
CCD linear image sensor 36-pin ceramic DIP (600 mil)



PHOTOCELL STRUCTURE DIAGRAM



PHOTOCELL ARRAY STRUCTURE DIAGRAM (Line spacing)



ABSOLUTE MAXIMUM RATINGS (T_A = +25 °C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	–0.3 to +16	V
Reset drain voltage	V_{RD}	–0.3 to +16	V
Shift register clock voltage	$V_{\phi1}$, $V_{\phi2}$	–0.3 to +8	V
Reset gate clock voltage	$V_{\phi RB}$	–0.3 to +8	V
Reset feed-through level clamp clock voltage	$V_{\phi CLB}$	–0.3 to +8	V
Transfer gate clock voltage	$V_{\phi TG}$	–0.3 to +8	V
Operating ambient temperature	T_A	–25 to +60	°C
Storage temperature	T_{stg}	–40 to +100	°C

Caution Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.

RECOMMENDED OPERATING CONDITIONS (T_A = +25 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output drain voltage	V_{OD}	14.0	15.0	16.0	V
Reset drain voltage	V_{RD}	14.0	V_{OD}	V_{OD}	V
Shift register clock high level	$V_{\phi1H}$, $V_{\phi2H}$	4.5	5.0	5.5	V
Shift register clock low level	$V_{\phi1L}$, $V_{\phi2L}$	–0.3	0	+0.5	V
Reset gate clock high level	$V_{\phi RBH}$	4.5	5.0	5.5	V
Reset gate clock low level	$V_{\phi RBL}$	–0.3	0	+0.5	V
Reset feed-through level clamp clock high level	$V_{\phi CLBH}$	4.5	5.0	5.5	V
Reset feed-through level clamp clock low level	$V_{\phi CLBL}$	–0.3	0	+0.5	V
Transfer gate clock high level	$V_{\phi TGH}$	4.5	$V_{\phi1H}$ **Note**	$V_{\phi1H}$ **Note**	V
Transfer gate clock low level	$V_{\phi TGL}$	–0.3	0	+0.3	V
Data rate	$f_{\phi RB}$	–	1	2	MHz

Note When Transfer gate clock high level ($V_{\phi TGH}$) is higher than Shift register clock high level ($V_{\phi1H}$), Image lag can increase.

ELECTRICAL CHARACTERISTICS

(T_A = +25 °C, V_{OD} = 15 V, V_{RD} = 15 V, data rate ($f_{\phi RB}$) = 2 MHz, storage time = 5.5 ms, light source: 3200 K halogen lamp +C-500S (infrared cut filter, t = 1mm), input signal clock = 5 V_{p-p})

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage		V_{sat}		4.0	5.0	–	V
Saturation exposure	Red	SER			0.52		lx•s
	Green	SEG			0.57		lx•s
	Blue	SEB			0.94		lx•s
Photo response non-uniformity		PRNU	V_{OUT} = 2.5 V		6	20	%
Average dark signal		ADS	Light shielding		0.8	3.0	mV
Dark signal non-uniformity		DSNU	Light shielding		1.5	5.0	mV
Power consumption		P_W			400	600	mW
Output impedance		Z_O			0.5	1	kΩ
Response	Red	R_R		6.8	9.7	12.6	V/lx•s
	Green	R_G		6.2	8.8	11.4	V/lx•s
	Blue	R_B		3.8	5.3	6.8	V/lx•s
Image lag		IL	V_{OUT} = 2.5 V		2.0	5.0	%
Offset level **Note1**		V_{OS}		8.8	10.8	12.8	V
Output fall delay time **Note2**		t_d	V_{OUT} = 2.5 V		70		ns
Total transfer efficiency		TTE	V_{OUT} = 2.5 V	92	98		%
Response peak	Red				630		nm
	Green				540		nm
	Blue				460		nm
Dynamic range		DR1	V_{sat} /DSNU		3333		times
		DR2	V_{sat} /σ		10000		times
Reset feed-through noise **Note1**		RFTN	Light shielding	0	1500	2500	mV
Random noise		σ	Light shielding	–	0.5	–	mV

Notes 1. Refer to **TIMING CHART 2**.

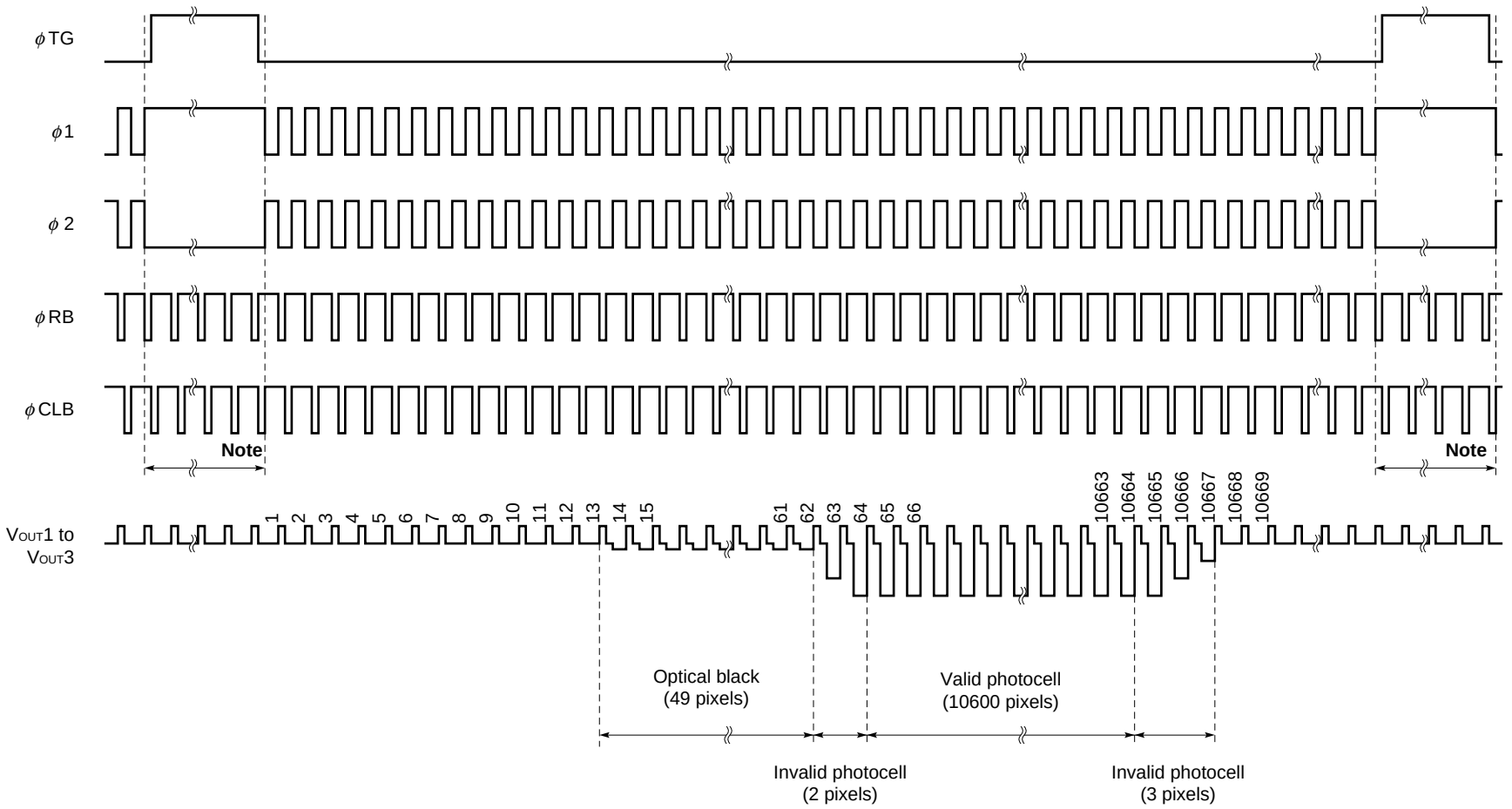
2. When the fall time of ϕ1 (t1) is the TYP. value (refer to **TIMING CHART 2**).

INPUT PIN CAPACITANCE (T_A = +25 °C, V_{OD} = V_{RD} = 15 V)

Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1}$	ϕ1	13		1600		pF
			24		1600		pF
Shift register clock pin capacitance 2	$C_{\phi 2}$	ϕ2	12		1600		pF
			25		1600		pF
Reset gate clock pin capacitance	$C_{\phi RB}$	ϕRB	5		15		pF
Reset feed-through level clamp clock pin capacitance	$C_{\phi CLB}$	ϕCLB	31		15		pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	ϕTG	23		200		pF

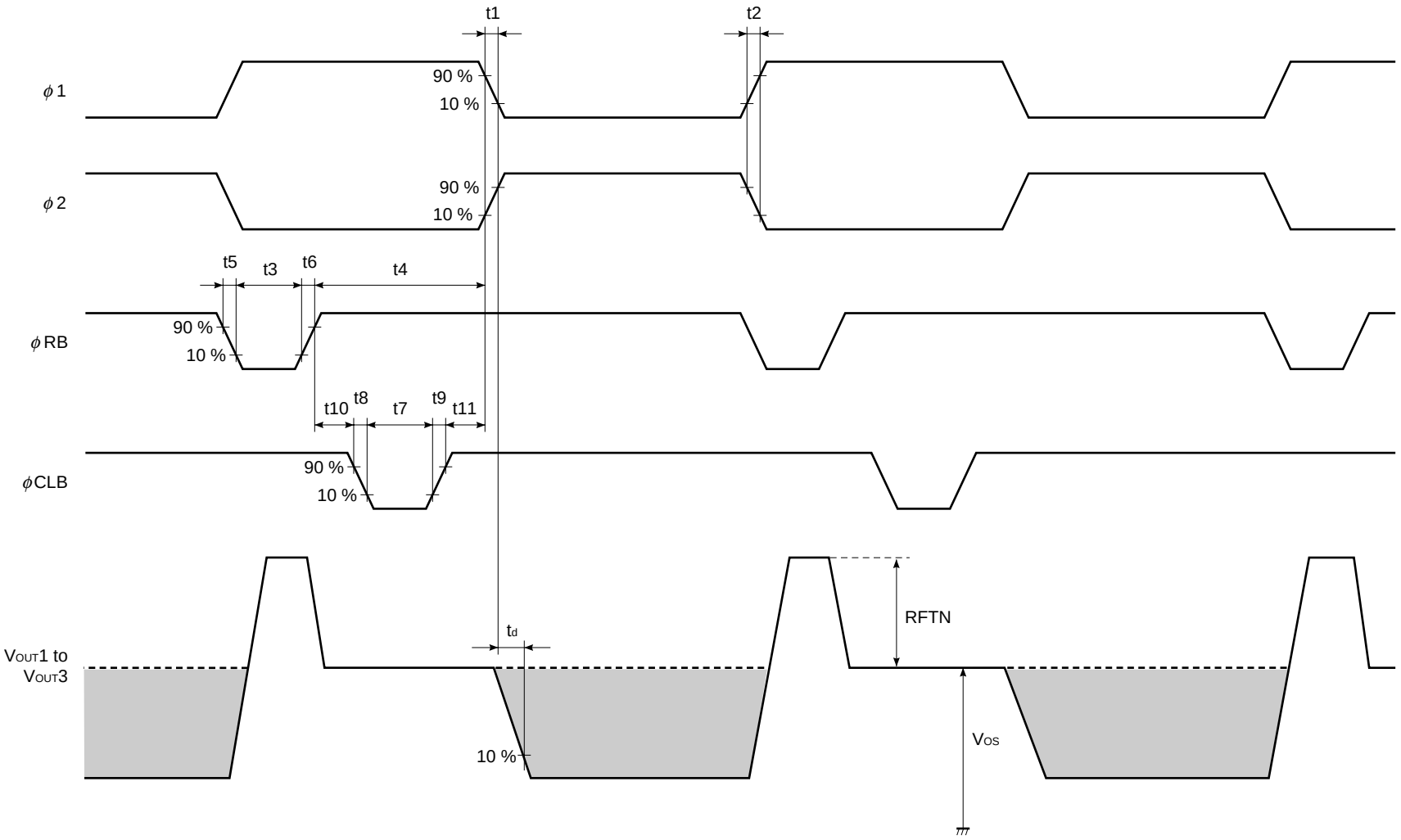
Remark Pins 13 and 24 (ϕ1), 12 and 25 (ϕ2) are each connected inside of the device.

TIMING CHART 1 (for each color)

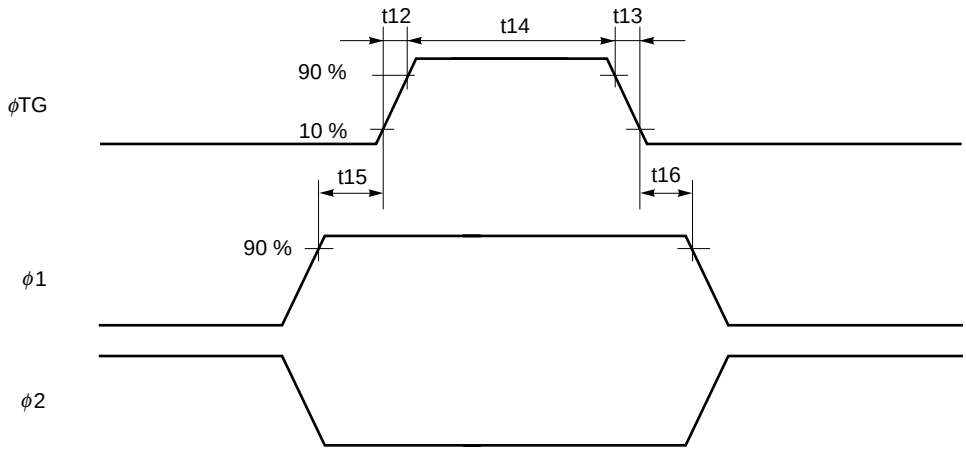


Note Input the φRB and φCLB pulses continuously during this period, too.

TIMING CHART 2 (for each color)



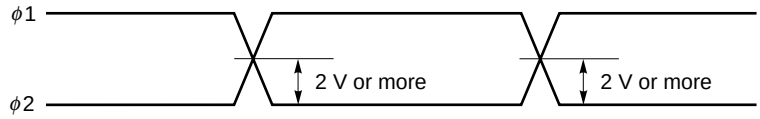
φTG, φ1, φ2 TIMING CHART



Symbol	MIN.	TYP.	MAX.	Unit
t1, t2	0	25	—	ns
t3	30	50	—	ns
t4	70	150	—	ns
t5, t6	0	25	—	ns
t7	30	75	—	ns
t8, t9	0	25	—	ns
t10	10	20	—	ns
t11	5	10	—	ns
t12, t13	0	50	—	ns
t14	3000	10000	—	ns
t15, t16	900	1000	—	ns

Remark TYP. is an example of at 1 MHz data rate ($f_{\phi RB}$) operation.

φ1, φ2 cross points



Remark Adjust cross points of φ1 and φ2 with input resistance of each pin.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage: V_{sat}
   Output signal voltage at which the response linearity is lost.

2. Saturation exposure: SE
   Product of intensity of illumination (I_X) and storage time (s) when saturation of output voltage occurs.

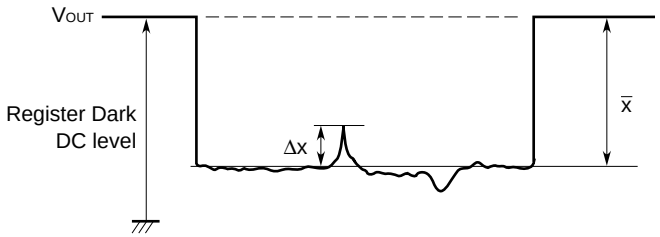
3. Photo response non-uniformity: PRNU
   The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$PRNU\ (\%) = \frac{\Delta x}{\overline{x}} \times 100$$

Δx : maximum of $|x_j - \overline{x}|$

$$\overline{x} = \frac{\sum_{j=1}^{10600} x_j}{10600}$$

x_j : Output voltage of valid pixel number j



4. Average dark signal: ADS
   Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

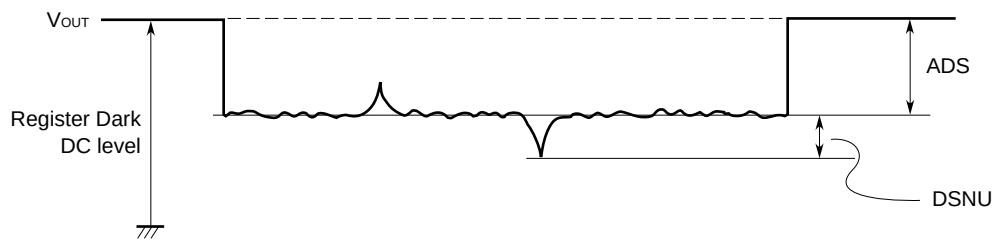
$$ADS\ (mV) = \frac{\sum_{j=1}^{10600} d_j}{10600}$$

d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity: DSNU
   Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

$$DSNU\ (mV) : \text{maximum of } |d_j - ADS|_{j = 1 \text{ to } 10600}$$

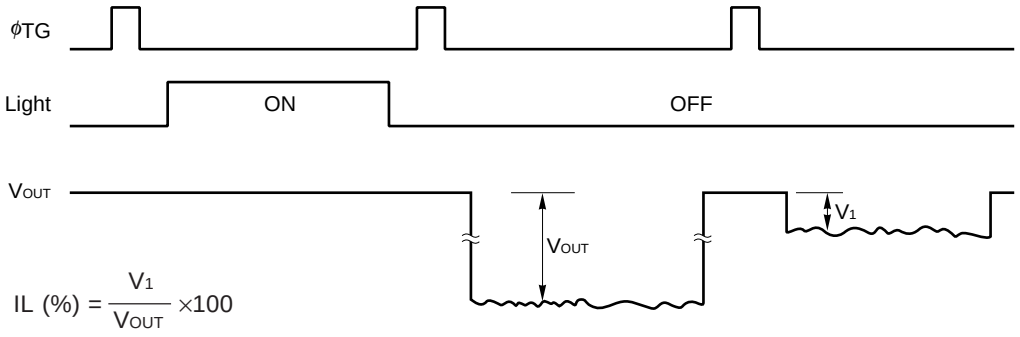
d_j : Dark signal of valid pixel number j



6. Output impedance: Z_O
   Impedance of the output pins viewed from outside.

7. Response: R
   Output voltage divided by exposure (Ix•s).
   Note that the response varies with a light source (spectral characteristic).

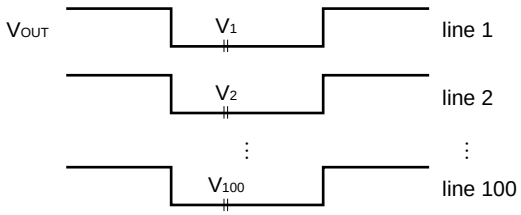
8. Image Lag: IL
   The rate between the last output voltage and the next one after read out the data of a line.



9. Random noise: σ
   Random noise σ is defined as the standard deviation of a valid pixel output signal with 100 times (=100 lines) data sampling at dark (light shielding).

$$\sigma\,(mV) = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \overline{V})^2}{100}} \quad , \quad \overline{V} = \frac{1}{100}\sum_{i=1}^{100} V_i$$

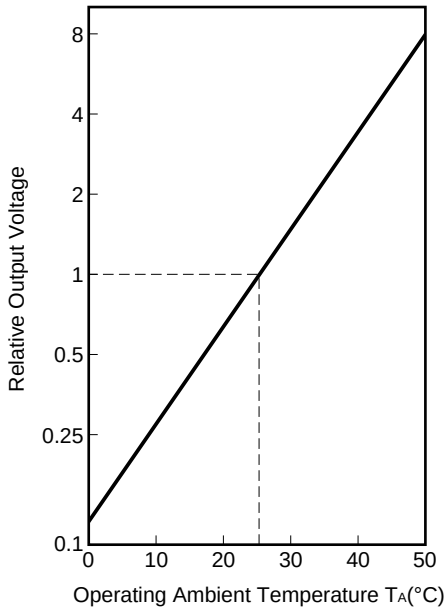
V_i: A valid pixel output signal among all of the valid pixels for each color



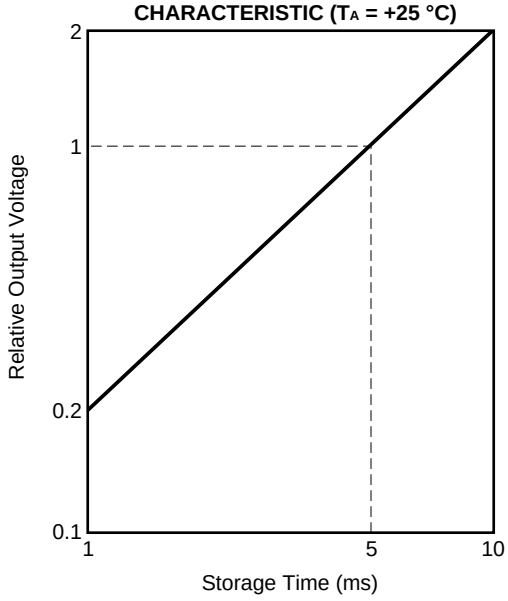
This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

STANDARD CHARACTERISTIC CURVES

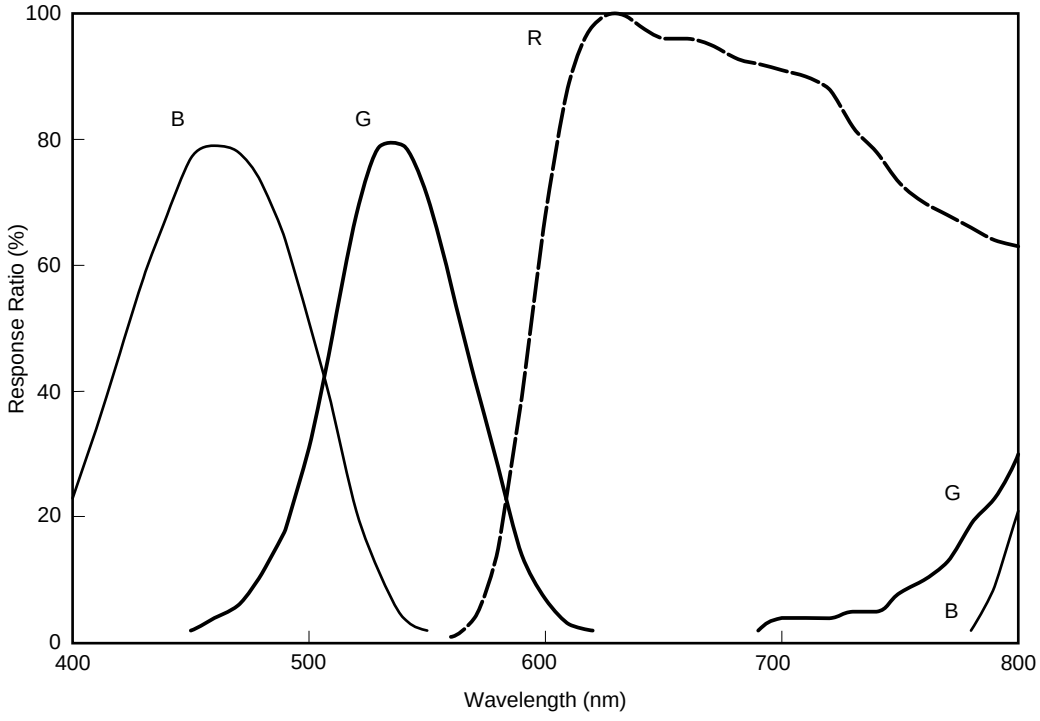
DARK OUTPUT TEMPERATURE CHARACTERISTIC



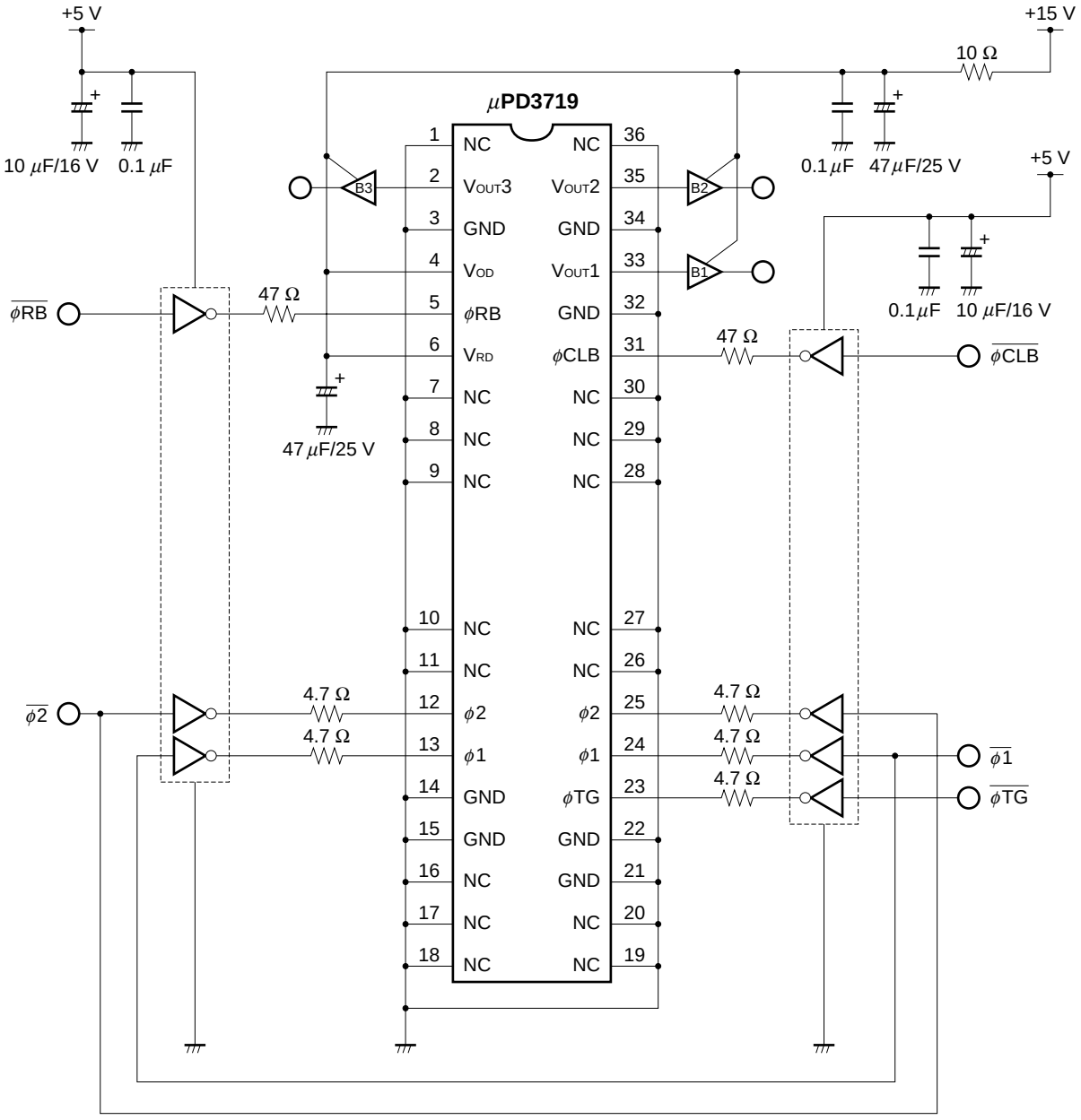
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC (T_A = +25 °C)



TOTAL SPECTRAL RESPONSE CHARACTERISTICS (without infrared cut filter) (T_A = +25 °C)

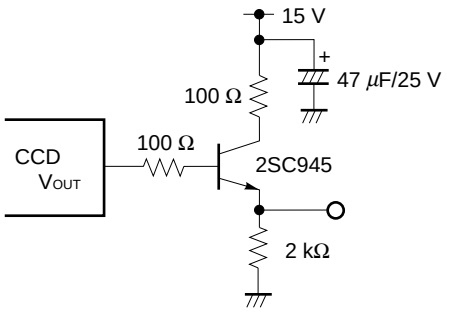


APPLICATION CIRCUIT EXAMPLE



Remark The inverters shown in the above application circuit example are the 74HC04.

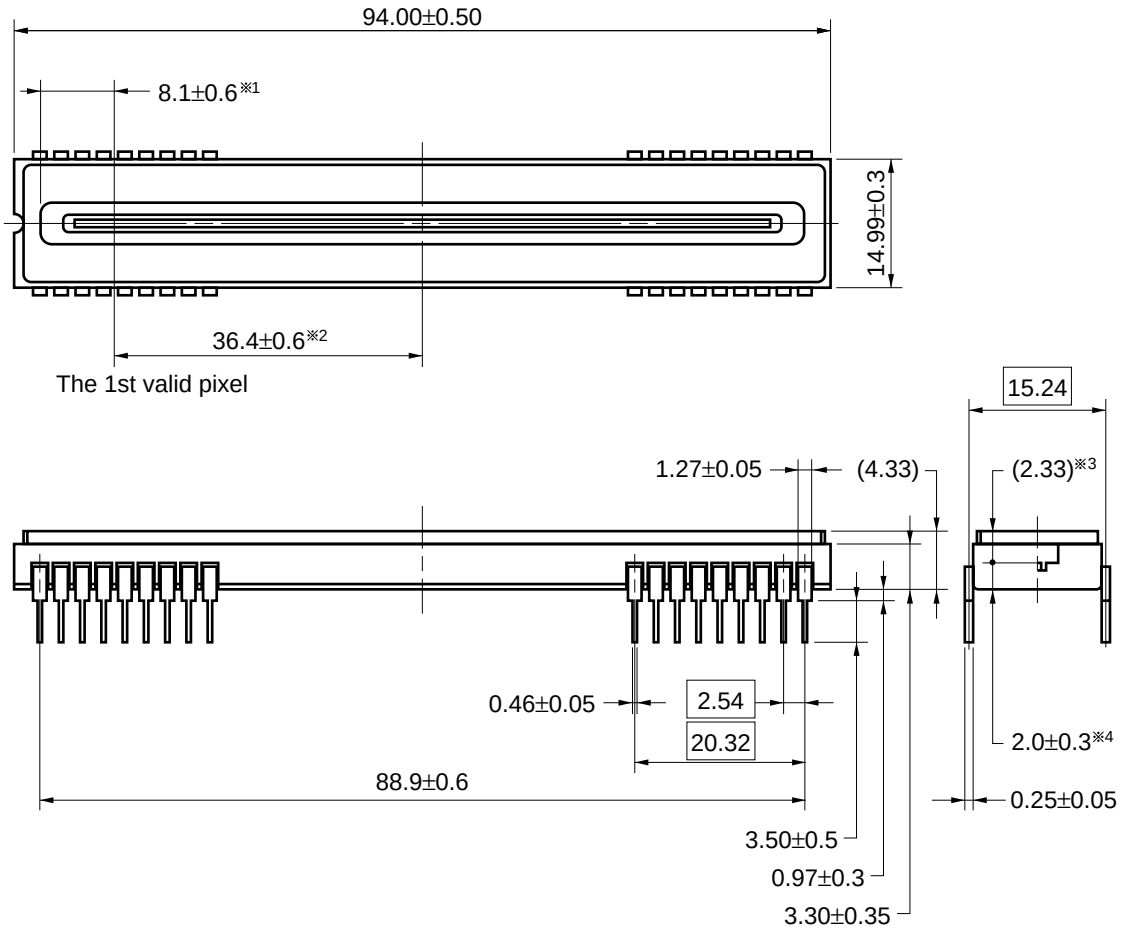
B1 to B3 EQUIVALENT CIRCUIT



PACKAGE DRAWING

CCD LINEAR IMAGE SENSOR 36-PIN CERAMIC DIP (600mil)

(Unit : mm)



Name	Dimensions	Refractive index
Glass cap	93.0 × 13.6 × 1.0	1.5

※1 The 1st valid pixel ⟷ The center of the pin1
※2 The 1st valid pixel ⟷ The center of the package
※3 The surface of the chip ⟷ The top of the glass cap (Reference)
※4 The bottom of the package ⟷ The surface of the chip

36D-1CCD-PKG-1

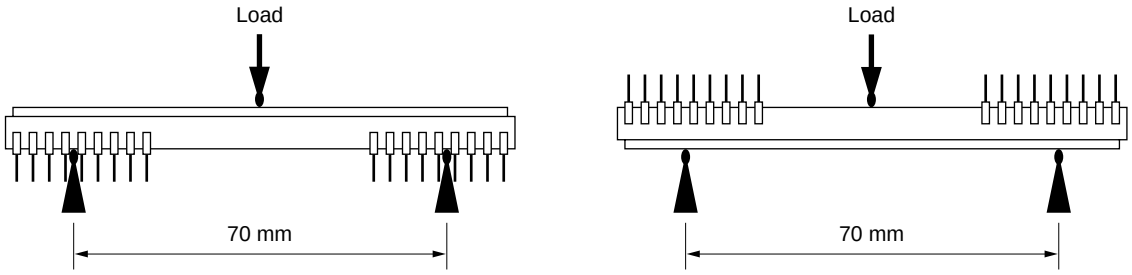
NOTES ON THE USE OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board.

When mounting the package, use a circuit board which will not subject the package to bending stress, or use a socket.

For this product, the reference value for the three-point bending strength[Note] is 30 kg. Avoid imposing a load, however, on the inside portion as viewed from the face on which the window (glass) is bonded to the package body (ceramic).

Note Three-point bending strength test
Distance between supports: 70 mm, Support R: R 2 mm, Loading rate: 0.5 mm / min.



[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

M4 96.5