NEC

MOS INTEGRATED CIRCUIT

μPD3739

5000 PIXELS CCD LINEAR IMAGE SENSOR

The μPD3739 is a CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal.

The μPD3739 is a 2-output type CCD sensor with 2 rows of high-speed charge transfer register, which transfers the photo signal electrons of 5000 pixels separately in odd and even pixels. It is developed as the higher sensitivity version of the previous device, the μPD35H71A. It is suitable for 400 dpi/A3 high-speed digital copiers, OCRs and high-end business facsimiles.

FEATURES

- Valid photocell : 5000 pixels
- Photocell's pitch : 7 μm
- High sensitivity : 9.0 V/lx·s TYP. (Light source: Daylight color fluorescent lamp)
- Low image lag : 1 % MAX.
- Peak response wavelength : 550 nm (green)
- Resolution : 16 dot/mm (400 dpi) A3 (297 × 420 mm) size (shorter side)
- Data rate : 40 MHz MAX. (20 MHz/1 output)
- Output type : 2 outputs out of phase (2 outputs in phase also supported)
- Power supply : +12 V
- Drive clock level : CMOS output under 5 V operation
- On-chip circuit : Automatic φR level adjuster
- Pin assign : Functional compatible with the μPD35H71A

ORDERING INFORMATION

Part Number	Package
μPD3739D	CCD linear image sensor 22-pin ceramic DIP (CERDIP) (400 mil)

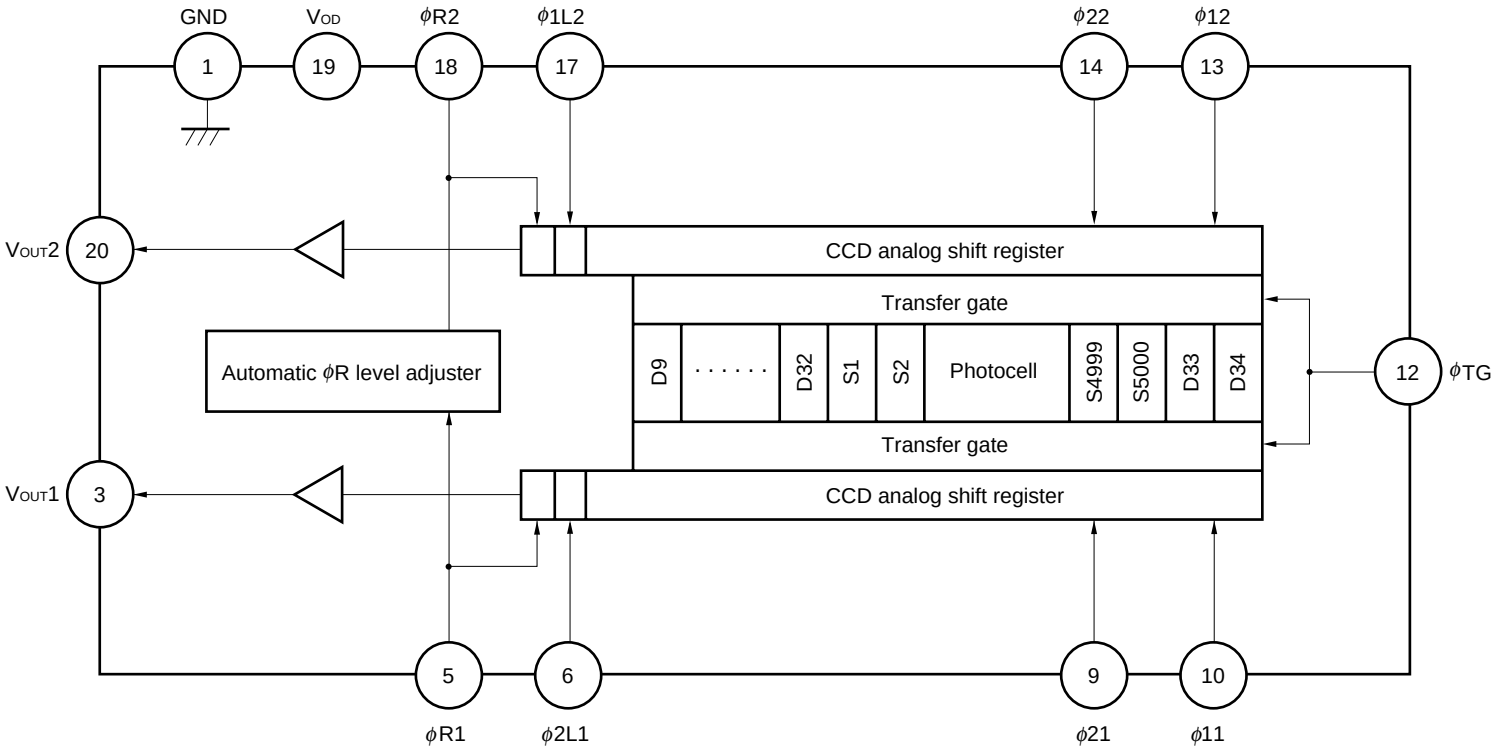
Document No. S12744EJ1V0DS00 (1st edition)
Date Published September 1997 N
Printed in Japan

COMPARISON CHART

Item			μPD3739	μPD35H71A
PIN CONFIGURATION	Pin 1		GND	DGND
	Pin 2		NC	TEST
	Pin 4		NC	V_{DD}
	Pin 11		NC	V_{SUB}
	Pin 21		NC	AGND
	Pin 22		NC	DGND
RECOMMENDED OPERATING CONDITIONS	Capacitance of reset gate clock pin external capacitor (pF)		1000 ± 20 %	Unspecified
	Data rate MIN. (MHz)		0.5	Unspecified
ELECTRICAL CHARACTERISTICS	Saturation exposure TYP. (lx·s)		0.17	0.29
	Photo response non-uniformity (%)	TYP. MAX.	4 10	±5 ±10
	Average dark signal TYP. (mV)		0.3	1.0
	Dark signal non-uniformity (mV)	MIN. TYP. MAX.	0 4 6	–3 –1, +3 +6
	Power consumption MAX. (mW)		400	Unspecified
	Response (V/lx·s)	MIN. TYP. MAX.	7.2 9.0 10.8	4.15 5.2 6.25
	Offset level TYP. (V)		3.5	3.0
	Shift register clock pin capacitance (pF) [Note]	MIN. TYP. MAX.	250 350 500	400 500 800
	Dynamic range TYP. (times)	DR1 DR2	375 2143	500 Undefined
	Reset feed-through noise (mV)	MIN. TYP. MAX.	0 400 600	Unspecified 250 500
	Random noise TYP. (mV)		0.7	Undefined
TIMING CHART			In phase outputs operating timing is added	Out of phase outputs operation only
DEFINITIONS OF CHARACTERISTICS ITEMS	Photo response non-uniformity		Absolute value	Minus and plus value
	Dark signal non-uniformity		Absolute value	Minus and plus value
	Random noise		Standard deviation of signal level distribution by scan	Undefined
RECOMMENDED SOLDERING CONDITIONS			Wave soldering is deleted	—

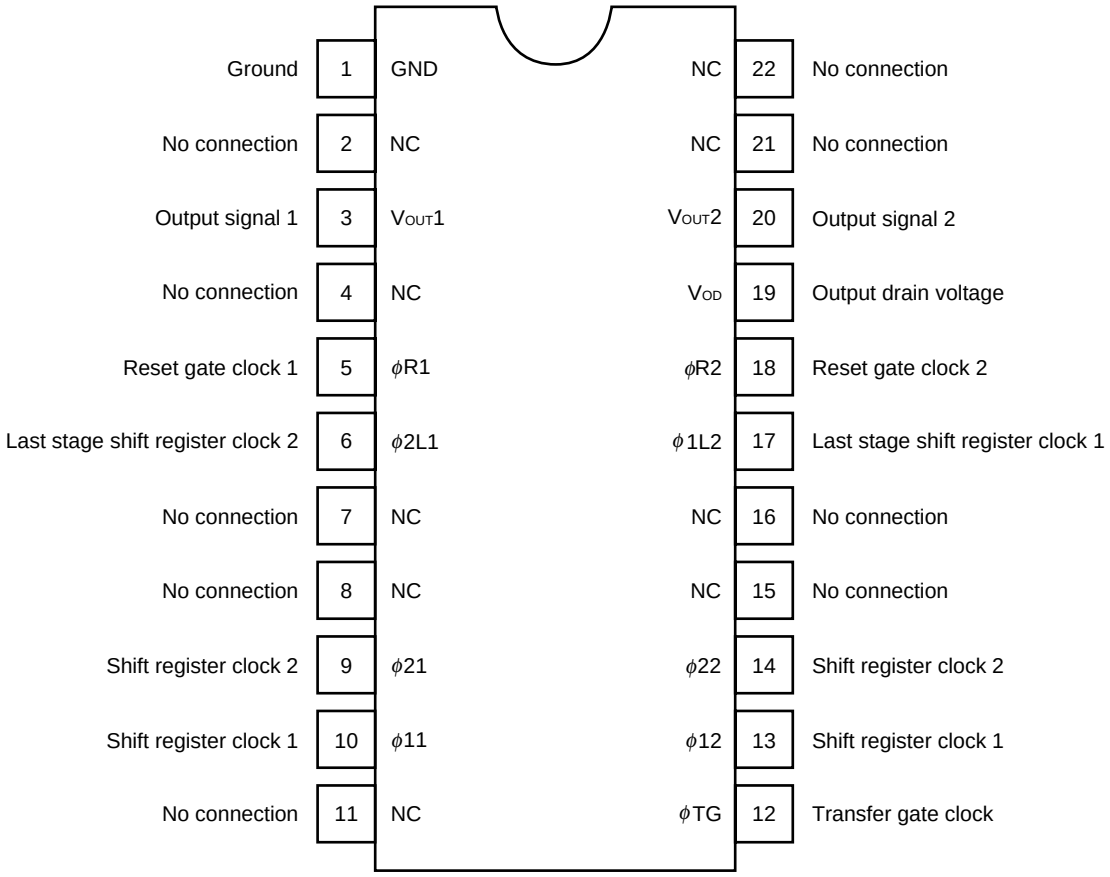
Note Due to the changing of measurement conditions, and pin capacitance of each devices is almost the same. (μPD3739: Power supply = 12 V, μPD35H71A: Power supply = 0 V)

BLOCK DIAGRAM

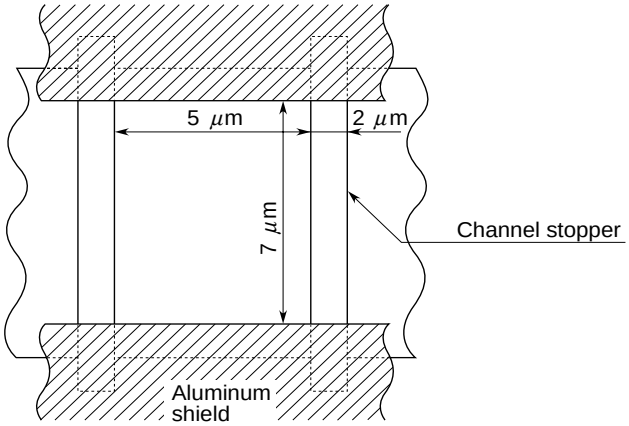


PIN CONFIGURATION (Top View)

CCD linear image sensor 22-pin ceramic DIP (CERDIP) (400 mil)



PHOTOCELL STRUCTURE DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = +25 °C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	–0.3 to +15	V
Shift register clock voltage	$V_{\phi1}$, $V_{\phi2}$	–0.3 to +15	V
Reset gate clock voltage	$V_{\phi R1}$, $V_{\phi R2}$	–0.3 to +15	V
Transfer gate clock voltage	$V_{\phi TG}$	–0.3 to +15	V
Operating ambient temperature	T_A	–25 to +55	°C
Storage temperature	T_{stg}	–40 to +100	°C

Caution Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.

RECOMMENDED OPERATING CONDITIONS (T_A = –25 to +55 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output drain voltage	V_{OD}		11.4	12.0	12.6	V
Shift register clock high level	$V_{\phi1H}$, $V_{\phi2H}$		4.5	5.0	5.5	V
Shift register clock low level	$V_{\phi1L}$, $V_{\phi2L}$		–0.3	0	+0.5	V
Reset gate clock high level	$V_{\phi R1H}$, $V_{\phi R2H}$	**Note**	4.5	5.0	5.5	V
Reset gate clock low level	$V_{\phi R1L}$, $V_{\phi R2L}$	**Note**	–0.3	0	+0.5	V
Capacitance of reset gate clock pin external capacitor	$C_{EXT\phi R}$	Non-polar type	800	1000	1200	pF
Transfer gate clock high level	$V_{\phi TGH}$		4.5	5.0	5.5	V
Transfer gate clock low level	$V_{\phi TGL}$		–0.3	0	+0.5	V
Data rate	$2f_{\phi R1}$, $2f_{\phi R2}$		0.5	2	40	MHz

Note Input the reset gate clocks 1 and 2 (ϕR1, ϕR2) to pins 5 and 18, respectively, via an input resistor and a capacitor. Use of a capacitor is indispensable. Refer to **APPLICATION CIRCUIT EXAMPLE** for the connection method. The reset gate clock high level and low level at the IC pins (after passing through the external capacitor) varies according to the IC, due to the on-chip automatic ϕR level adjuster. The recommended operating conditions of reset gate clocks 1, 2 (ϕR1, ϕR2) in the table above are for signals applied to the external capacitor.

Remark ϕ1 in the above tables represents ϕ11, ϕ12 and ϕ1L2. ϕ2 represents ϕ21, ϕ22 and ϕ2L1.

ELECTRICAL CHARACTERISTICS

(T_A = +25 °C, V_{OD} = 12 V, $f_{\phi 1}$ = 1 MHz, data rate = 2 MHz, storage time = 10 ms
light source: 3200 K halogen lamp + C-500S (infrared cut filter, t = 1 mm), input signal clock = 5 V_{p-p})

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	V_{sat}		1.0	1.5		V
Saturation exposure	SE	Daylight color fluorescent lamp		0.17		lx•s
Photo response non-uniformity	PRNU	V_{OUT} = 500 mV		4	10	%
Average dark signal	ADS	Light shielding		0.3	3.0	mV
Dark signal non-uniformity	DSNU	Light shielding	0	4.0	6.0	mV
Power consumption	P_W			200	400	mW
Output impedance	Z_O			0.2	0.5	kΩ
Response	R_F	Daylight color fluorescent lamp	7.2	9.0	10.8	V/lx·s
Response peak wavelength				550		nm
Image lag	IL	V_{OUT} = 1 V		0.3	1.0	%
Offset level **Note 1**	V_{OS}		2.0	3.5	5.0	V
Output fall delay time **Note 2**	t_d	V_{OUT} = 1 V		20		ns
Register imbalance	RI	V_{OUT} = 500 mV	0		4.0	%
Total transfer efficiency	TTE	V_{OUT} = 500 mV, data rate = 40 MHz	92	98		%
Dynamic range	DR1	V_{sat}/DSNU		375		times
	DR2	V_{sat}/σ		2143		times
Reset feed-through noise **Note 1**	RFTN	Light shielding	0	400	600	mV
Random noise	σ	Light shielding	—	0.7	—	mV

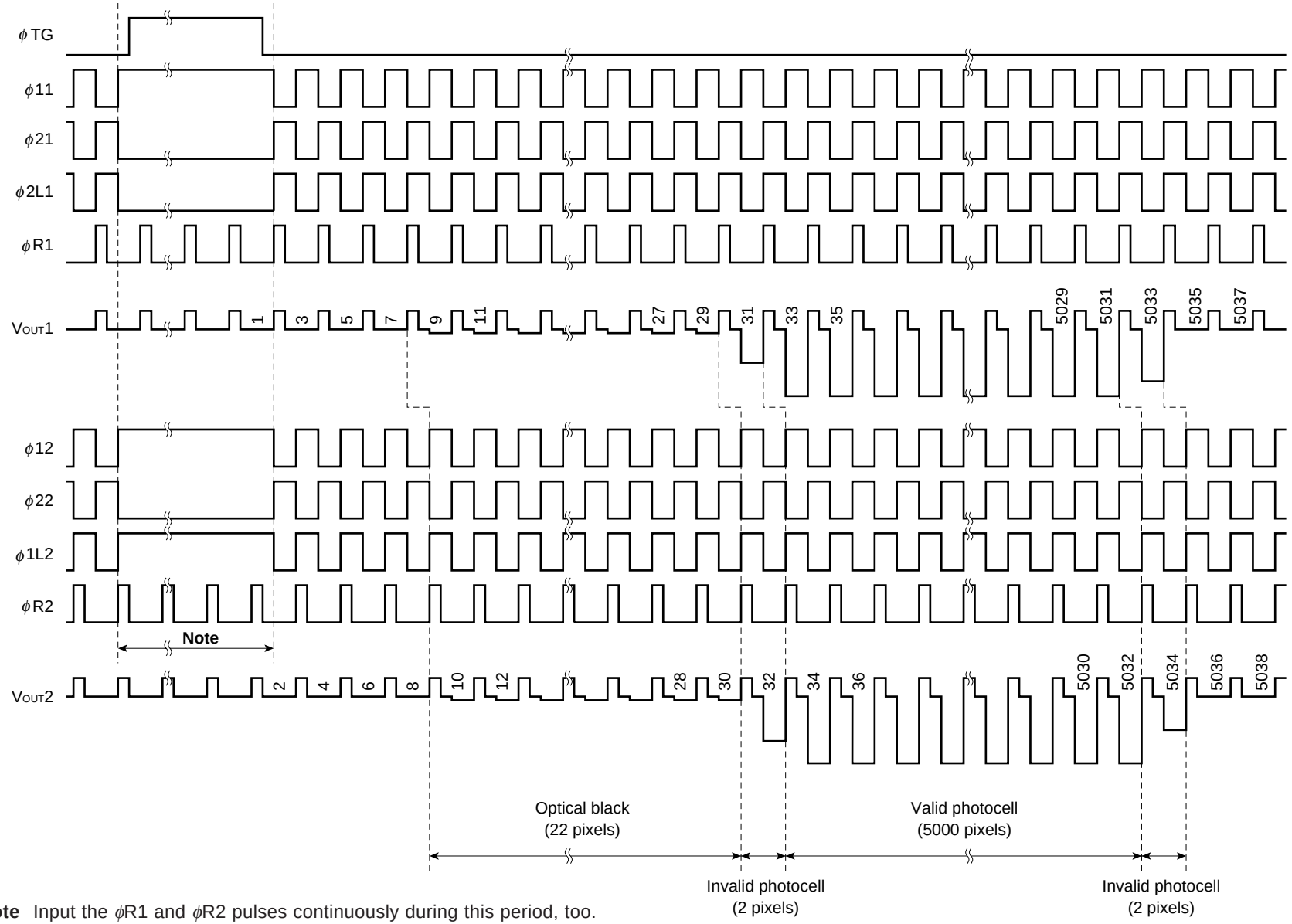
Notes 1. Refer to **TIMING CHART 2, 5**.

2. Typical value when the respective fall times of ϕ1L2 and ϕ2L1 are t11', t41' and t2', t32' (refer to **TIMING CHART 2, 5**). Note that V_{OUT}1 and V_{OUT}2 are the outputs of the two steps of emitter-follower shown in **APPLICATION CIRCUIT EXAMPLE**.

INPUT PIN CAPACITANCE (T_A = +25 °C, V_{OD} = 12 V)

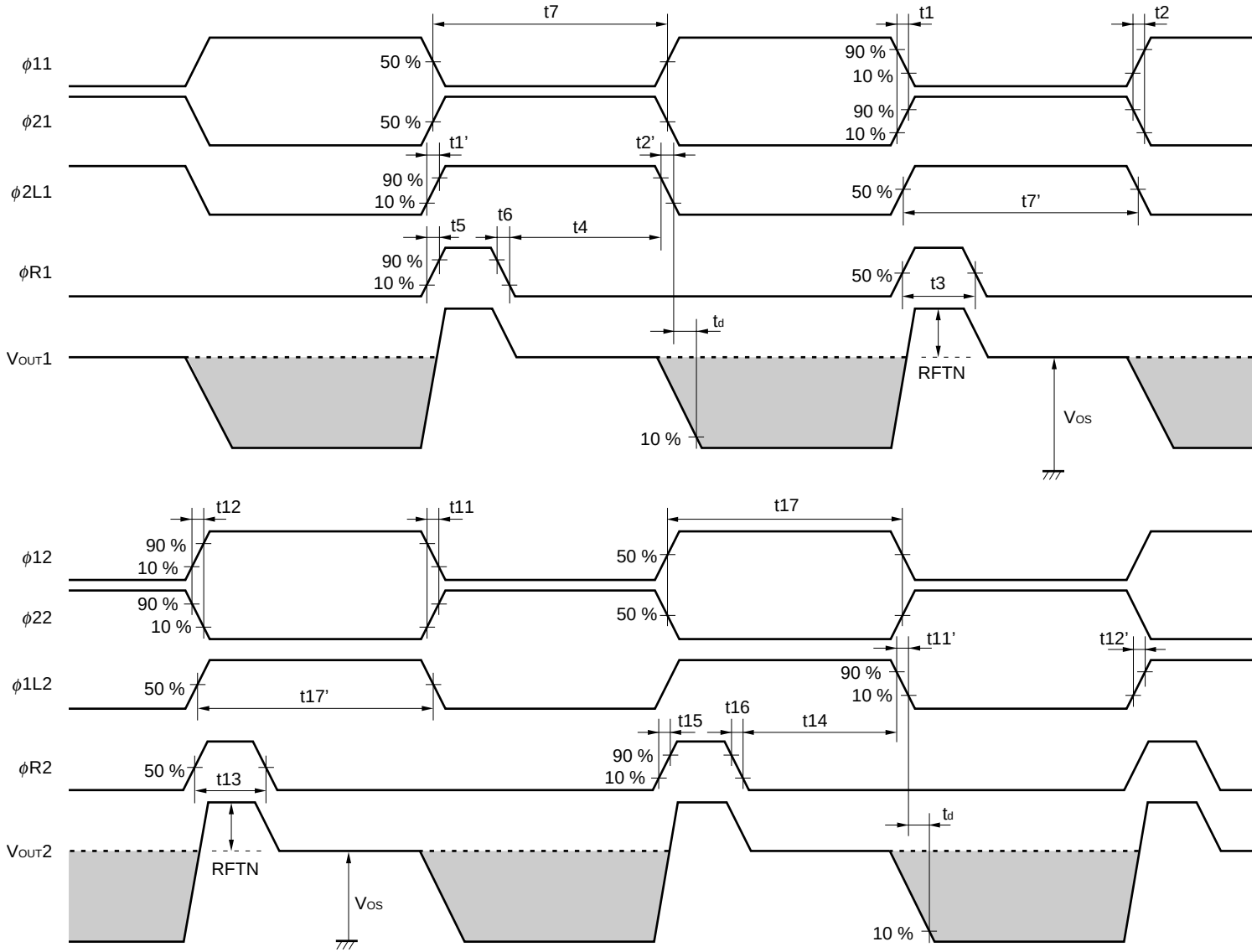
Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1}$	ϕ11	10	250	350	500	pF
		ϕ12	13	250	350	500	pF
Shift register clock pin capacitance 2	$C_{\phi 2}$	ϕ21	9	250	350	500	pF
		ϕ22	14	250	350	500	pF
Last stage shift register clock pin capacitance	$C_{\phi L}$	ϕ1L2	17	40	50	100	pF
		ϕ2L1	6	40	50	100	pF
Reset gate clock pin capacitance	$C_{\phi R}$	ϕR1	5	8	10	15	pF
		ϕR2	18	8	10	15	pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	ϕTG	12	100	150	200	pF

TIMING CHART 1 (Out of phase operation)

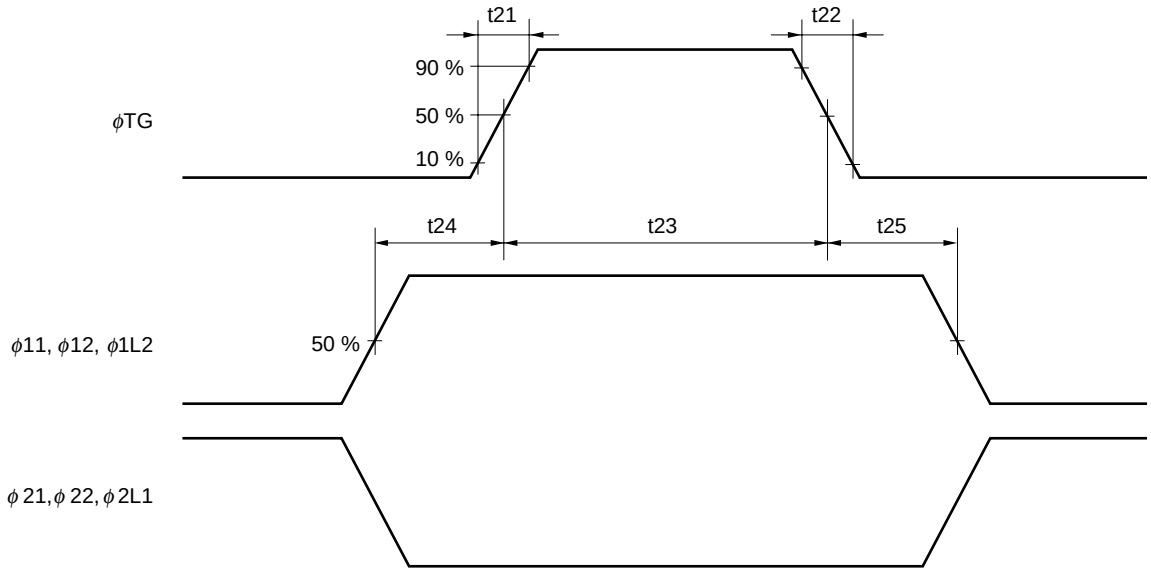


Note Input the φR1 and φR2 pulses continuously during this period, too.

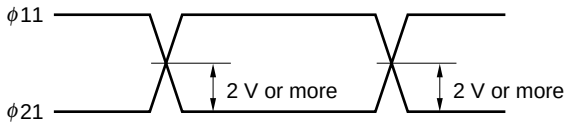
TIMING CHART 2 (Out of phase operation)



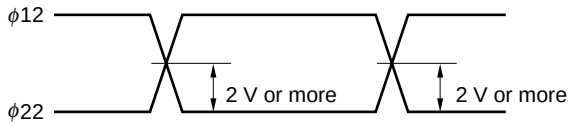
TIMING CHART 3 (Out of phase operation)



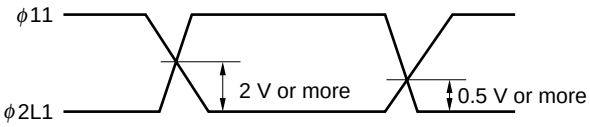
φ11, φ21 cross points



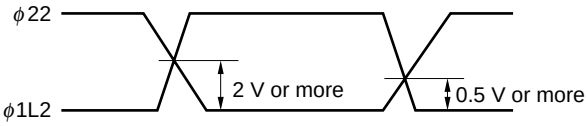
φ12, φ22 cross points



φ11, φ2L1 cross points



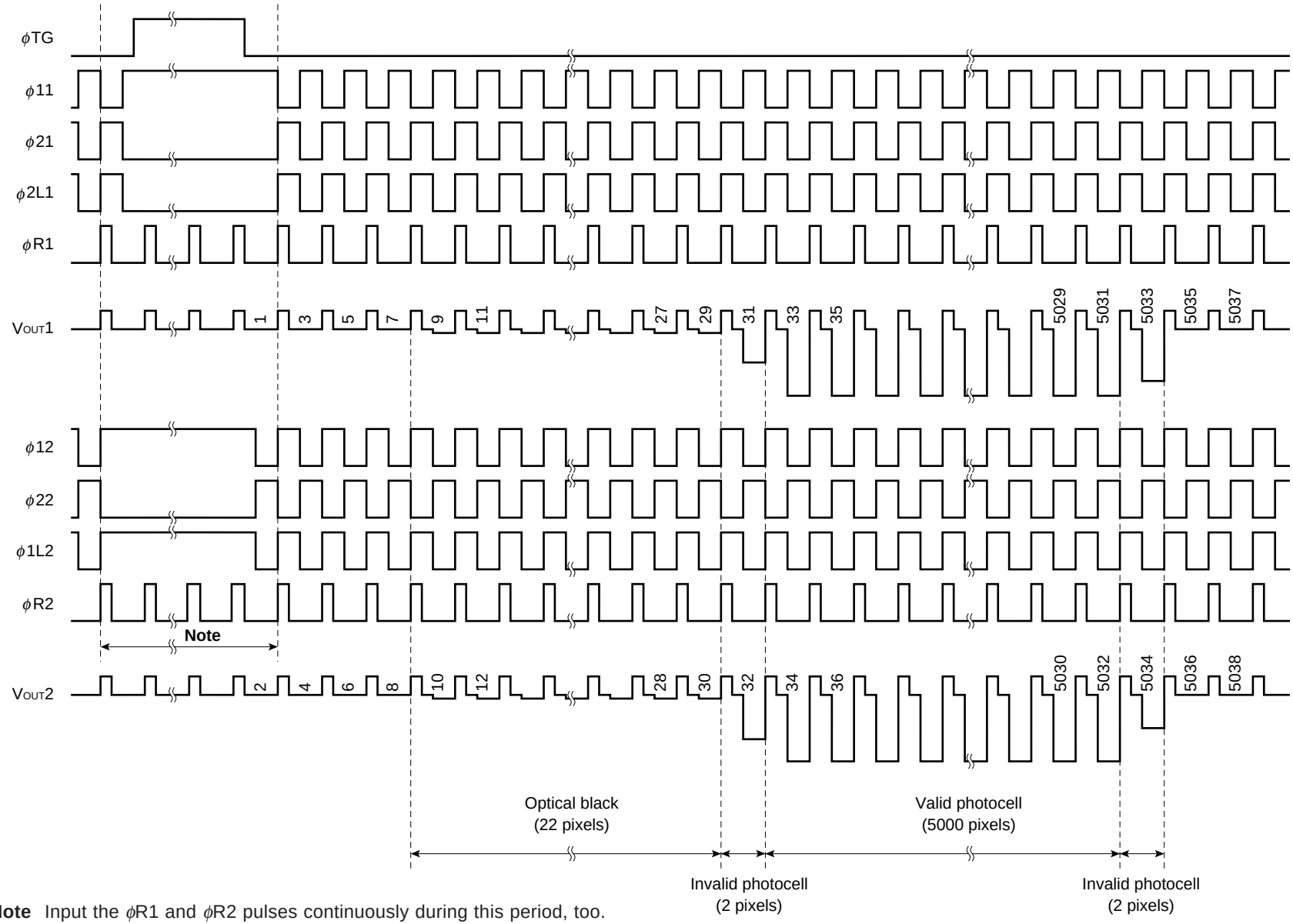
φ1L2, φ22 cross points



Remark Adjust cross points of (φ11, φ21), (φ12, φ22), (φ11, φ2L1) and (φ1L2, φ22) with input resistance of each pin.

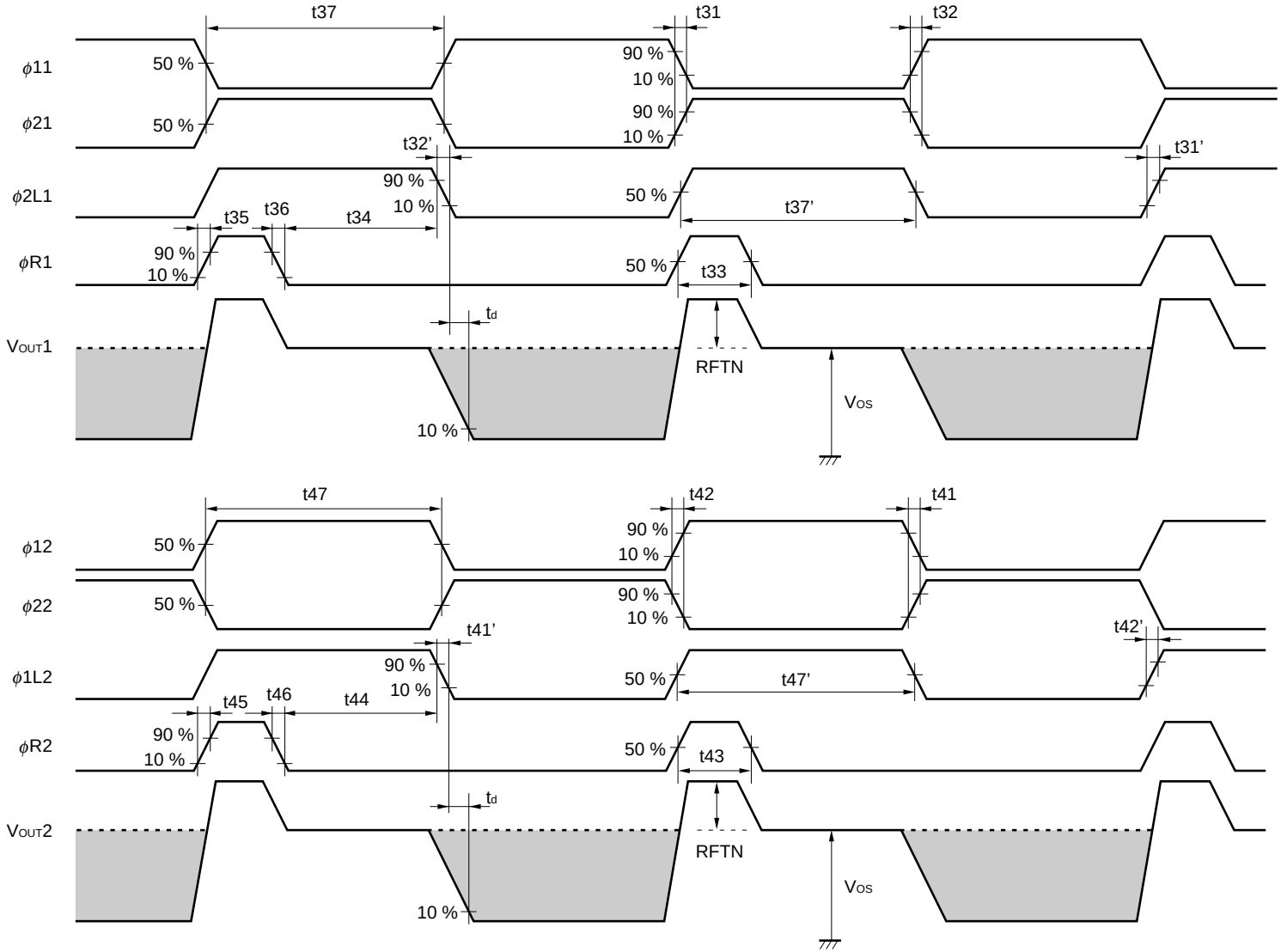
Symbol	MIN.	TYP.	MAX.	Unit
t1, t2, t11, t12	0	50		ns
t1', t2', t11', t12'	0	5		ns
t3, t13	15	50		ns
t4, t14	5	20		ns
t5, t6, t15, t16	0	20		ns
t7, t7', t17, t17'	25	—		ns
t21, t22	0	50		ns
t23	1000	2000	5000	ns
t24, t25	10	100		ns

TIMING CHART 4 (In phase operation)

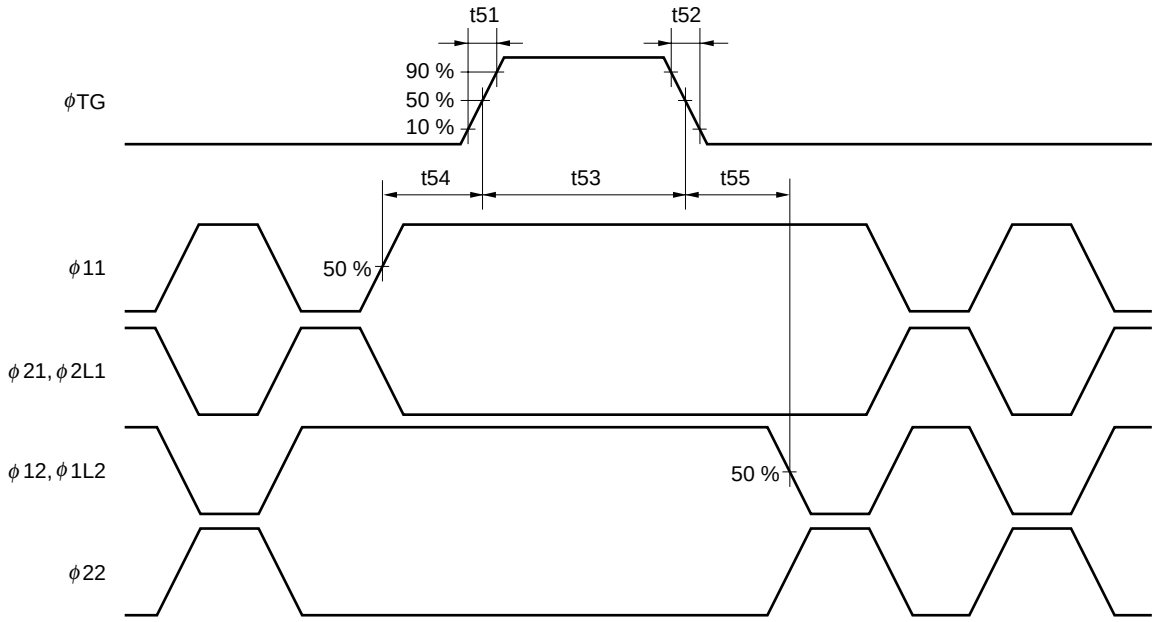


Note Input the φR1 and φR2 pulses continuously during this period, too.

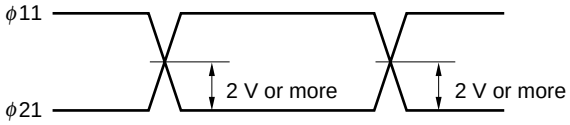
TIMING CHART 5 (In phase operation)



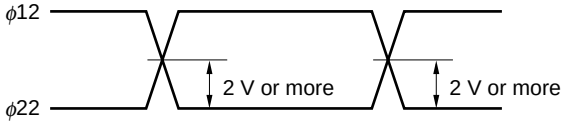
TIMING CHART 6 (In phase operation)



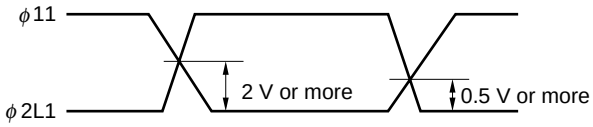
φ11, φ21 cross points



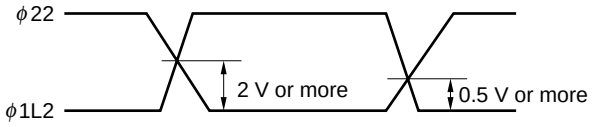
φ12, φ22 cross points



φ11, φ2L1 cross points



φ1L2, φ22 cross points



Remark Adjust cross points of (φ11, φ21), (φ12, φ22), (φ11, φ2L1) and (φ1L2, φ22) with input resistance of each pin.

Symbol	MIN.	TYP.	MAX.	Unit
t31, t32, t41, t42	0	50		ns
t31', t32', t41', t42'	0	5		ns
t33, t43	15	50		ns
t34, t44	5	20		ns
t35, t36, t45, t46	0	20		ns
t37, t37', t47, t47'	25	—		ns
t51, t52	0	50		ns
t53	1000	2000	5000	ns
t54, t55	10	100		ns

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage: V_{sat}
   Output signal voltage at which the response linearity is lost.

2. Saturation exposure: SE
   Product of intensity of illumination (I_X) and storage time(s) when saturation of output voltage occurs.

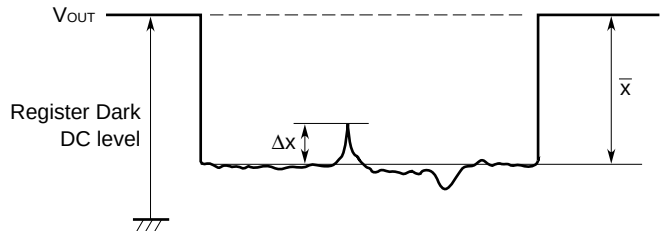
3. Photo response non-uniformity: PRNU
   The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$\text{PRNU (\%)} = \frac{\Delta x}{\overline{x}} \times 100$$

Δx : maximum of $|x_j - \overline{x}|$

$$\overline{x} = \frac{\sum_{j=1}^{5000} x_j}{5000}$$

x_j : Output voltage of valid pixel number j



4. Average dark signal: ADS
   Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

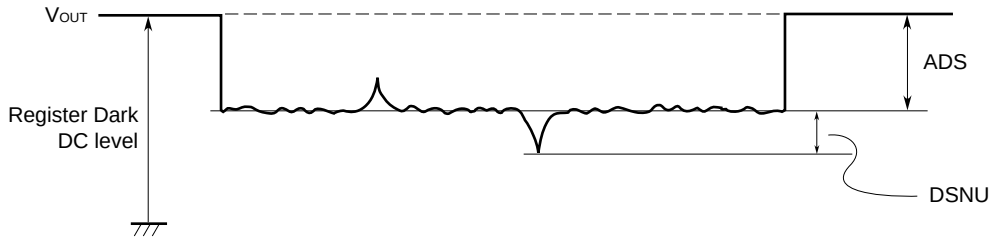
$$\text{ADS (mV)} = \frac{\sum_{j=1}^{5000} d_j}{5000}$$

d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity: DSNU
   Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

$$\text{DSNU (mV): maximum of } | d_j - \text{ADS} |_{j = 1 \text{ to } 5000}$$

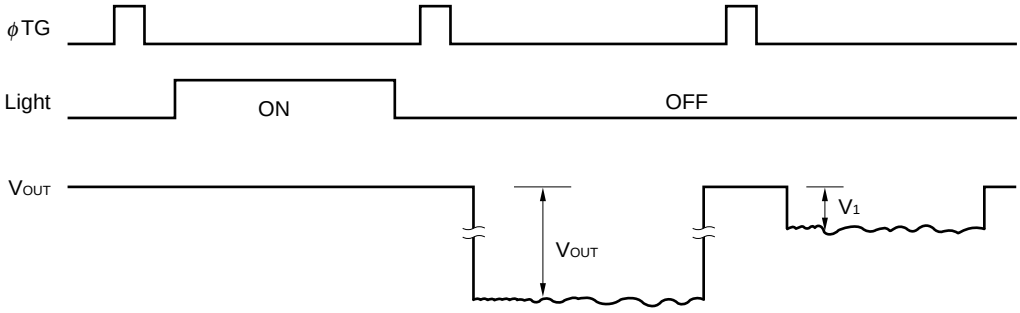
d_j: Dark signal of valid pixel number j



6. Output impedance: Z_O
   Impedance of the output pins viewed from outside.

7. Response: R
   Output voltage divided by exposure (Ix•s).
   Note that the response varies with a light source (spectral characteristic).

8. Image lag: IL
   The rate between the last output voltage and the next one after read out the data of a line.



$$\text{IL (\%)} = \frac{V_1}{V_{OUT}} \times 100$$

9. Register imbalance: RI

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI\ (\%) = \frac{\frac{2}{n}\left|\sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j})\right|}{\frac{1}{n}\sum_{j=1}^{n} V_j} \times 100$$

n : Number of valid pixels

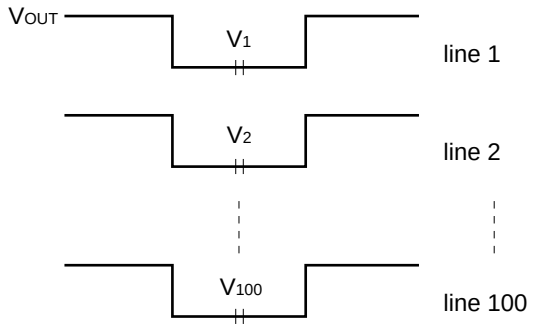
V_j : Output voltage of each pixel

10. Random noise: σ

Random noise σ is defined as the standard deviation of a valid pixel output signal with 100 times (=100 lines) data sampling at dark (light shielding).

$$\sigma\ (mV) = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \overline{V})^2}{100}} \quad , \quad \overline{V} = \frac{1}{100}\sum_{i=1}^{100} V_i$$

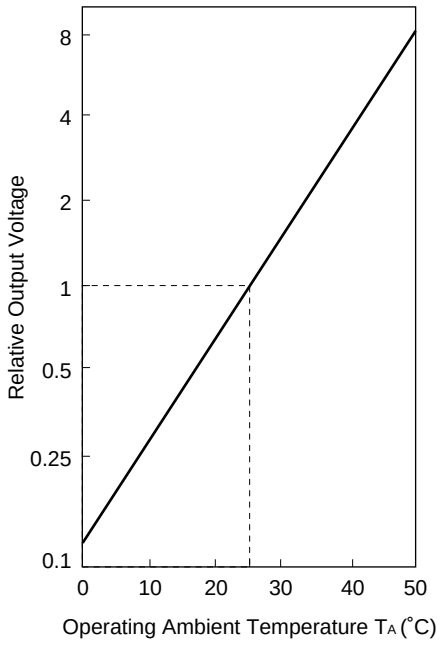
V_i : A valid pixel output signal among all of the valid pixels



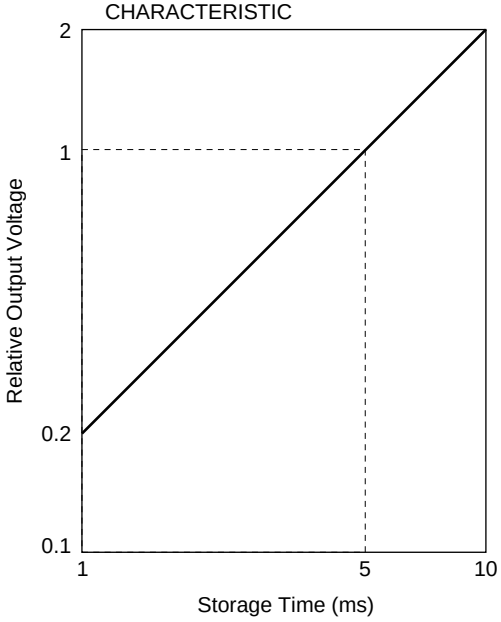
This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

STANDARD CHARACTERISTIC CURVES (T_A = +25 °C)

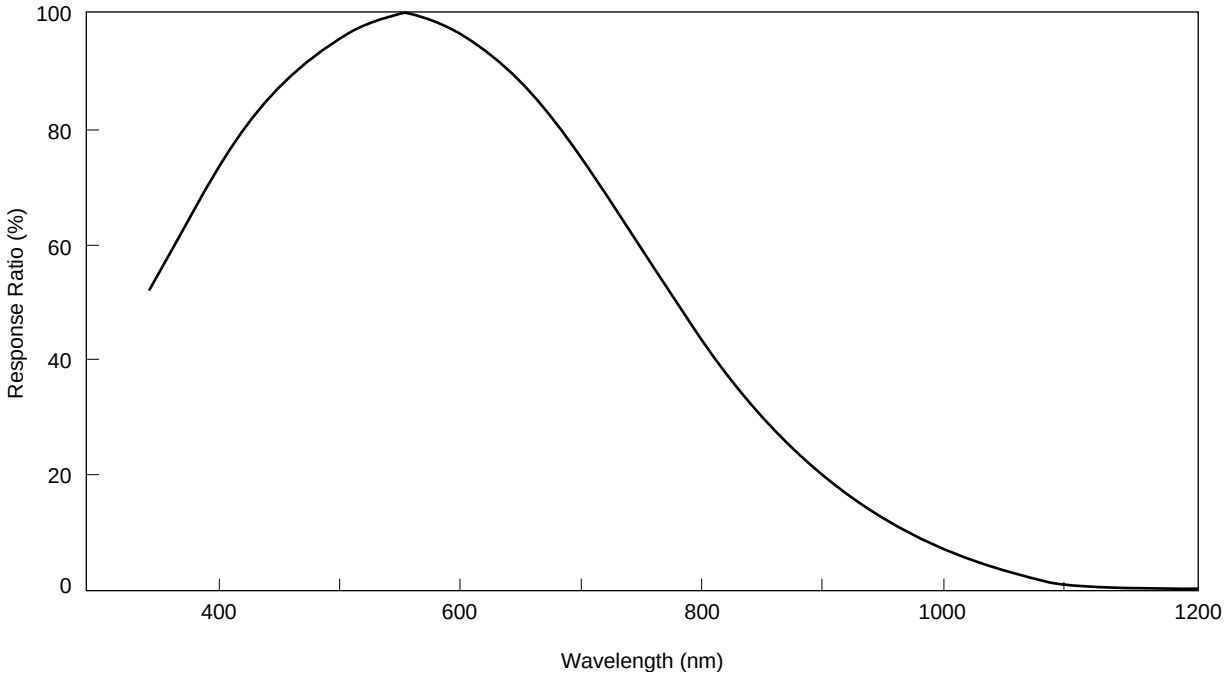
DARK OUTPUT TEMPERATURE CHARACTERISTIC



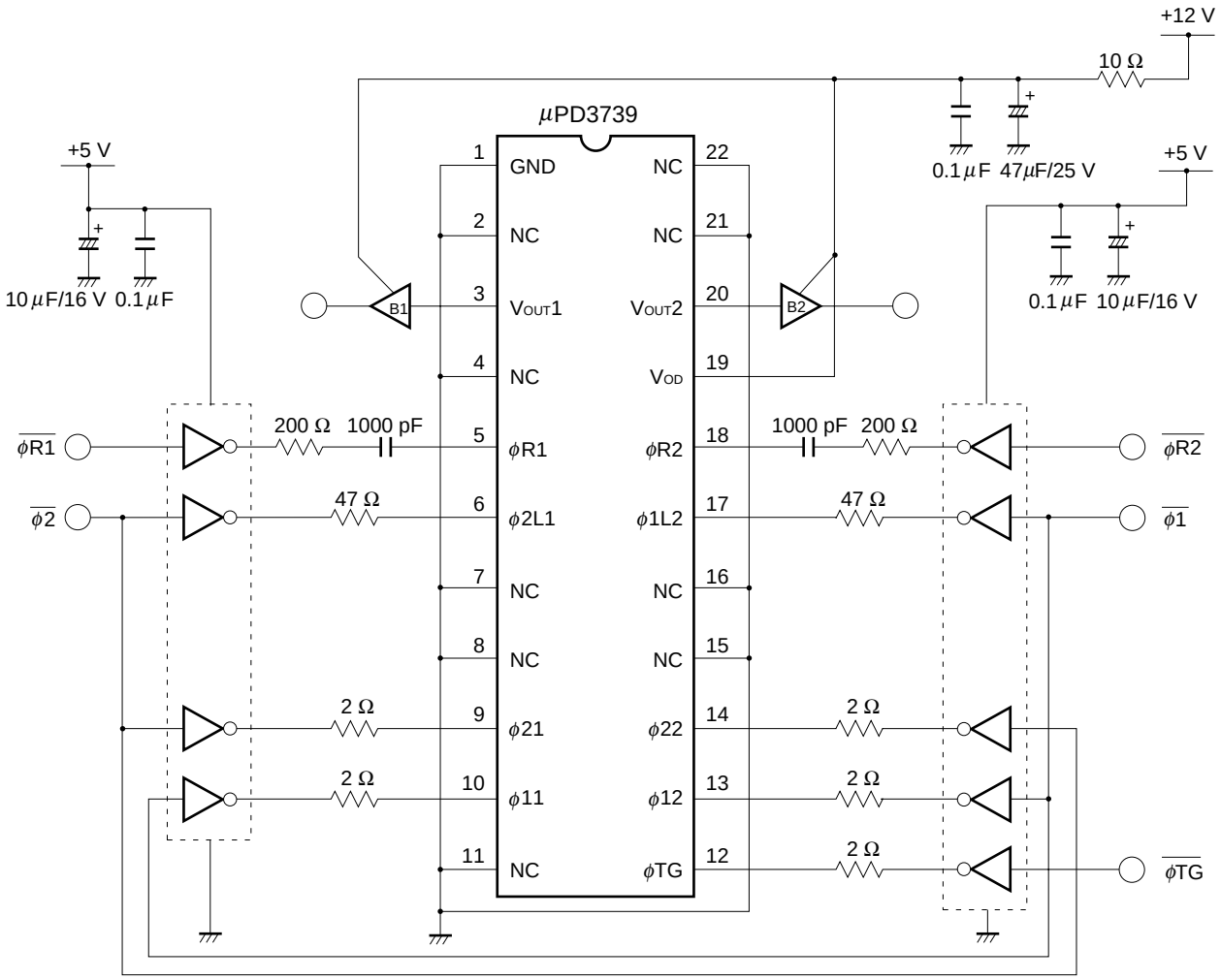
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC



SPECTRAL RESPONSE CHARACTERISTIC



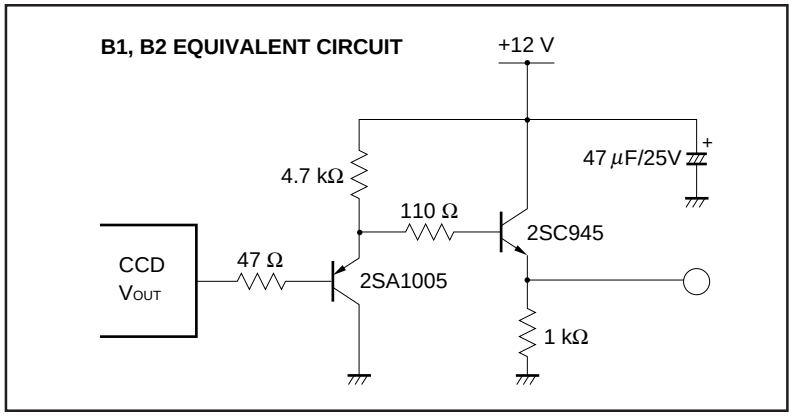
APPLICATION CIRCUIT EXAMPLE (Out of phase operation)



Remarks 1. The μPD3739 can be operated leaving pin 2 (NC) unconnected, and connecting pin 4 (NC) and pin 11 (NC) to a +12 V power supply (when replaces the μPD35H71A).

2. It is recommended that pins 6 (φ2L1) and 17 (φ1L2) each is separately driven a driver other than that of pins 10, 13 (φ11, φ12) and pins 9, 14 (φ21, φ22).

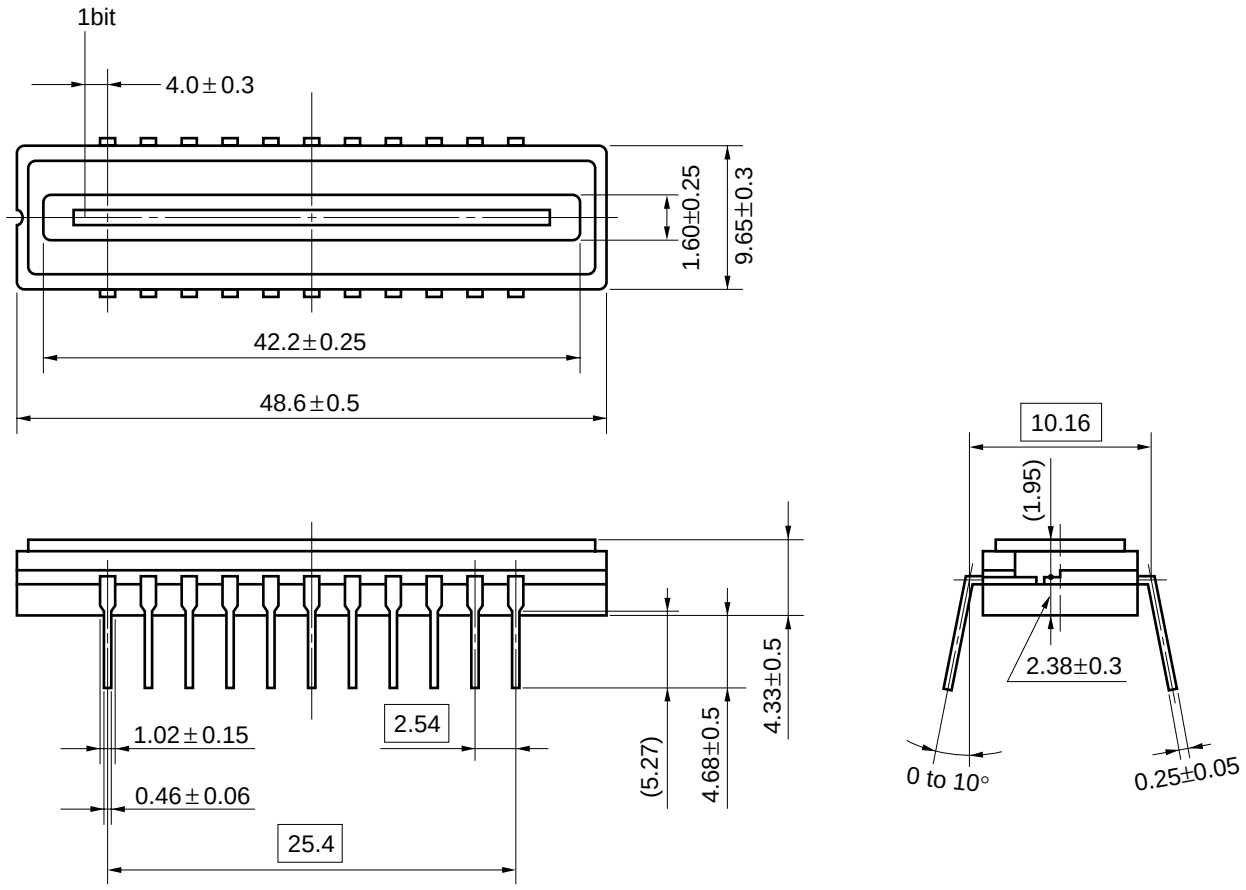
3. The inverters shown in the above application circuit example are the 74AC04.



PACKAGE DRAWING

CCD LINEAR IMAGE SENSOR 22PIN CERAMIC DIP(CERDIP)(400mil)

(Unit : mm)



Name	Dimensions	Refractive index
Glass cap	47.5×9.25×0.7	1.5

22D-1CCD-PKG8

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E)**.

Type of Through-hole Device

μPD3739D: CCD linear image sensor 22-pin ceramic DIP (CERDIP) (400 mil)

Process	Conditions
Partial heating method	Pin temperature: 260 °C or below, Heat time: 10 seconds or less (per pin).

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

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