NEC

MOS INTEGRATED CIRCUIT

μPD3747

7400 PIXELS CCD LINEAR IMAGE SENSOR

The μPD3747 is a high-speed and high sensitive CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal.

The μPD3747 is a 2-output type CCD sensor with 2 rows of high-speed charge transfer register, which transfers the photo signal electrons of 7400 pixels separately in odd and even pixels. And it has reset feed-through level clamp circuits and voltage amplifiers. Therefore, it is suitable for 600 dpi/A3 high-speed digital copiers, multi-function products and so on.

FEATURES

- Valid photocell : 7400 pixels
- Photocell pitch : 4.7 μm
- Photocell size : 4.7 × 4.7 μm^2
- Resolution : 24 dot/mm (600 dpi) A3 (297 × 420 mm) size (shorter side)
- Data rate : 44 MHz MAX. (22 MHz/1 output)
- Output type : 2 outputs in phase
- High sensitivity : 19.0 V/lx•s TYP. (Light source: Daylight color fluorescent lamp)
- Low image lag : 1 % MAX.
- Power supply : +12 V
- Drive clock level : CMOS output under 5 V operation
- On-chip circuits : Reset feed-through level clamp circuits
  Voltage amplifiers

ORDERING INFORMATION

Part Number	Package
μPD3747D	CCD linear image sensor 22-pin ceramic DIP (CERDIP) (10.16 mm (400))

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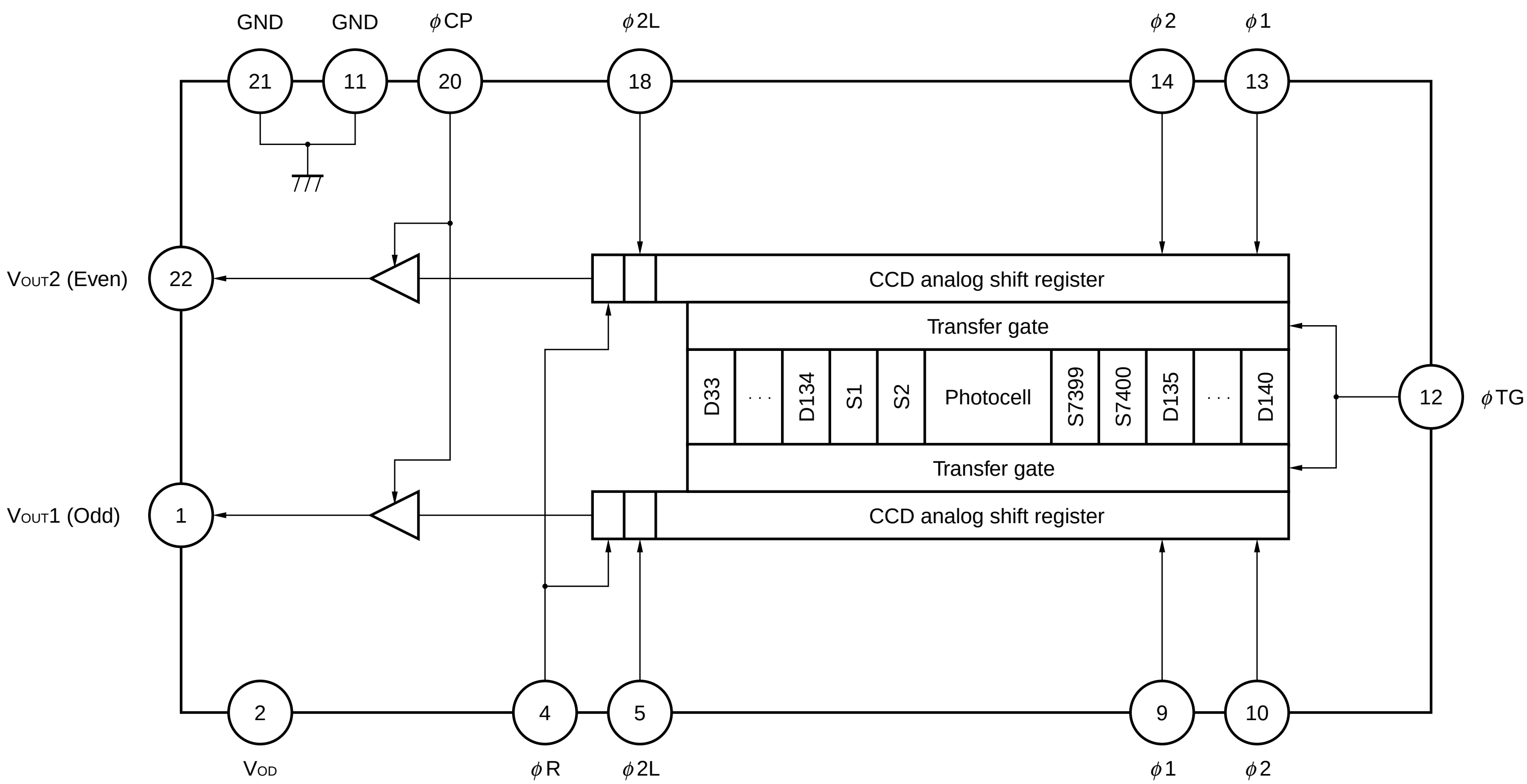
Printed in Japan

BLOCK DIAGRAM



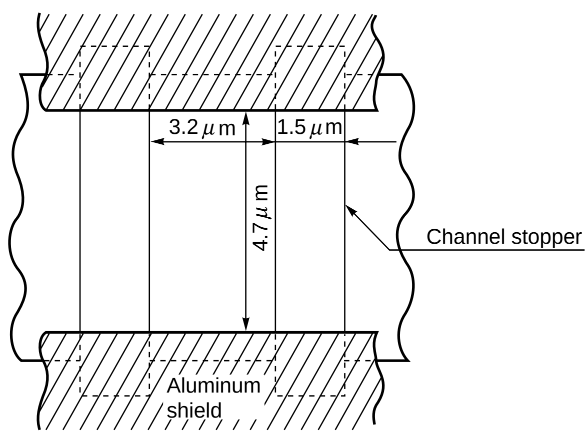
PIN CONFIGURATION (Top View)

CCD linear image sensor 22-pin ceramic DIP (CERDIP) (10.16 mm (400))

- μPD3747D

Output signal 1 (Odd)	$V_{OUT}1$	1	22	$V_{OUT}2$	Output signal 2 (Even)
Output drain voltage	V_{OD}	2	21	GND	Ground
No connection	NC	3	20	ϕCP	Reset feed-through level clamp clock
Reset gate clock	ϕR	4	19	NC	No connection
Last stage shift register clock 2	ϕ2L	5	18	ϕ2L	Last stage shift register clock 2
No connection	NC	6	17	NC	No connection
No connection	NC	7	16	NC	No connection
No connection	NC	8	15	NC	No connection
Shift register clock 1	ϕ1	9	14	ϕ2	Shift register clock 2
Shift register clock 2	ϕ2	10	13	ϕ1	Shift register clock 1
Ground	GND	11	12	ϕTG	Transfer gate clock

PHOTOCELL STRUCTURE DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	–0.3 to +14	V
Shift register clock voltage	$V_{\phi 1}$, $V_{\phi 2}$, $V_{\phi 2L}$	–0.3 to +8	V
Reset gate clock voltage	$V_{\phi R}$	–0.3 to +8	V
Reset feed-through level clamp clock voltage	$V_{\phi CP}$	–0.3 to +8	V
Transfer gate clock voltage	$V_{\phi TG}$	–0.3 to +8	V
Operating ambient temperature	T_A	–25 to +55	°C
Storage temperature	T_{stg}	–40 to +100	°C

Caution Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output drain voltage	V_{OD}	11.4	12.0	12.6	V
Shift register clock high level	$V_{\phi 1H}$, $V_{\phi 2H}$, $V_{\phi 2LH}$	4.5	5.0	5.5	V
Shift register clock low level	$V_{\phi 1L}$, $V_{\phi 2L}$, $V_{\phi 2LL}$	–0.3	0	+0.5	V
Reset gate clock high level	$V_{\phi RH}$	4.5	5.0	5.5	V
Reset gate clock low level	$V_{\phi RL}$	–0.3	0	+0.5	V
Reset feed-through level clamp clock high level	$V_{\phi CPH}$	4.5	5.0	5.5	V
Reset feed-through level clamp clock low level	$V_{\phi CPL}$	–0.3	0	+0.5	V
Transfer gate clock high level	$V_{\phi TGH}$	4.5	5.0	5.5	V
Transfer gate clock low level	$V_{\phi TGL}$	–0.3	0	+0.5	V
Data rate	$2f_{\phi R}$	1	2	44	MHz

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{OD} = 12 V, $f_{\phi R}$ = 1 MHz, data rate = 2 MHz, storage time = 10 ms, input signal clock = 5 V_{p-p},
light source : 3200 K halogen lamp + C-500S (infrared cut filter, t = 1 mm) + HA-50 (heat absorbing filter, t = 3 mm))

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	V_{sat}		1.5	2.0	–	V
Saturation exposure	SE	Daylight color fluorescent lamp	–	0.10	–	lx•s
Photo response non-uniformity	PRNU	V_{OUT} = 500 mV	–	5	10	%
Average dark signal	ADS	Light shielding	–	0.5	3.0	mV
Dark signal non-uniformity	DSNU	Light shielding	–	8.0	14.0	mV
Power consumption	P_W		–	350	600	mW
Output impedance	Z_O		–	0.2	0.3	kΩ
Response	R_F	Daylight color fluorescent lamp	13.3	19.0	24.7	V/lx•s
Image lag	IL	V_{OUT} = 500 mV	–	0.5	1.0	%
Offset level Note 1	V_{OS}		3.7	4.7	5.7	V
Output fall delay time Note 2	t_d	V_{OUT} = 500 mV	–	14	–	ns
Register imbalance	RI	V_{OUT} = 500 mV	0	1.0	4.0	%
Total transfer efficiency	TTE	V_{OUT} = 1 V, data rate = 44 MHz	94	98	–	%
Response peak			–	550	–	nm
Dynamic range	DR1	V_{sat}/DSNU	–	250	–	times
	DR2	V_{sat}/σ bit	–	1000	–	times
Reset feed-through noise Note 1	RFTN	Light shielding	–300	+300	+900	mV
Random noise	σ bit	Light shielding, bit clamp mode	–	2.0	–	mV
	σ line	Light shielding, line clamp mode	–	8.0	–	mV
Shot noise	σ shot	V_{OUT} = 500 mV, bit clamp mode	–	8.0	–	mV

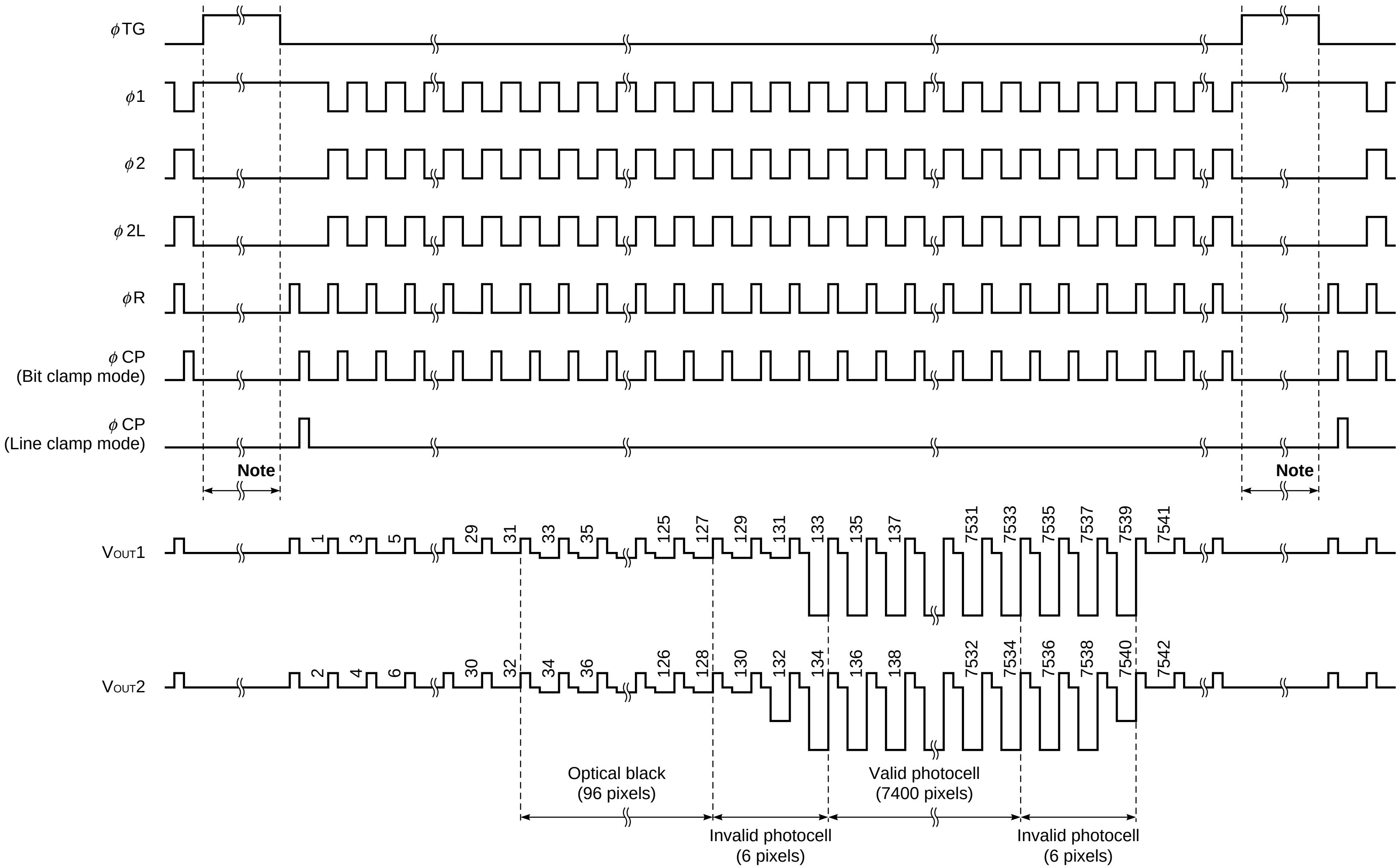
Notes 1. Refer to **TIMING CHART 2, 3**.

2. When the fall time of ϕ2L (t2') is the TYP. value (refer to **TIMING CHART 2, 3**). Note that $V_{OUT}1$ and $V_{OUT}2$ are the outputs of the two steps of emitter-follower shown in **APPLICATION CIRCUIT EXAMPLE**.

INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = 12 V)

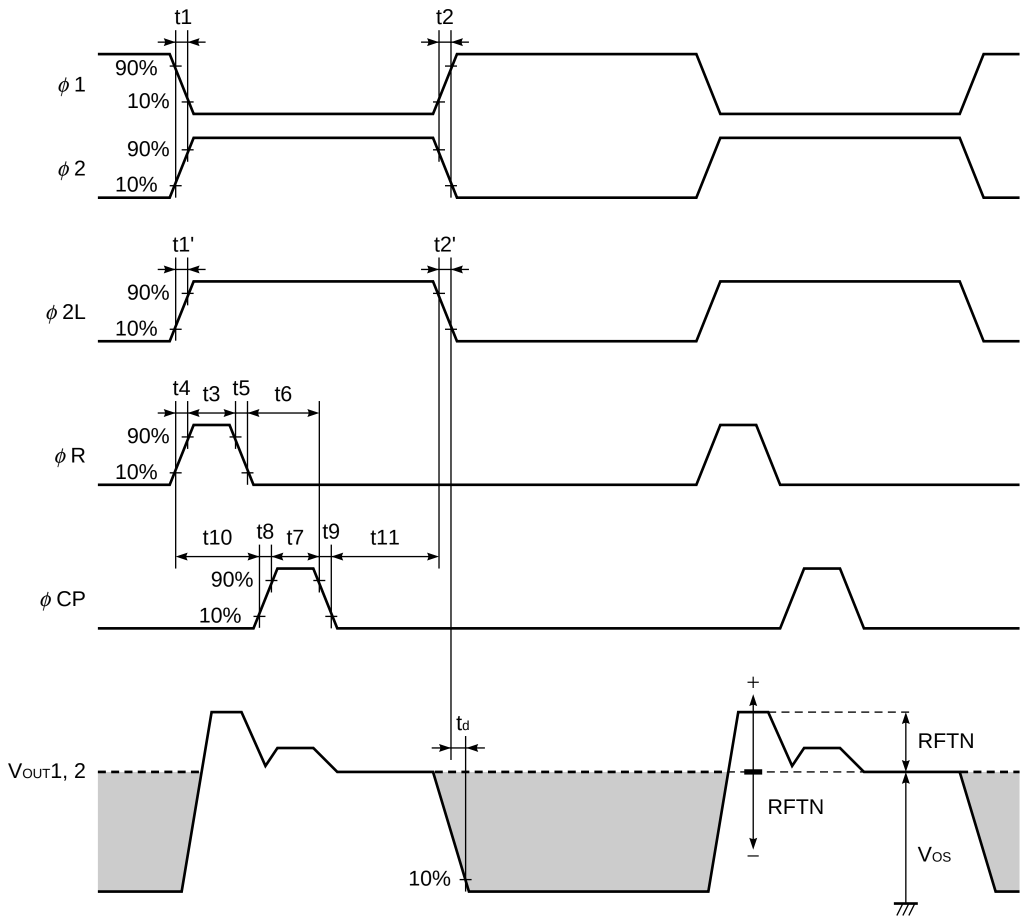
Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1}$	ϕ1	9	–	250	300	pF
			13	–	250	300	pF
Shift register clock pin capacitance 2	$C_{\phi 2}$	ϕ2	10	–	250	300	pF
			14	–	250	300	pF
Last stage shift register clock pin capacitance	$C_{\phi L}$	ϕ2L	5	–	10	20	pF
			18	–	10	20	pF
Reset gate clock pin capacitance	$C_{\phi R}$	ϕR	4	–	10	20	pF
Reset feed-through level clamp clock pin capacitance	$C_{\phi CP}$	ϕCP	20	–	10	20	pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	ϕTG	12	–	100	150	pF

TIMING CHART 1



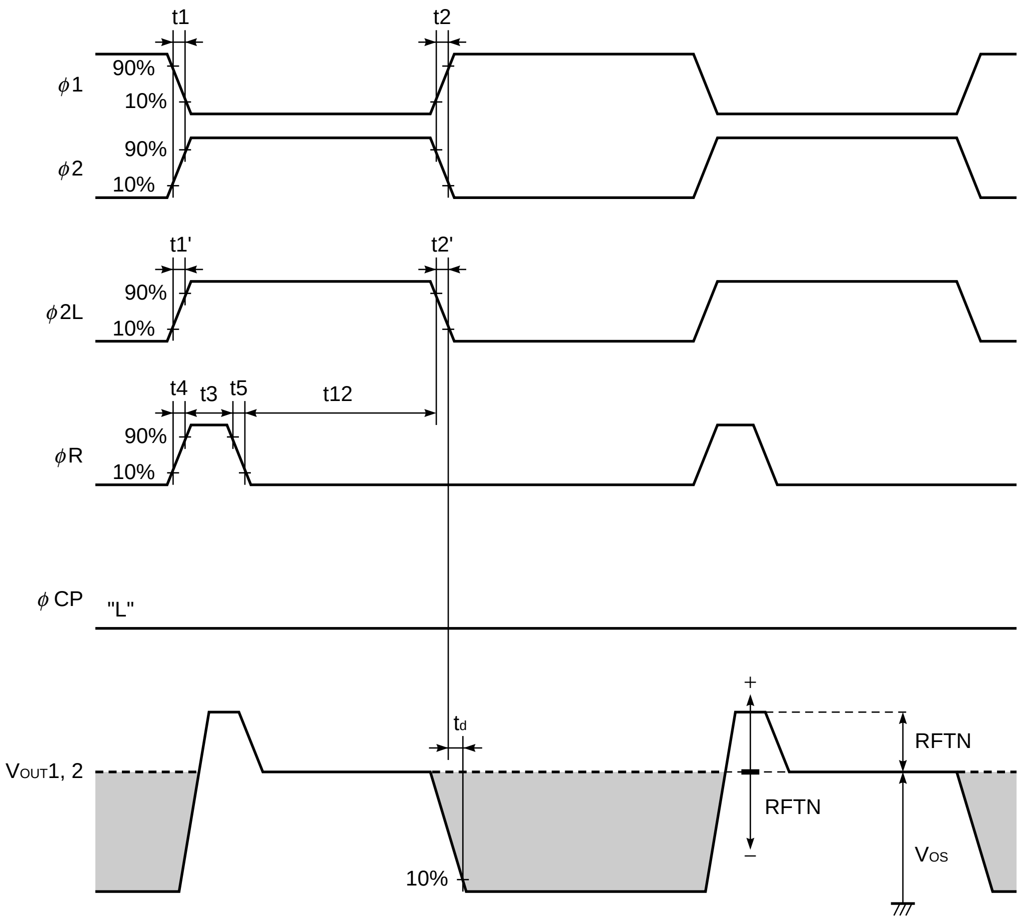
Note Set the ϕR and ϕCP to low level during this period.

TIMING CHART 2 (Bit clamp mode)



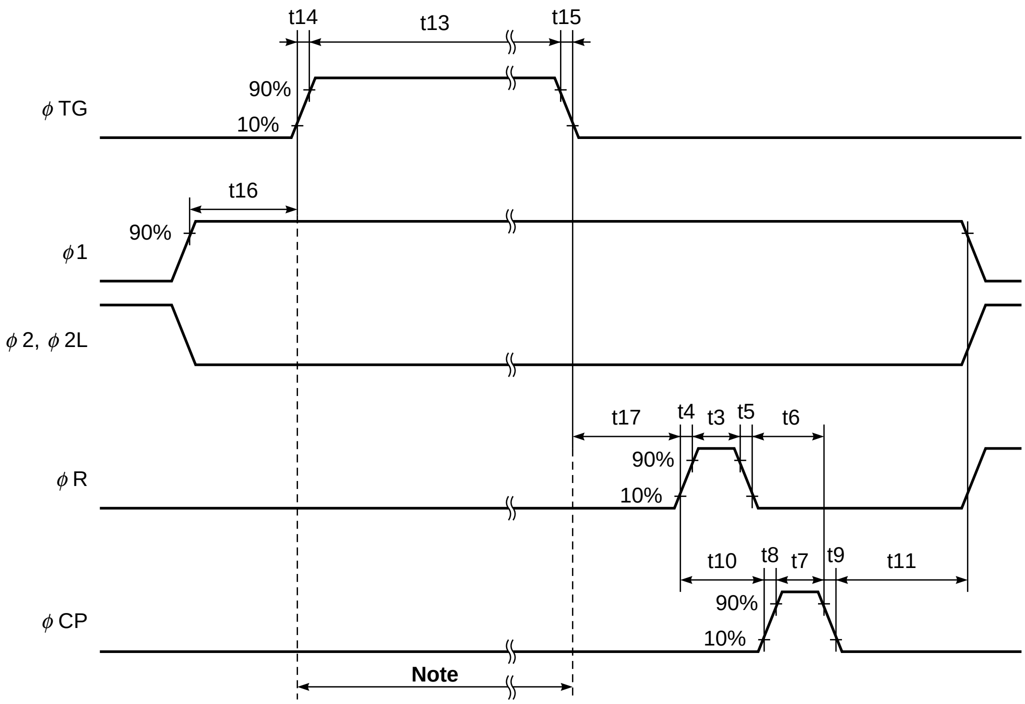
Symbol	MIN.	TYP.	MAX.	Unit
t1, t2	0	50	–	ns
t1', t2'	0	5	–	ns
t3	10	125	–	ns
t4, t5	0	5	–	ns
t6	0	125	–	ns
t7	5	125	–	ns
t8, t9	0	5	–	ns
t10	t3	125	–	ns
t11	0	250	–	ns

TIMING CHART 3 (Line clamp mode)



Symbol	MIN.	TYP.	MAX.	Unit
t1, t2	0	50	–	ns
t1', t2'	0	5	–	ns
t3	10	125	–	ns
t4, t5	0	5	–	ns
t12	5	250	–	ns

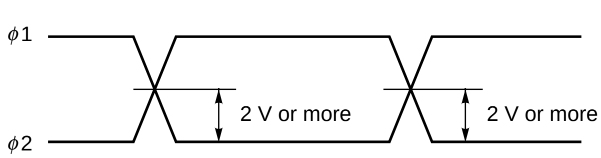
TIMING CHART 4 (Bit clamp mode, Line clamp mode)



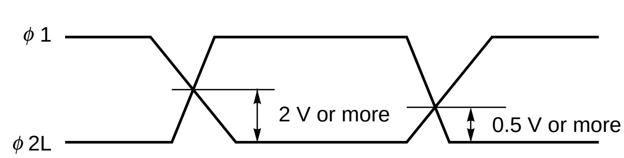
Note Set the φR and φCP to low level during this period.

Symbol	MIN.	TYP.	MAX.	Unit
t3	10	125	–	ns
t4, t5	0	5	–	ns
t6	0	125	–	ns
t7	5	125	–	ns
t8, t9	0	5	–	ns
t10	t3	125	–	ns
t11	0	250	–	ns
t13	1000	1500	–	ns
t14, t15	0	50	–	ns
t16, t17	200	300	–	ns

φ1, φ2 cross points



φ1, φ2L cross points



Remark Adjust cross points of (φ1, φ2) and (φ1, φ2L) with input resistance of each pin.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage : **V_{sat}**
   Output signal voltage at which the response linearity is lost.

2. Saturation exposure : **SE**
   Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

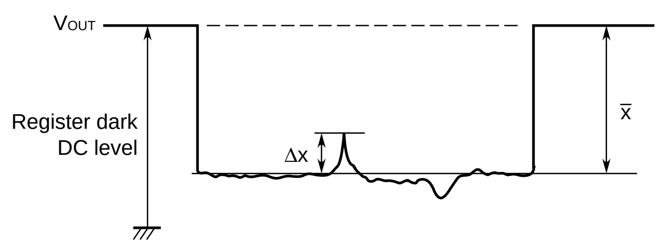
3. Photo response non-uniformity : **PRNU**
   The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$\text{PRNU (\%)} = \frac{\Delta x}{\overline{x}} \times 100$$

Δx: maximum of $|x_j - \overline{x}|$

$$\overline{x} = \frac{\sum_{j=1}^{7400} x_j}{7400}$$

x_j: Output voltage of valid pixel number j



4. Average dark signal : **ADS**
   Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$\text{ADS (mV)} = \frac{\sum_{j=1}^{7400} d_j}{7400}$$

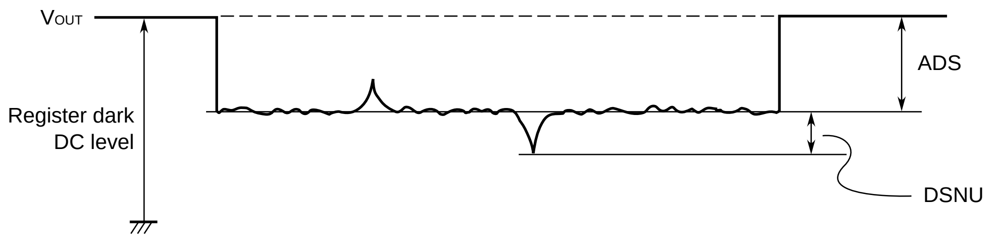
d_j: Dark signal of valid pixel number j

5. Dark signal non-uniformity : **DSNU**

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

DSNU (mV): maximum of $|d_j - ADS|_{\ j = 1 \text{ to } 7400}$

d_j: Dark signal of valid pixel number j



6. Output impedance : **ZO**

Impedance of the output pins viewed from outside.

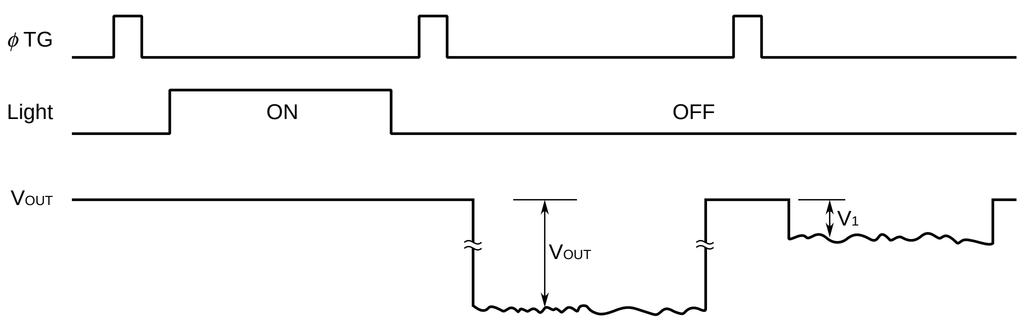
7. Response : **R**

Output voltage divided by exposure (lx•s).

Note that the response varies with a light source (spectral characteristic).

8. Image lag : **IL**

The rate between the last output voltage and the next one after read out the data of a line.



$$IL\ (\%) = \frac{V_1}{V_{OUT}} \times 100$$

9. Register imbalance : **RI**

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI\ (\%) = \frac{\frac{2}{n}\left|\sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j})\right|}{\frac{1}{n}\sum_{j=1}^{n} V_j} \times 100$$

n : Number of valid pixels

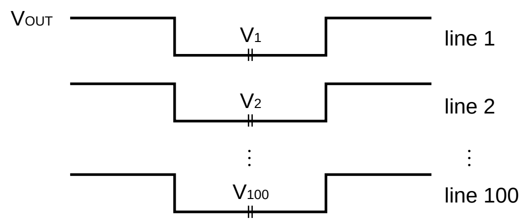
V_j : Output voltage of each pixel

10. Random noise : σ

Random noise σ is defined as the standard deviation of a valid pixel output signal with 100 times (= 100 lines) data sampling at dark (light shielding).

$$\sigma\ (\text{mV}) = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \overline{V})^2}{100}} \quad , \quad \overline{V} = \frac{1}{100}\sum_{i=1}^{100} V_i$$

V_i : A valid pixel output signal among all of the valid pixels



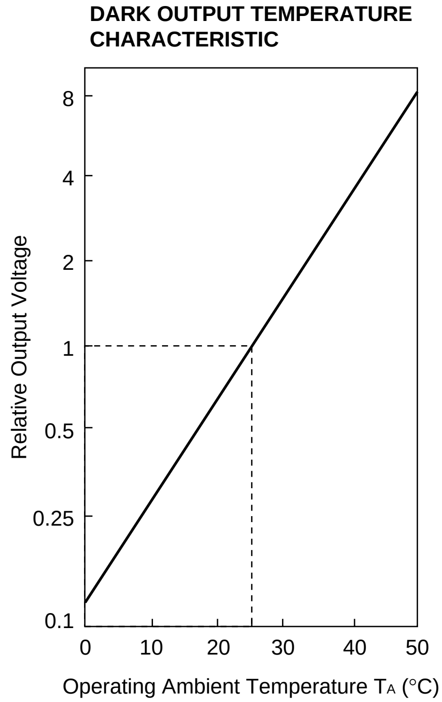
This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

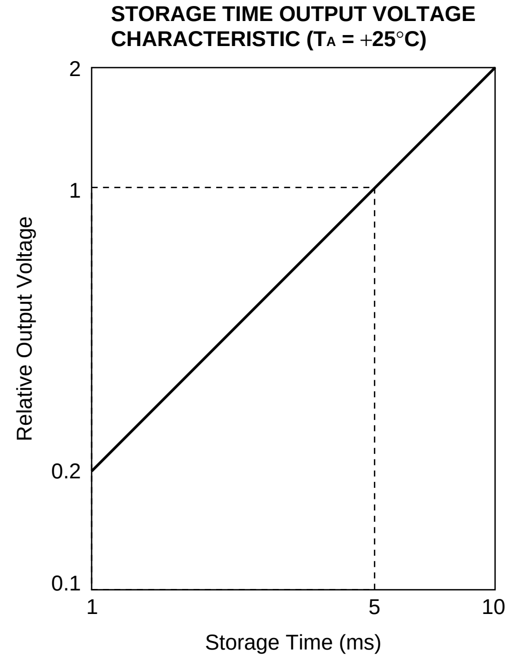
11. Shot noise : **σ shot**

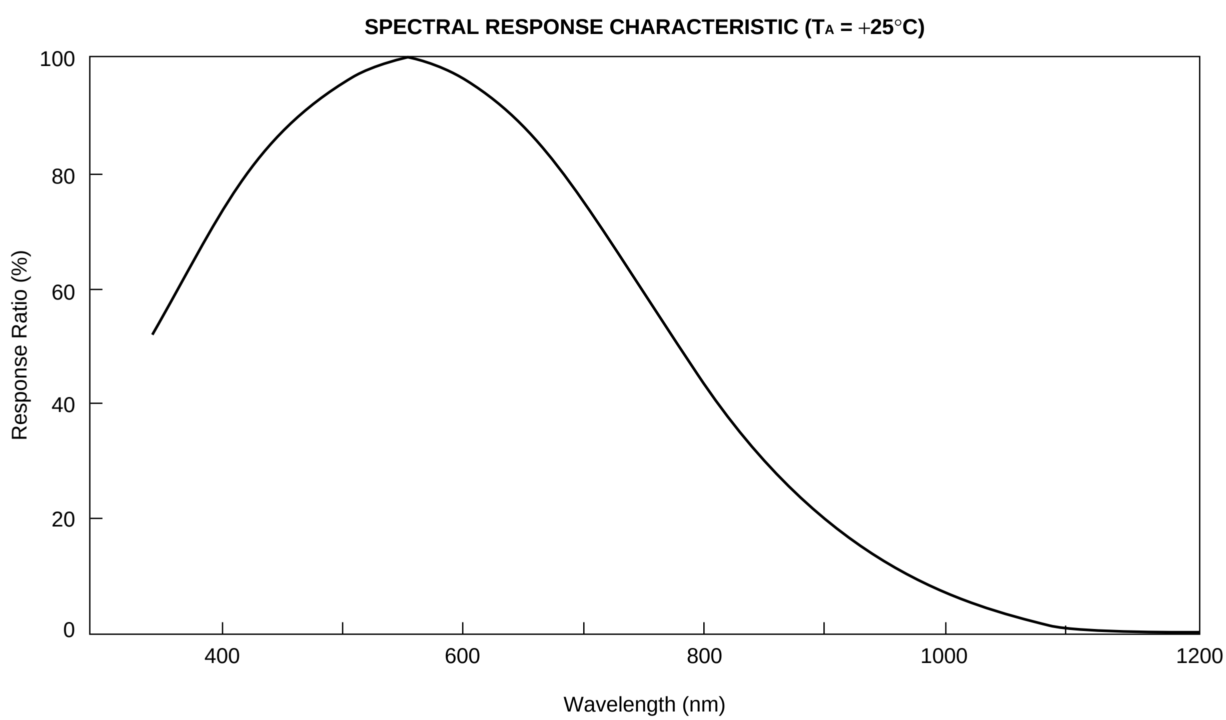
Shot noise is defined as the standard deviation of a valid pixel output signal with 100 times (= 100 lines) data sampling in the light. This includes the random noise.

The formula is the same with that of random noise.

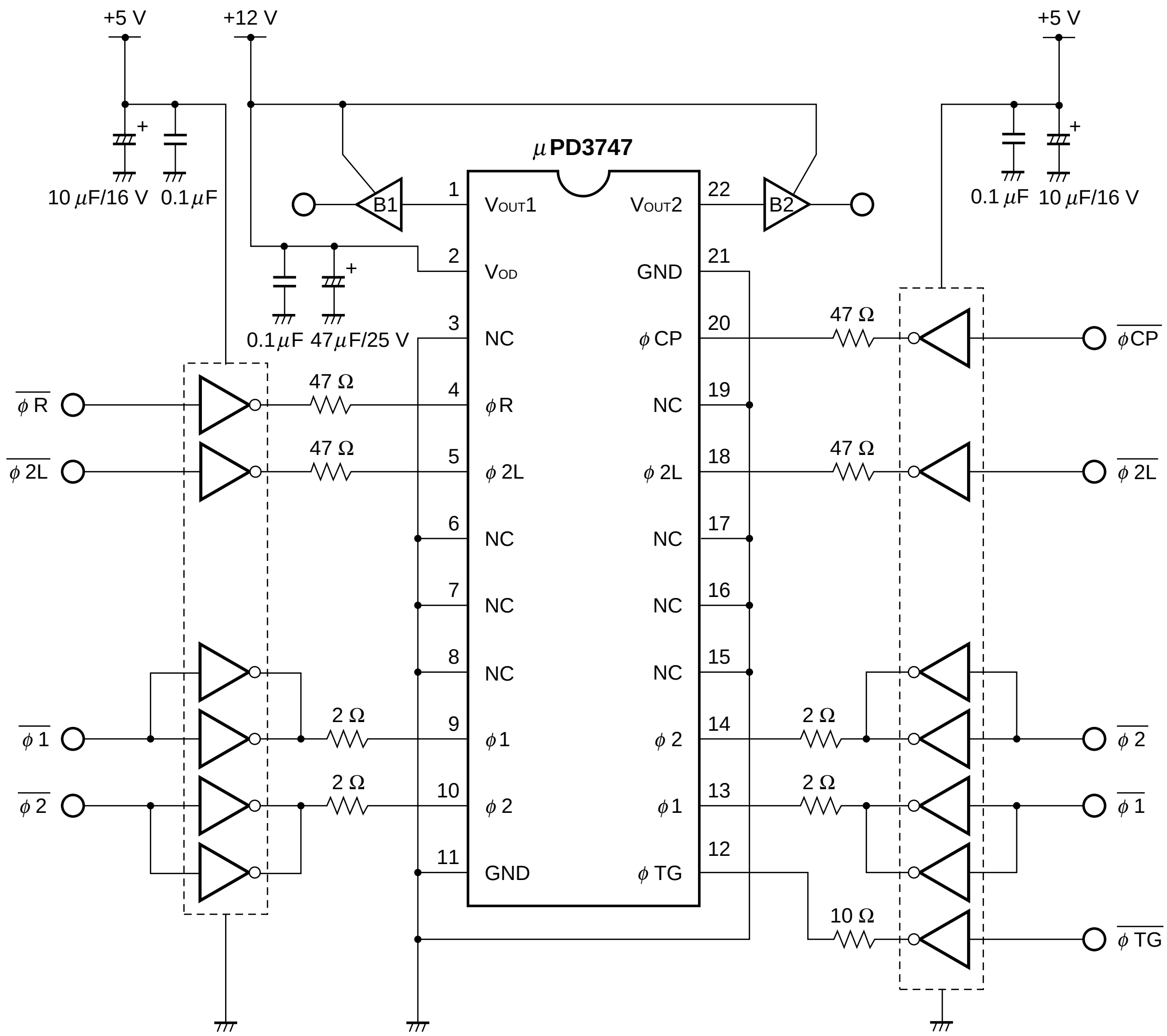
STANDARD CHARACTERISTIC CURVES (Nominal)





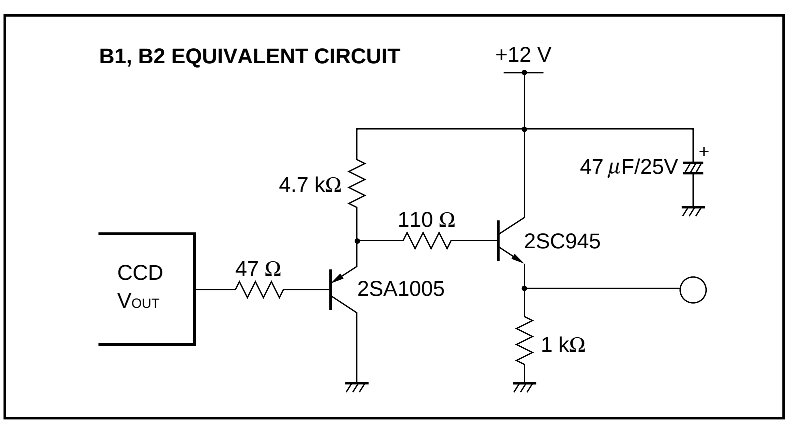


APPLICATION CIRCUIT EXAMPLE



Remarks 1. It is recommended that pins 5 and 18 (φ 2L) are separately driven a driver other than that of pins 10, 14 (φ 2).

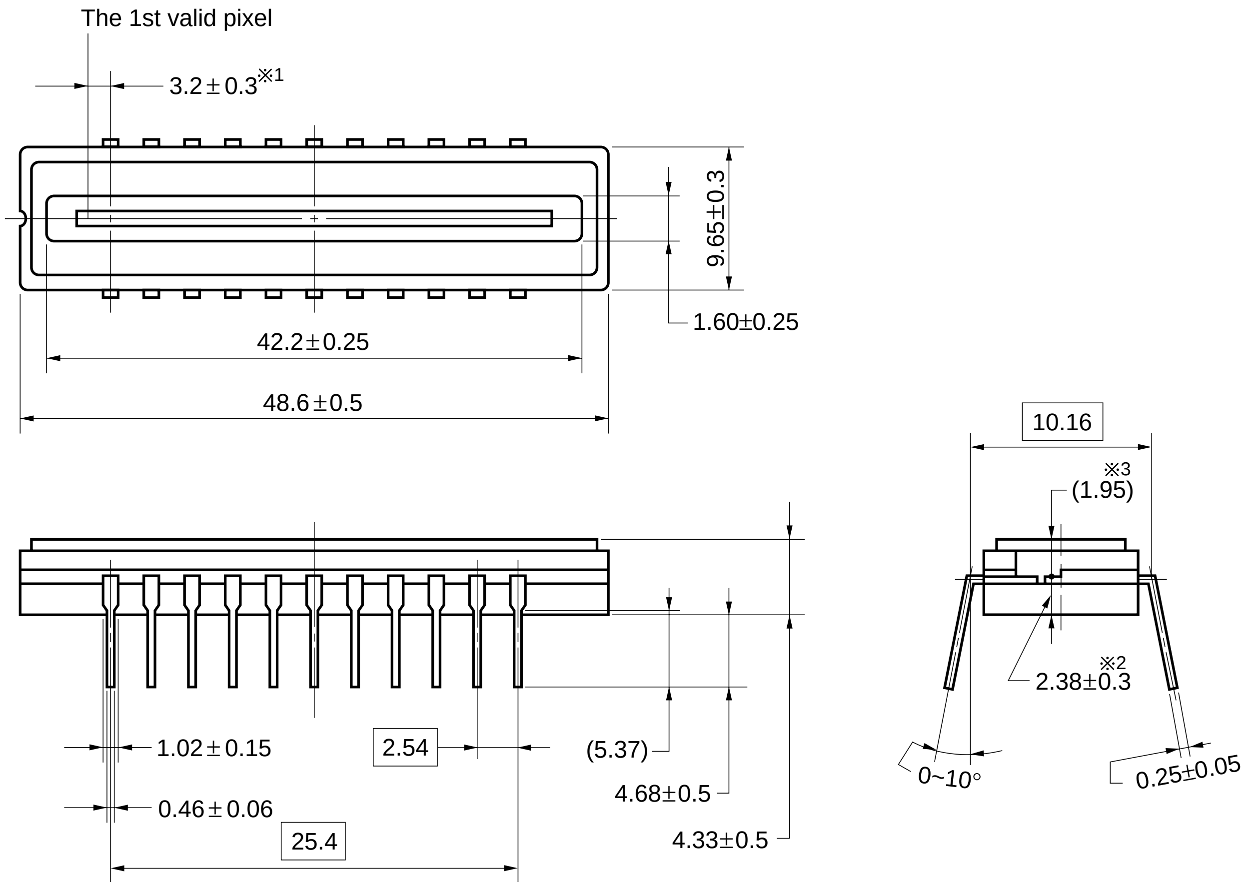
2. The inverters shown in the above application circuit example are the 74AC04.



PACKAGE DRAWING

CCD LINEAR IMAGE SENSOR 22-PIN CERAMIC DIP (CERDIP) (10.16 mm (400))

(Unit : mm)



Name	Dimensions	Refractive index
Glass cap	47.5×9.25×0.7	1.5

※1 1st valid pixel ←→ Center of pin 1
※2 Photosensitive surface of CCD chip ←→ Bottom of package
※3 Photosensitive surface of CCD chip ←→ Top of glass cap

22D-1CCD-PKG10

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

Type of Through-hole Device

μPD3747D : CCD linear image sensor 22-pin ceramic DIP (CERDIP) (10.16 mm (400))

Process	Conditions
Partial heating method	Pin temperature : 300°C or below, Heat time : 3 seconds or less (per pin)

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.