NEC

μPD411
μPD411-1
μPD411-2
μPD411-3
μPD411-4

FULLY DECODED RANDOM ACCESS MEMORY

3

DESCRIPTION

The μPD411 Family consists of six 4096 words by 1 bit dynamic N-channel MOS RAMs. They are designed for memory applications where very low cost and large bit storage are important design objectives. The μPD411 Family is designed using dynamic circuitry which reduces the standby power dissipation.

Reading information from the memory is a non-destructive. Refreshing is easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic high or a logic low.

FEATURES

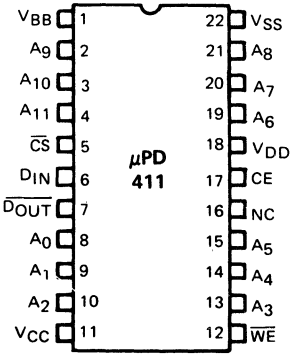
All of these products are guaranteed for operation over the 0 to 70°C temperature range.

Important features of the μPD411 family are:

- Low Standby Power
- 4096 words x 1 bit Organization
- A single low-capacitance high level clock input with solid ±1 volt margins.
- Inactive Power/0.3 mW (Typ.)
- Power Supply: +12, +5, -5V
- Easy System Interface
- TTL Compatible (Except CE)
- Address Registers on the Chip
- Simple Memory Expansion by Chip Select
- Three State Output and TTL Compatible
- 22 pin Ceramic Dual-in-Line Package
- Replacement for INTEL'S 2107B, TI'S 4060 and Equivalent Devices.
- 5 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	REFRESH TIME
μPD411	300 ns	470 ns	650 ns	2 ms
μPD411-1	250 ns	470 ns	640 ns	2 ms
μPD411-2	200 ns	400 ns	520 ns	2 ms
μPD411-3	150 ns	380 ns	470 ns	2 ms
μPD411-4	135 ns	320 ns	320 ns	2 ms

PIN CONFIGURATION



PIN NAMES

A_0 - A_{11}	Address Inputs
A_0 - A_5	Refresh Addresses
CE	Chip Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{WE}$	Write Enable
V_{DD}	Power (+12V)
V_{CC}	Power (+5V)
V_{SS}	Ground
V_{BB}	Power
NC	No Connection

FUNCTIONAL DESCRIPTION

CE Chip Enable

A single external clock input is required. All read, write, refresh and read-modify-write operations take place when chip enable input is high. When the chip enable is low, the memory is in the low power standby mode. No read/write operations can take place because the chip is automatically precharging.

$\overline{CS}$ Chip Select

The chip select terminal affects the data in, data out and read/write inputs. The data input and data output terminals are enabled when chip select is low. The chip select input must be low on or before the rising edge of the chip enable and can be driven from standard TTL circuits. A register for the chip select input is provided on the chip to reduce overhead and simplify system design.

$\overline{WE}$ Write Enable

The read or write mode is selected through the write enable input. A logic high on the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The $\overline{WE}$ terminal can be driven from standard TTL circuits. The data input is disabled when the read mode is selected.

A_0–A_{11} Addresses

All addresses must be stable on or before the rising edge of the chip enable pulse. All address inputs can be driven from standard TTL circuits. Address registers are provided on the chip to reduce overhead and simplify system design.

D_{IN} Data Input

Data is written during a write or read-modify-write cycle while the chip enable is high. The data in terminal can be driven from standard TTL circuits. There is no register on the data in terminal.

$\overline{D_{OUT}}$ Data Output

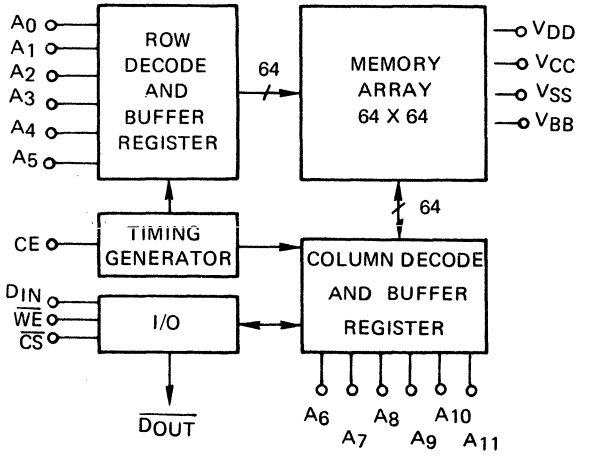
The three state output buffer provides direct TTL compatibility with a fan-out of two TTL gates. The output is in the high-impedance (floating) state when the chip enable is low or when the Chip Select input is high. Data output is inverted from data in.

Refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs A_0 through A_5 or by addressing every row within any 2-millisecond period. Addressing any row refreshes all 64 bits in that row.

The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, the chip select must be high.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

	μPD411 FAMILY (EXCEPT 411-4)	μPD411-4
Operating Temperature	0°C to +70°C	+10°C to +55°C
Storage Temperature	−55°C to +150°C	−55°C to +150°C
All Output Voltages	−0.3 to +20 Volts	−0.3 to +25 Volts ①
All Input Voltages	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Supply Voltage V_{DD}	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Supply Voltage V_{CC}	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Power Dissipation	1.0W	1.5W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V,
Except V_{DD} = +15V ±5% for 4114.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current	I_{LI}		0.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
CE Input Load Current	I_{LC}		0.01	10	μA	$V_{IN} = V_{ILC\ MIN}$ to $V_{IHC\ MAX}$
Output Leakage Current for High Impedance State	I_{LO}		0.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	$I_{DD\ OFF}$		20	200	μA	CE = 1.0V to 0.6V
V_{DD} Supply Current during CE on	$I_{DD\ ON}$		35 ⑤	60 ④	mA	CE = V_{IHC}, T_a = 25°C
Average V_{DD} Current						T_a = 25°C
μPD411	$I_{DD\ AV}$		37	60	mA	Cycle Time = 470 ns
μPD411-1	$I_{DD\ AV}$		37	60	mA	Cycle Time = 470 ns
μPD411-2	$I_{DD\ AV}$		37	60	mA	Cycle Time = 400 ns
μPD411-3	$I_{DD\ AV}$		41	65	mA	Cycle Time = 380 ns
μPD411-4	$I_{DD\ AV}$		55	80	mA	Cycle Time = 320 ns
V_{BB} Supply Current ②	I_{BB}		5	100	μA	
V_{CC} Supply Current during CE off ③	$I_{CC\ OFF}$		0.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
Input Low Voltage	V_{IL}	1.0		0.6	V	
Input High Voltage	V_{IH}	2.4		V_{CC}+1	V	
CE Input Low Voltage	V_{ILC}	1.0		0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD}−1	V_{DD}	V_{DD}+1	V	
Output Low Voltage	V_{OL}	0		0.40	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = 2.0 mA

Notes: ① Typical values are for T_a = 25°C and nominal power supply voltages.

② The I_{BB} current is the sum of all leakage current.

③ During CE on V_{CC} supply current is dependent on output loading.
V_{CC} is connected to output buffer only.

④ 65 mA for μPD411-3
80 mA for μPD411-4

⑤ 41 mA for μPD411-3
55 mA for μPD411-4

CAPACITANCE

T_a = 0° − 70°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address Capacitance, $\overline{CS}$	C_{AD}		4	6	pF	$V_{IN} = V_{SS}$
CE Capacitance	C_{CE}		18	27	pF	$V_{IN} = V_{SS}$
Data Output Capacitance	C_{OUT}		5	7	pF	V_{OUT} = 0V
D_{IN} and $\overline{WE}$ Capacitance	C_{IN}		8	10	pF	$V_{IN} = V_{SS}$

AC CHARACTERISTICS

READ CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS										UNIT
		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Time Between Refresh	t_{REF}		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		100		ns
CE Off Time	t_{CC}	130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	ns
Cycle Time	t_{CY}	470		470		400		380		320		ns
CE on Time	t_{CE}	300	3000	260	3000	230	3000	210	3000	200	3000	ns
CE Output Delay	t_{CO}		280		230		180		130		115	ns
Access Time	t_{ACC}		300		250		200		150		135	ns
CE to $\overline{WE}$	t_{WL}	40		40		40		40		40		ns
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		0		ns

WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS										UNIT
		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t_{CY}	470		470		400		380		320		ns
Time Between Refresh	t_{REF}		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		100		ns
CE Off Time	t_{CC}	130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	ns
CE on Time	t_{CE}	300	3000	260	3000	230	3000	210	3000	200	3000	ns
$\overline{WE}$ to CE off	t_W	180		180		150		150		65		ns
CE to $\overline{WE}$	t_{CW}	300		260		230		210		200		ns
D_{IN} to $\overline{WE}$ Set Up ①	t_{DW}	0		0		0		0		0		ns
D_{IN} Hold Time	t_{DH}	40		40		40		40		40		ns
$\overline{WE}$ Pulse Width	t_{WP}	180		180		150		100		65		ns

Note: ① If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.

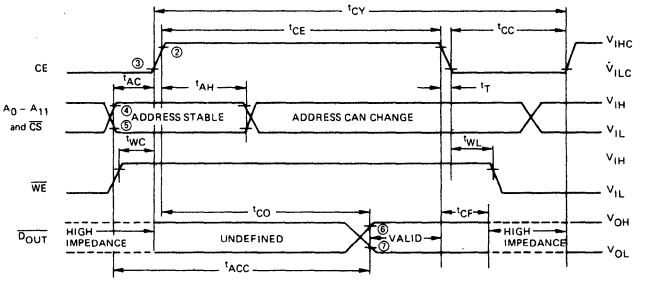
READ – MODIFY – WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = 5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS										UNIT
		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read–Modify–Write (RMW) Cycle Time	t_{RWC}	650		640		520		470		320		ns
Time Between Refresh	t_{REF}		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		100		ns
CE Off Time	t_{CC}	130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	ns
CE Width During RMW	t_{CRW}	480	3000	430	3000	350	3000	300	3000	200	3000	ns
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		0		ns
$\overline{WE}$ to CE off	t_W	180		180		150		150		65		ns
$\overline{WE}$ Pulse Width	t_{WP}	180		180		150		100		65		ns
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		0		0		ns
D_{IN} Hold Time	t_{DH}	40		40		40		40		40		ns
CE to Output Display	t_{CO}		280		230		180		130		115	ns
Access Time	t_{ACC}		300		250		200		150		135	ns

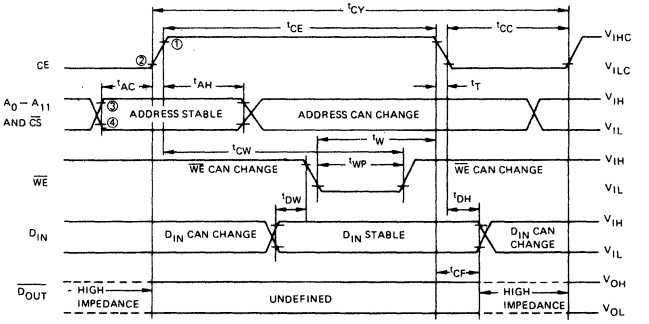
TIMING WAVEFORMS

READ CYCLE ①



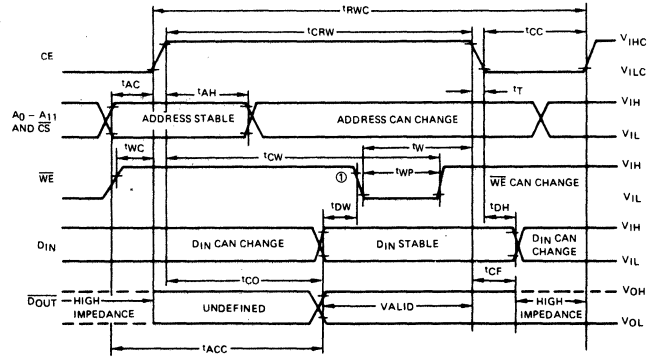
Notes ① For refresh cycle row and column addresses must be stable t_{AC} and remain stable for entire t_{AH} period.
② V_{DD} 2V is the reference level for measuring timing of CE.
③ V_{SS} +2V is the reference level for measuring timing of CE.
④ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
⑤ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}
⑥ V_{SS} +2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.
⑦ V_{SS} +0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$

WRITE CYCLE



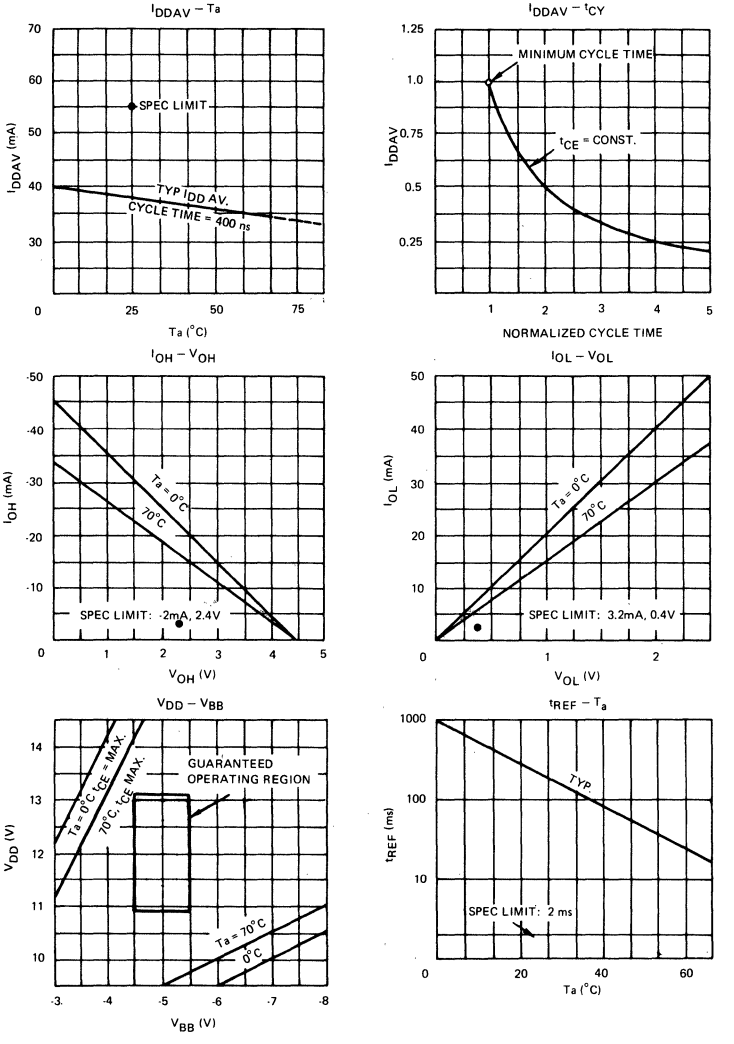
Notes ① V_{DD} -2V is the reference level for measuring timing of CE
② V_{SS} +2V is the reference level for measuring timing of CE.
③ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}
④ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

READ-MODIFY-WRITE CYCLE



Note ① $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

TYPICAL OPERATING CHARACTERISTICS (Except 411-4)



POWER CONSUMPTION

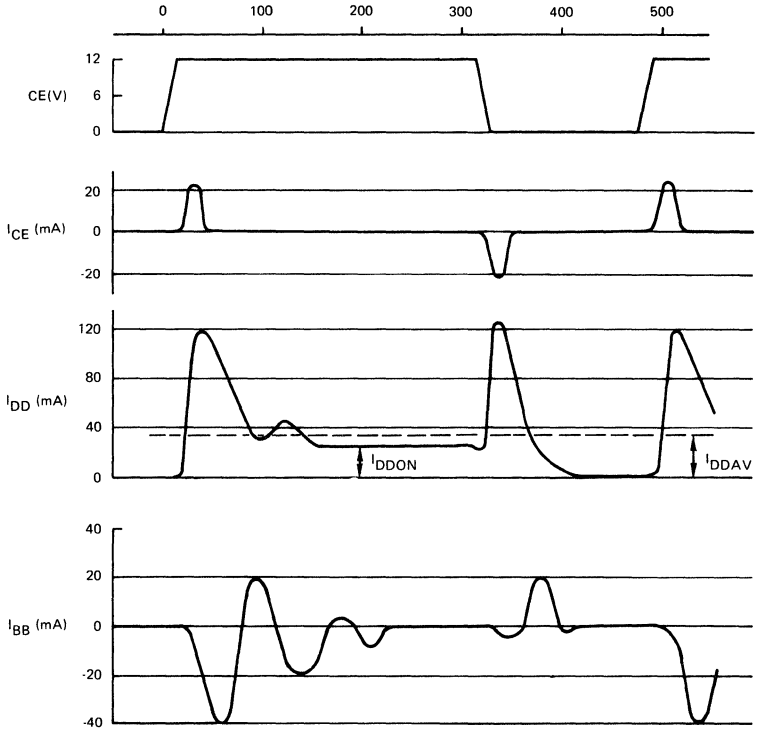
Power consumption = $V_{DD} \times I_{DDAV} + V_{BB} \times I_{BB}$.

Typical power dissiption for each product is shown below.

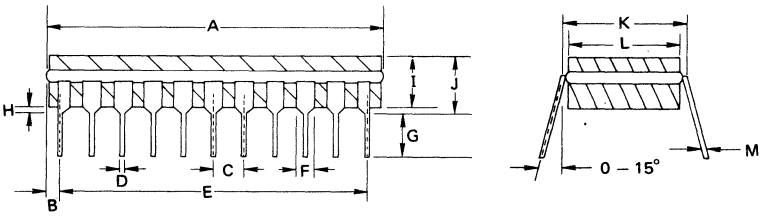
	mW (TYP.)	CONDITIONS
μPD411	450	Ta = 25° C, t_{cy} = 470ns, t_{CE} = 300ns
μPD411-1	450	Ta = 25° C, t_{cy} = 470ns, t_{CE} = 260ns
μPD411-2	450	Ta = 25° C, t_{cy} = 400ns, t_{CE} = 230ns
μPD411-3	550	Ta = 25° C, t_{cy} = 380ns, t_{CE} = 210ns
μPD411-4	660	Ta = 25° C, t_{cy} = 320ns, t_{CE} = 200ns

See above curves for power dissipation versus cycle time.

CURRENT WAVEFORMS



PACKAGE OUTLINE μPD411D



(Plastic)

ITEM	MILLIMETERS	INCHES
A	27.43 MAX	1.079 MAX
B	1.27 MAX	0.05 MAX
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 MAX	0.165 MAX
J	5.08 MAX	0.200 MAX
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009