NEC
NEC Electronics Inc.

μPD41257
262,144 x 1-BIT
DYNAMIC NMOS RAM

Description

The μPD41257 is a 262,144-word by 1-bit dynamic NMOS RAM designed to operate from a single +5-volt power supply. A double-polylayer N-channel silicon gate fabrication process provides for high storage cell density, high performance, and high reliability.The device also uses a single-transistor dynamic storage cell and advanced dynamic circuitry, including 1024 sense amplifiers, which ensure that power dissipation is minimized. The negative voltage substrate bias is automatically generated internally.

The three-state output is controlled by $\overline{\text{CAS}}$ independent of $\overline{\text{RAS}}$. Nibble mode read or write cycles are available by cycling $\overline{\text{CAS}}$.

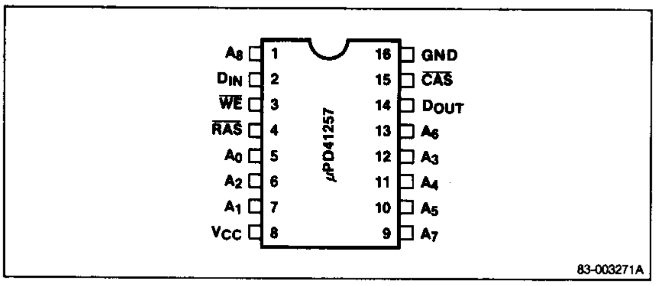
Refreshing is initiated by a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycle that enables internal generation of the refresh address. Refreshing is also accomplished by means of $\overline{\text{RAS}}$-only refresh cycles, hidden refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0-A_7 during a 4-ms period.

Features

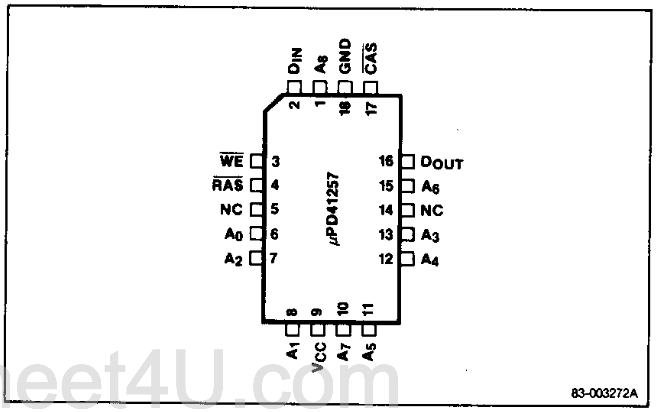
☐ 262,144-word x 1-bit organization
☐ Multiplexed address inputs
☐ Single +5-volt ±10% power supply
☐ Nibble read, write, or read-modify-write cycles
☐ $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ internal refreshing
☐ Low power dissipation
  — 28 mW max (standby)
  — 413 mW max (active, t_{RC} = 220 ns)
☐ Nonlatched, three-state output
☐ TTL-compatible inputs with low input capacitance
☐ 256-cycle/4-ms refresh period(A_0-A_7 are refresh addresses)
☐ High-density plastic DIP and PLCC packaging

Pin Configurations

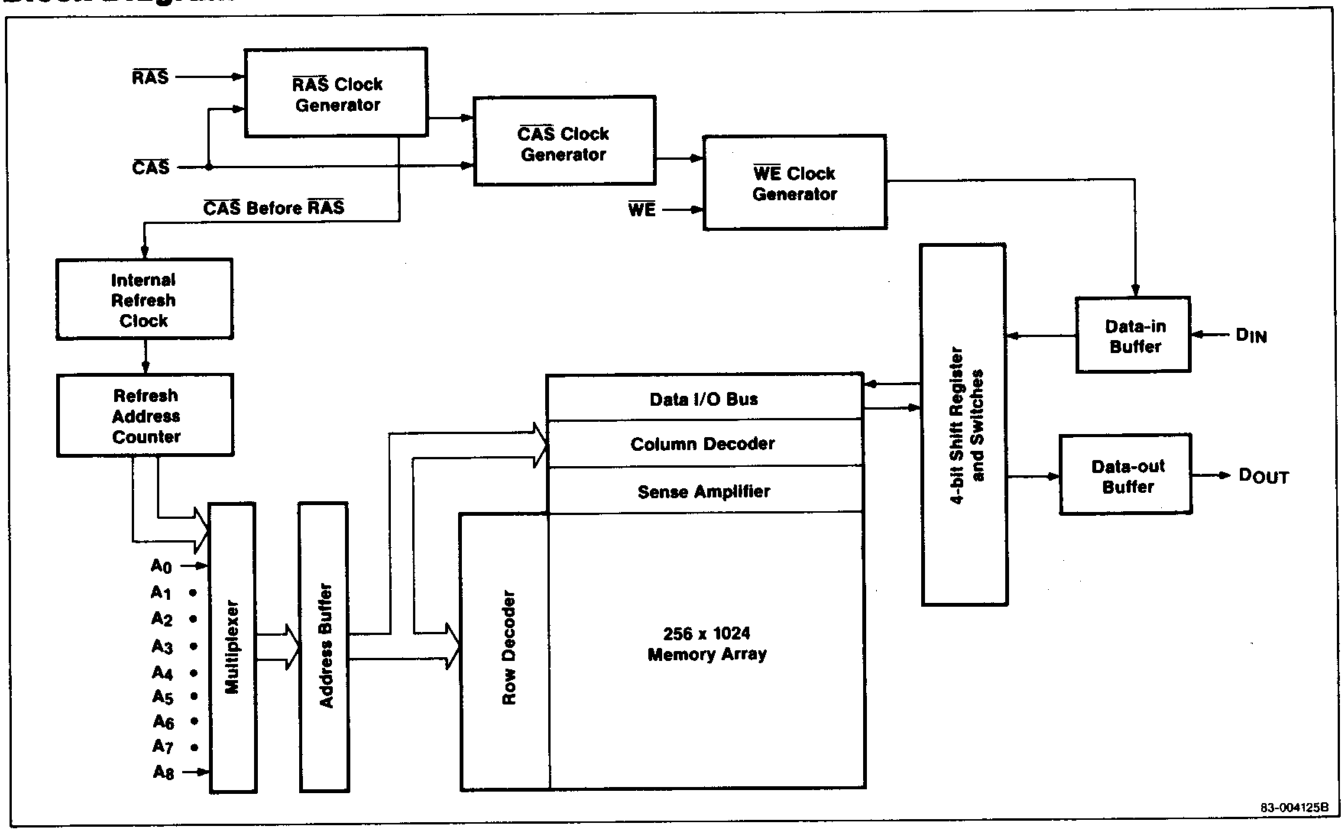
16-Pin Plastic DIP



18-Pin Plastic Leaded Chip Carrier (PLCC)



Block Diagram



Pin Identification

Symbol	Function
A_0-A_8	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{WE}$	Write enable
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
GND	Ground
V_{CC}	+5.0-volt power supply

Capacitance

$T_A = 0$ to $+70°C$; $V_{CC} = +5.0$ V ±10%

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_{I1}			5	pF	A_0-A_8, D_{IN}
	C_{I2}			8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_O			7	pF	D_{OUT}

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Short-circuit output current	50 mA
Power dissipation, P_D	1 W
Operating temperature, T_A	0 to +70°C
Storage temperature, T_{STG}	−55 to +150°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Ordering Information

Part Number	Access Time (max)	R/W Cycle (min)	Package
μPD41257C-12	120 ns	220 ns	16-pin plastic DIP
C-15	150 ns	260 ns	
C-20	200 ns	330 ns	
μPD41257L-12	120 ns	220 ns	18-pin PLCC
L-15	150 ns	260 ns	
L-20	200 ns	330 ns	

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$; GND = 0 V

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Standby power supply current	I_{CC2}			5	mA	$\overline{\text{RAS}} = V_{IH}$; D_{OUT} = high impedance
Input leakage current	$I_{I(L)}$	−10		10	μA	Any input V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, high	V_{OH}	2.4		V_{CC}	V	$I_{OUT} = -5$ mA
Output voltage, low	V_{OL}	0		0.4	V	$I_{OUT} = 4.2$ mA
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	GND	0	0	0	V	
Input voltage, high	V_{IH}	2.4		5.5	V	All inputs
Input voltage, low	V_{IL}	−1.0		0.8	V	All inputs

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

		Limits							
		μPD41257-12		μPD41257-15		μPD41257-20			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Standard Operation									
Average power supply operating current	I_{CC1}		75		70		60	mA	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Average power supply current, refresh cycle	I_{CC3}		60		55		55	mA	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}} = V_{IH}$; $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	220		260		330		ns	(Note 6)
Read-write cycle time	t_{RWC}	265		310		390		ns	(Note 6)
Access time from $\overline{\text{RAS}}$	t_{RAC}		120		150		200	ns	(Notes 7, 8)
Access time from $\overline{\text{CAS}}$	t_{CAC}		60		75		100	ns	(Notes 7, 9)
Output buffer turnoff delay	t_{OFF}	0	30	0	40	0	50	ns	(Note 10)
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{\text{RAS}}$ precharge time	t_{RP}	90		100		120		ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	120	10,000	150	10,000	200	10,000	ns	
$\overline{\text{RAS}}$ hold time	t_{RSH}	60		75		100		ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	60	10,000	75	10,000	100	10,000	ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	120		150		200		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	25	60	25	75	35	100	ns	(Note 11)
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{\text{CAS}}$ precharge time	t_{CPN}	30		30		35		ns	
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD41257-12		μPD41257-15		μPD41257-20		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Standard Operation (cont)									
Row address hold time	t_{RAH}	15		15		25		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	20		25		55		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	t_{AR}	80		100		155		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	10		10		25		ns	(Note 13)
Read command hold time referenced to $\overline{\text{CAS}}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		55		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	t_{WCR}	90		115		155		ns	
Write command pulse width	t_{WP}	20		25		55		ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	40		45		55		ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	40		45		55		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		55		ns	(Note 14)
Data-in hold time referenced to $\overline{\text{RAS}}$	t_{DHR}	90		115		155		ns	
Refresh period	t_{REF}		4		4		4	ms	
$\overline{\text{WE}}$ command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay	t_{CWD}	60		75		100		ns	(Note 15)
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay	t_{RWD}	120		150		200		ns	(Note 15)
Nibble Mode									
Average power supply current, nibble mode	I_{CC6}		35		27		27	mA	$\overline{\text{RAS}} = V_{IL}$; $\overline{\text{CAS}}$ cycling; $t_{NC} = t_{NC}$ min (Note 5)
Nibble-mode cycle time	t_{NC}	60		70		100		ns	(Note 6)
Nibble-mode access time	t_{NAC}		30		35		50	ns	(Note 7)
Nibble-mode precharge time	t_{NP}	20		25		40		ns	
Nibble-mode $\overline{\text{WE}}$ pulse width	t_{NWP}	20		25		40		ns	
Nibble-mode $\overline{\text{CAS}}$ pulse width	t_{NAS}	30		35		50		ns	
Nibble-mode $\overline{\text{RAS}}$ hold time (read cycle)	t_{NRRSH}	30		35		50		ns	
Nibble-mode $\overline{\text{RAS}}$ hold time (write cycle)	t_{NWRSH}	35		35		50		ns	
Nibble-mode $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay	t_{NCWD}	30		35		50		ns	
Nibble-mode $\overline{\text{WE}}$ to $\overline{\text{CAS}}$ lead time	t_{NCWL}	30		35		50		ns	

AC Characteristics (cont)

Parameter	Symbol	µPD41257-12		µPD41257-15		µPD41257-20		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle									
Average power supply current, $\overline{CAS}$ before $\overline{RAS}$ refreshing	I_{CC4}		65		60		55	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IL}$; $t_{RC} = t_{RC}$ min (Note 5)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	25		30		30		ns	
Read or write cycle time (counter test cycle)	t_{TRC}	245		285		350		ns	
Read-write cycle time (counter test cycle)	t_{TRWC}	290		335		410		ns	
$\overline{CAS}$ precharge time (counter test cycle)	t_{TCP}	50		60		80		ns	

Notes:

(1) An initial pause of 100 µs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(2) Ac measurements assume $t_T = 5$ ns.

(3) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(4) All voltages are referenced to GND.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on output loading and cycle rates. Specified values are obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70°C$) is assured.

(7) Load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown. For the $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle, t_{RAC} is specified as $t_{RAC} = t_{CHR} + t_{TCP} + t_{CAC} + 2t_T$ and is greater than the maximum specified value shown in this table.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. Time t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, t_{NCWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only.

If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle or a nibble mode early write cycle and the data output pin will remain open-circuit throughout the entire cycle.

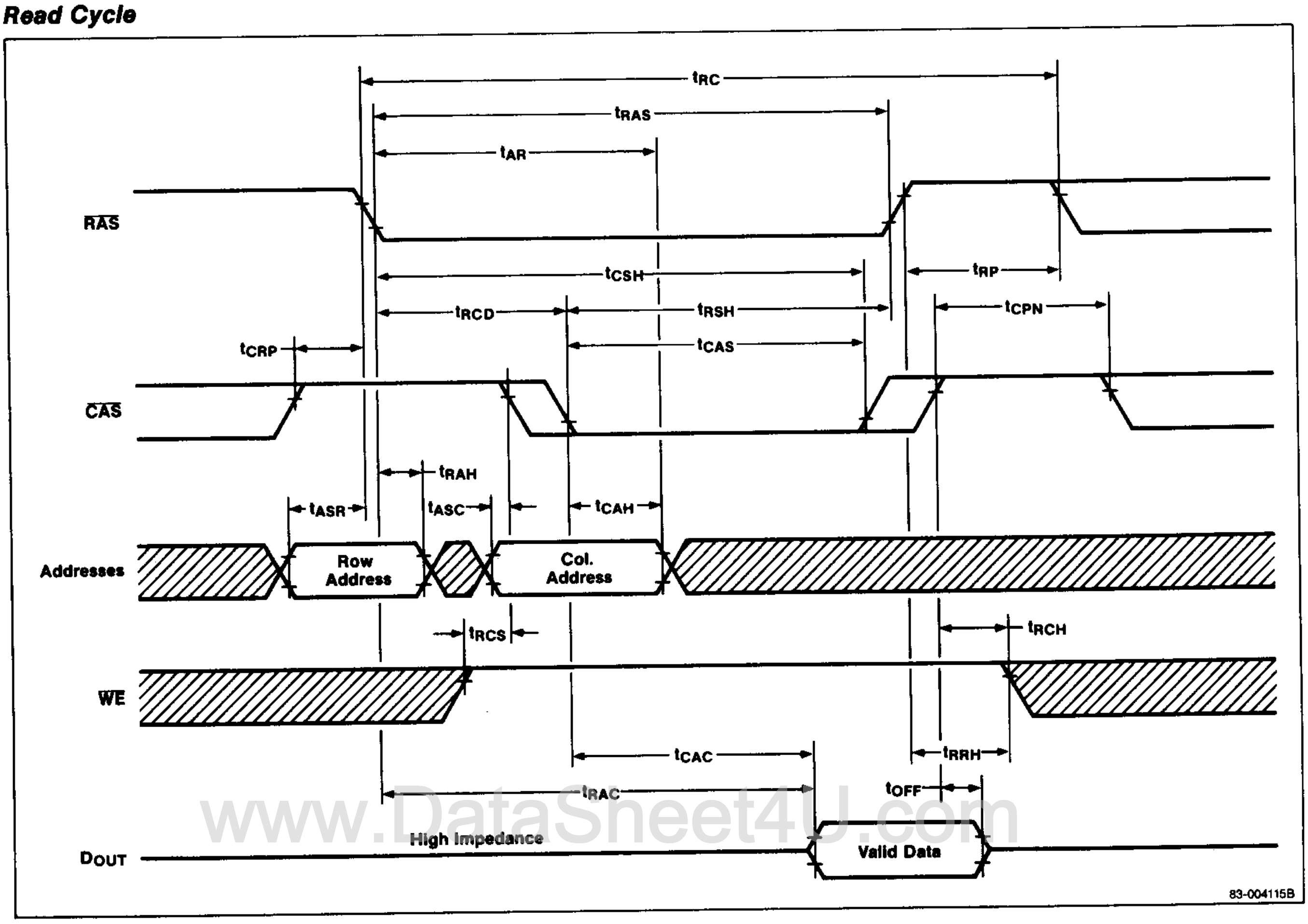
If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output pin will contain data read from the selected cell.

If $t_{NCWD} \geq t_{NCWD}$ (min), the cycle is a nibble mode read-write cycle and the data output pin will contain data read from the selected cell.

If none of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

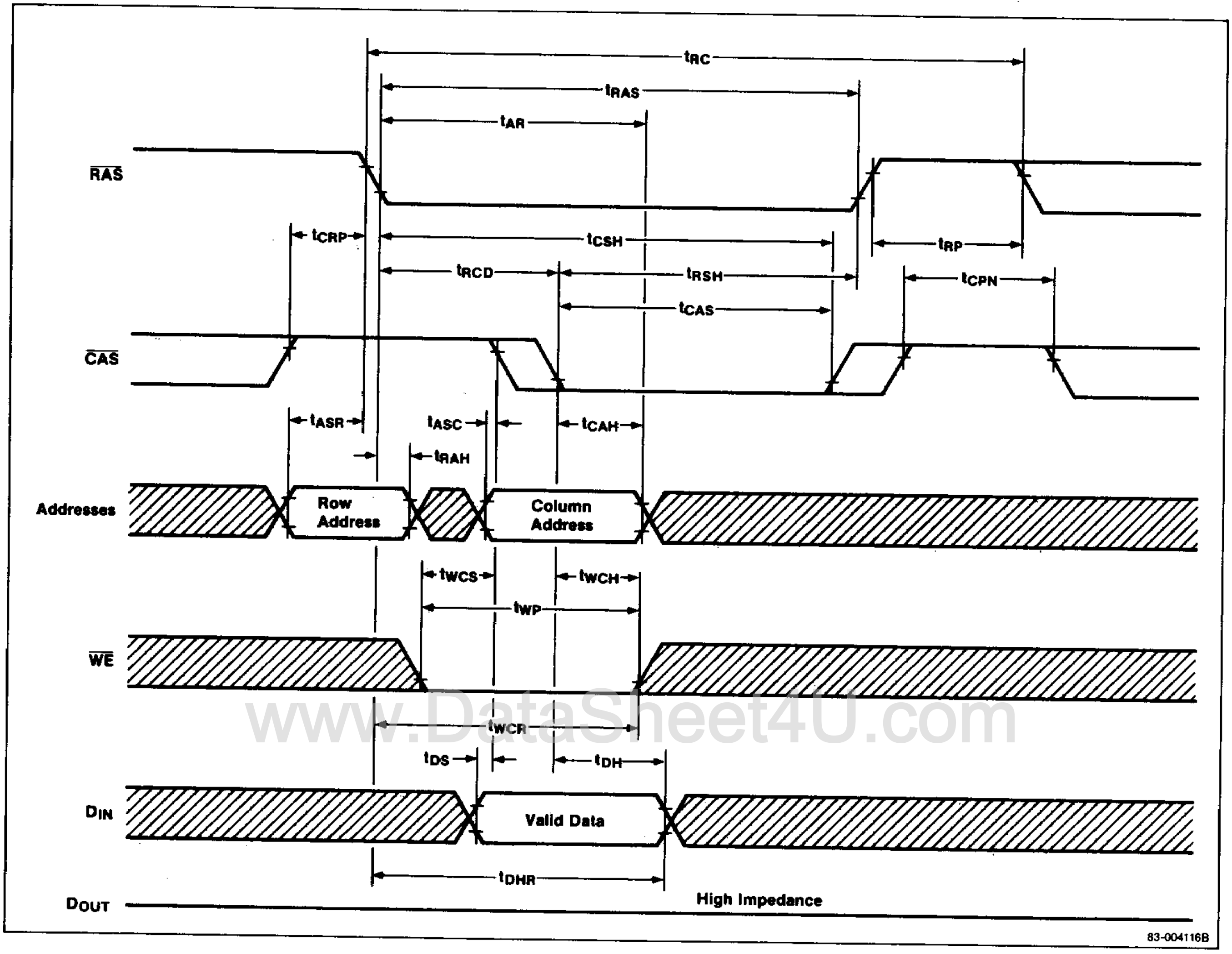
Timing Waveforms

Read Cycle



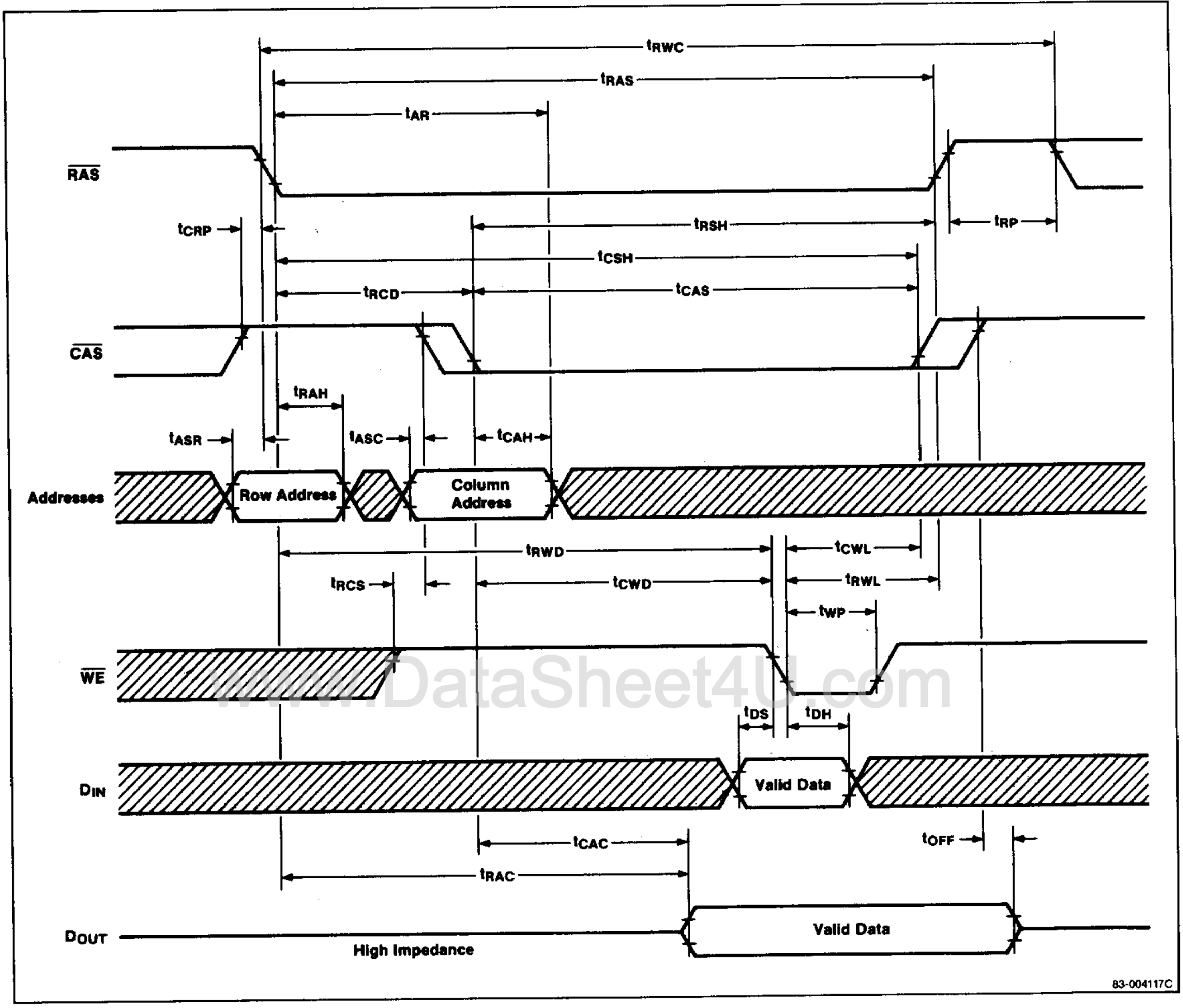
Timing Waveforms (cont)

Write Cycle (Early Write)



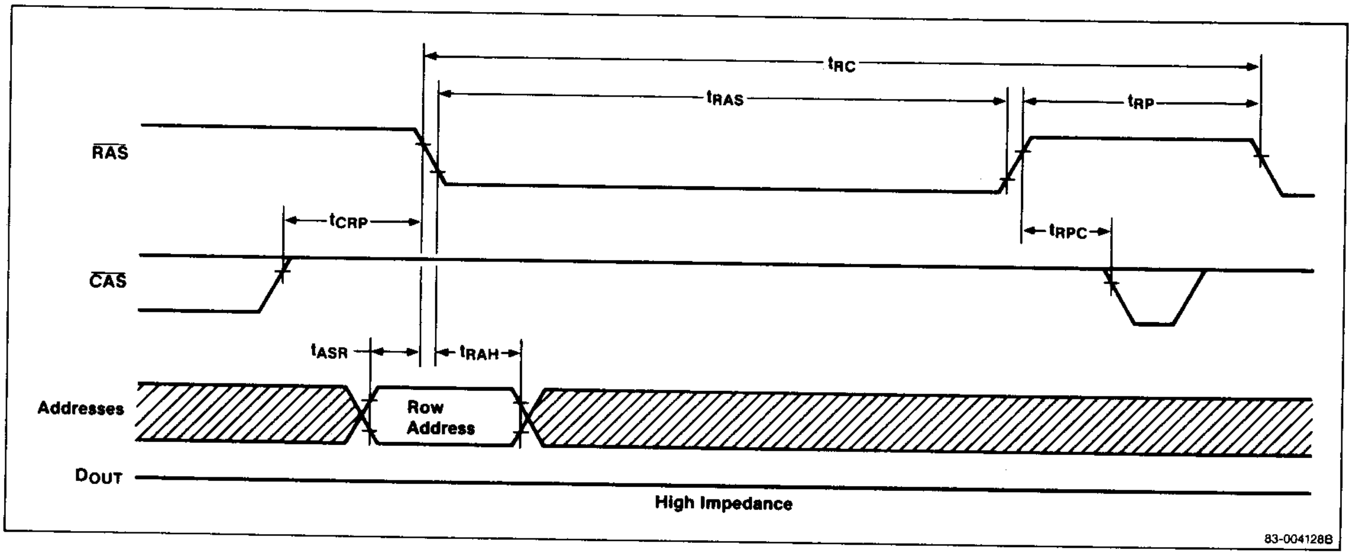
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle

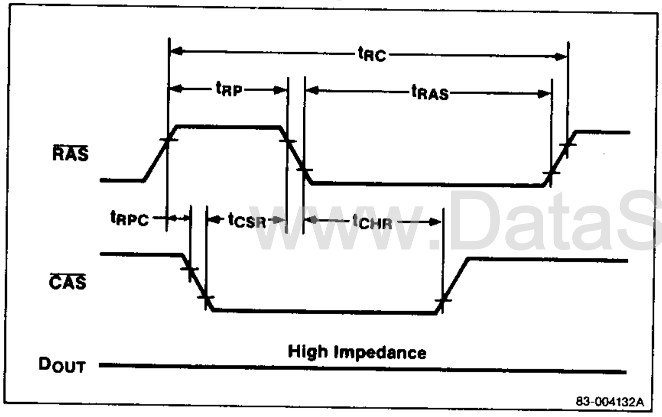


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle

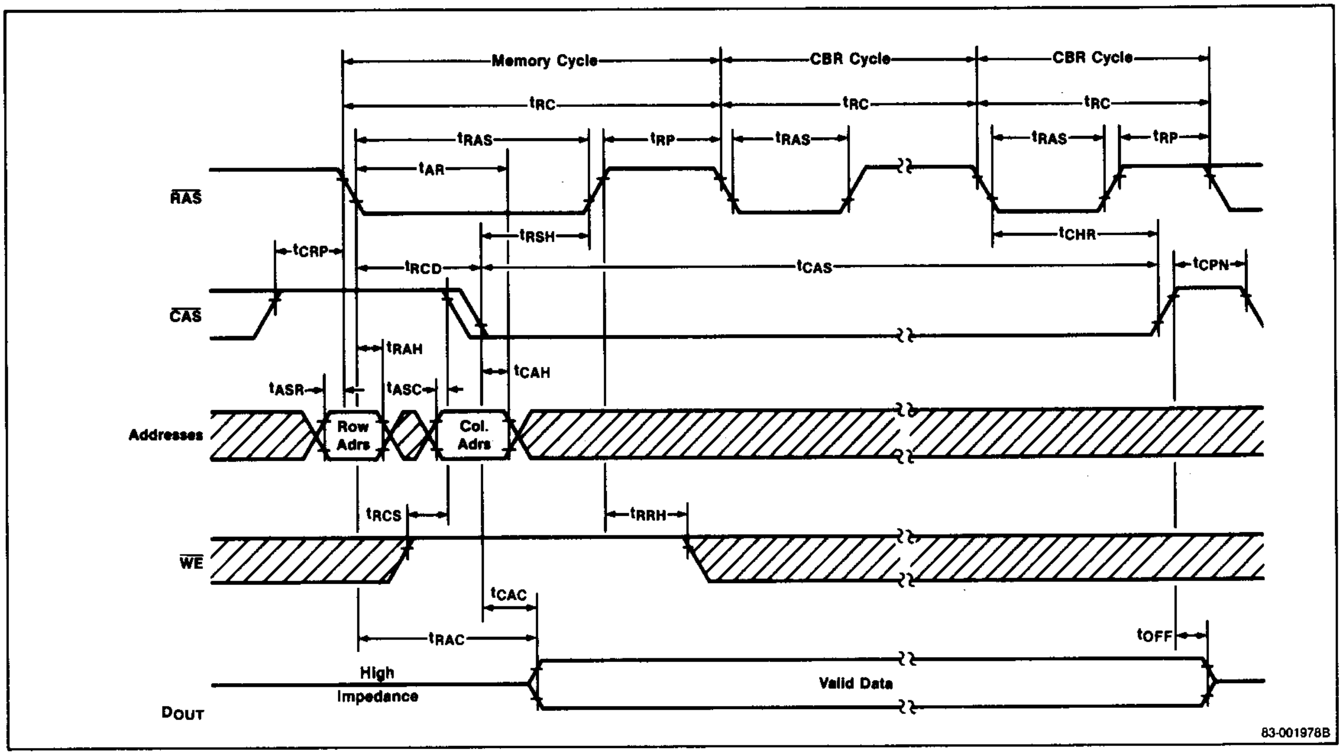


$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



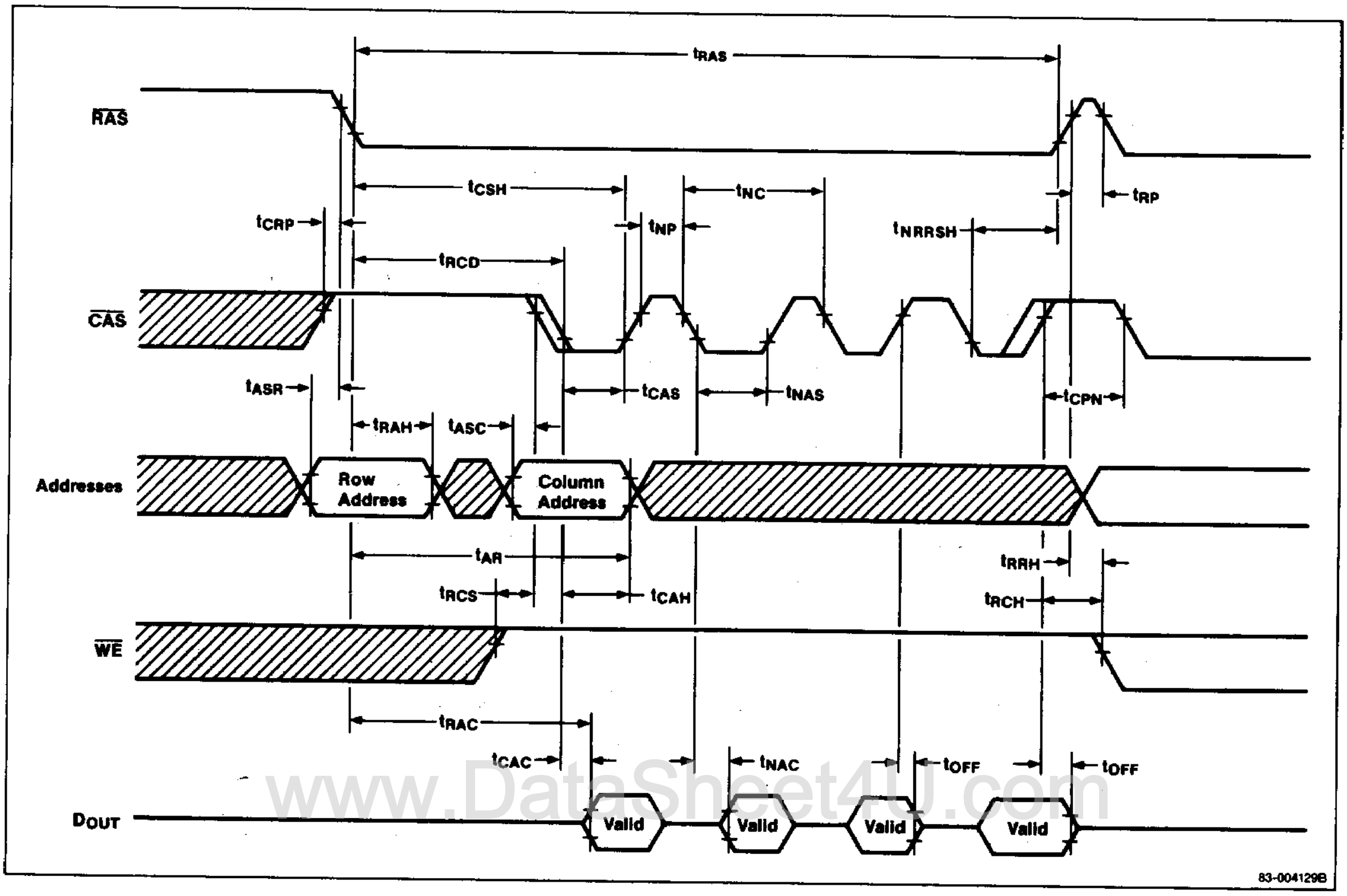
Nibble Mode

The μPD41257 is capable of executing nibble read, write, or read-modify-write cycles. Nibble mode allows high-speed serial access of a maximum of 4 data bits. The first bit is determined by the row and column addresses, and the next bits are accessed automatically by cycling $\overline{\text{CAS}}$ while $\overline{\text{RAS}}$ is held low. The addresses of nibble bits are determined by the combination of row address A_8 and column address A_8 in the following sequence.

		Row Address									Column Address									
Sequence	Nibble Bit	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Comment
$\overline{\text{RAS}}/\overline{\text{CAS}}$	1	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0	0	0	Example: external address input
$\overline{\text{CAS}}$ cycling	2	1	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0	0	0	Internal address generated
$\overline{\text{CAS}}$ cycling	3	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0	0	0	
$\overline{\text{CAS}}$ cycling	4	1	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0	0	0	
$\overline{\text{CAS}}$ cycling	1	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0	0	0	Repeated sequence

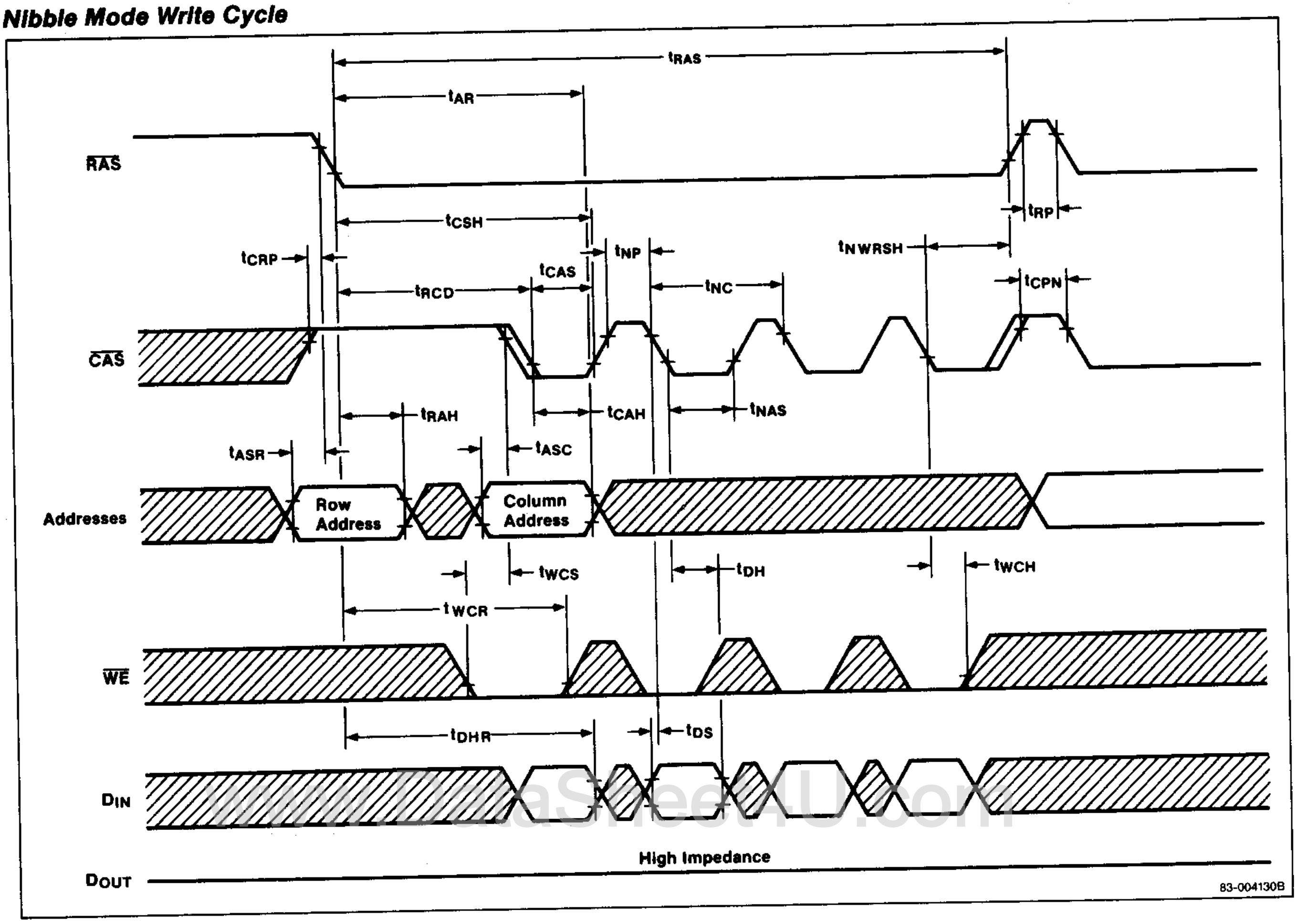
Timing Waveforms (cont)

Nibble Mode Read Cycle



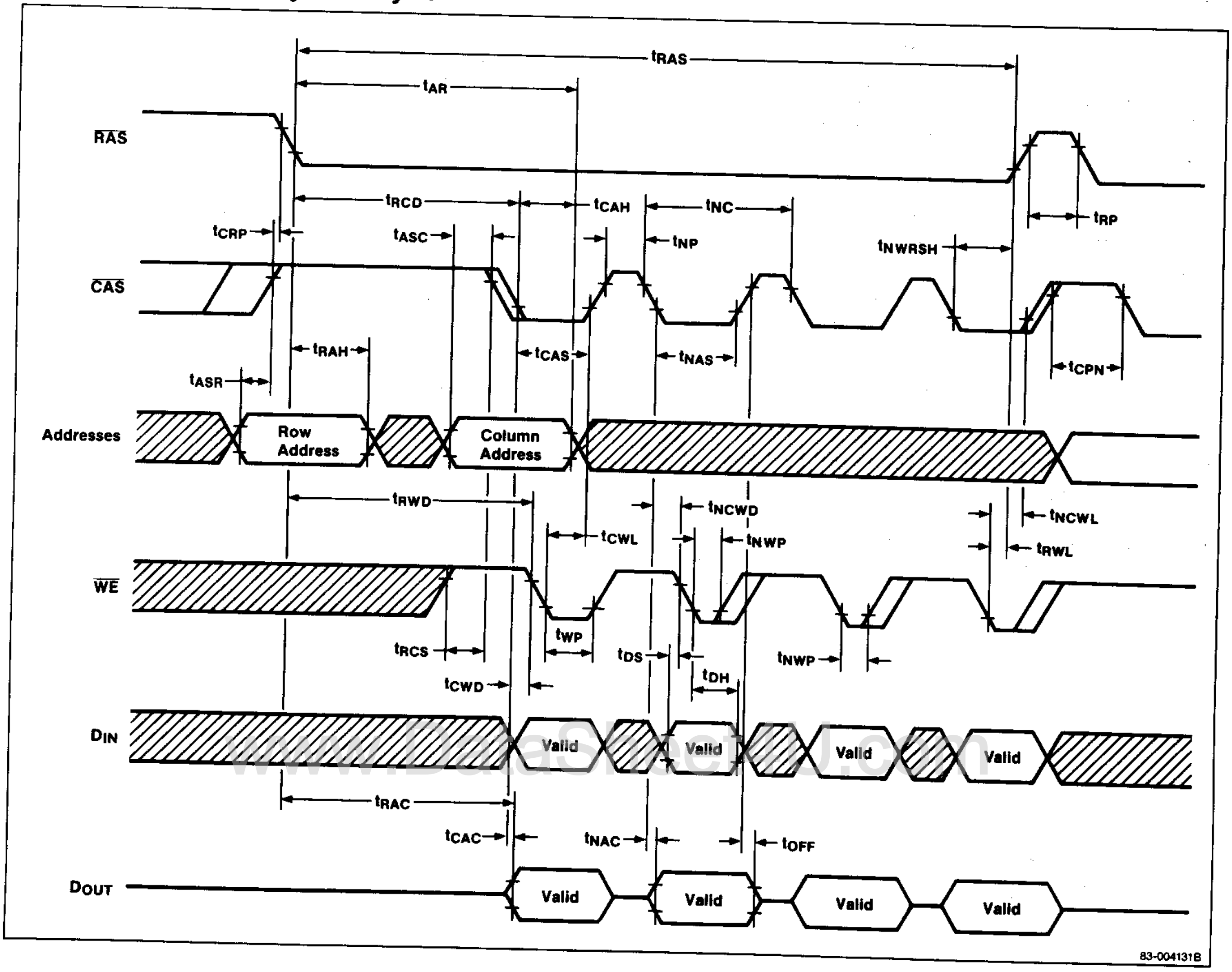
Timing Waveforms (cont)

Nibble Mode Write Cycle



Timing Waveforms (cont)

Nibble Mode Read-Modify-Write Cycle



Timing Waveforms (cont)

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Counter Test

The $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter functionality is verified by using the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle. After $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh operation, $\overline{\text{CAS}}$ goes to a high level (after prescribed time t_{CHR}) and then goes to a low level (after prescribed time t_{TCP}) while $\overline{\text{RAS}}$ is held at a low level. The read, write, and read-modify-write operations are enabled as shown in the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test timing diagrams. A row address is defined by the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh internal address counter, and a column address is defined by latching the external address at the second falling edge of $\overline{\text{CAS}}$.

Suggested $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test pattern:

(1) Initialize the internal refresh counter using 8 $\overline{\text{RAS}}$-only refresh cycles after power-on.

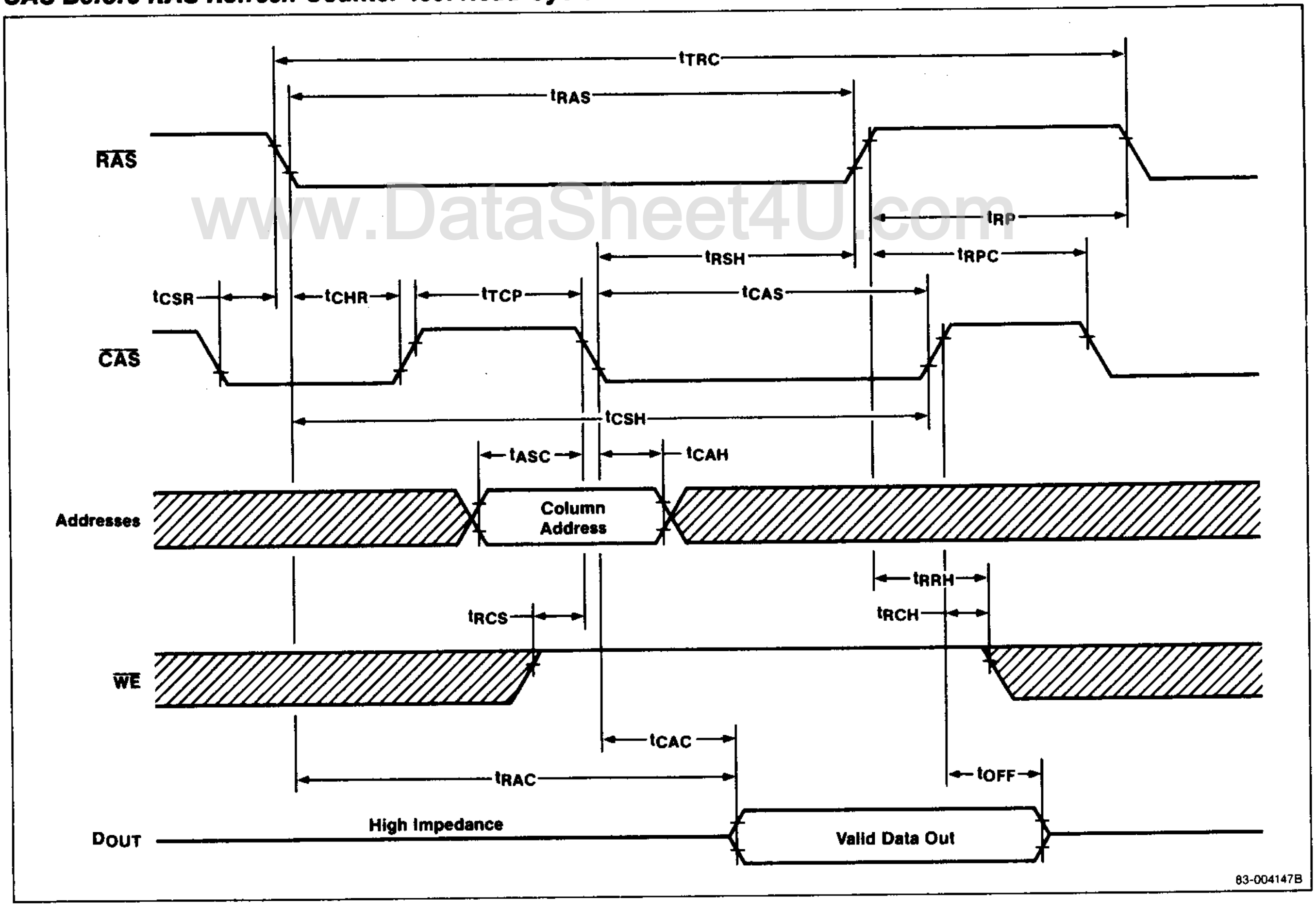
(2) Write a test pattern of zeros into 256 memory cells at a single fixed column address using 256 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test write cycles.

(3) Using the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test read-modify-write cycle, read the "0" previously written during operation (2) and write a new "1" in the same cycle. Repeat this 256 times to write a pattern of ones into the 256 memory cells.

(4) Read the "1" written in operation (3) using the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test read cycle.

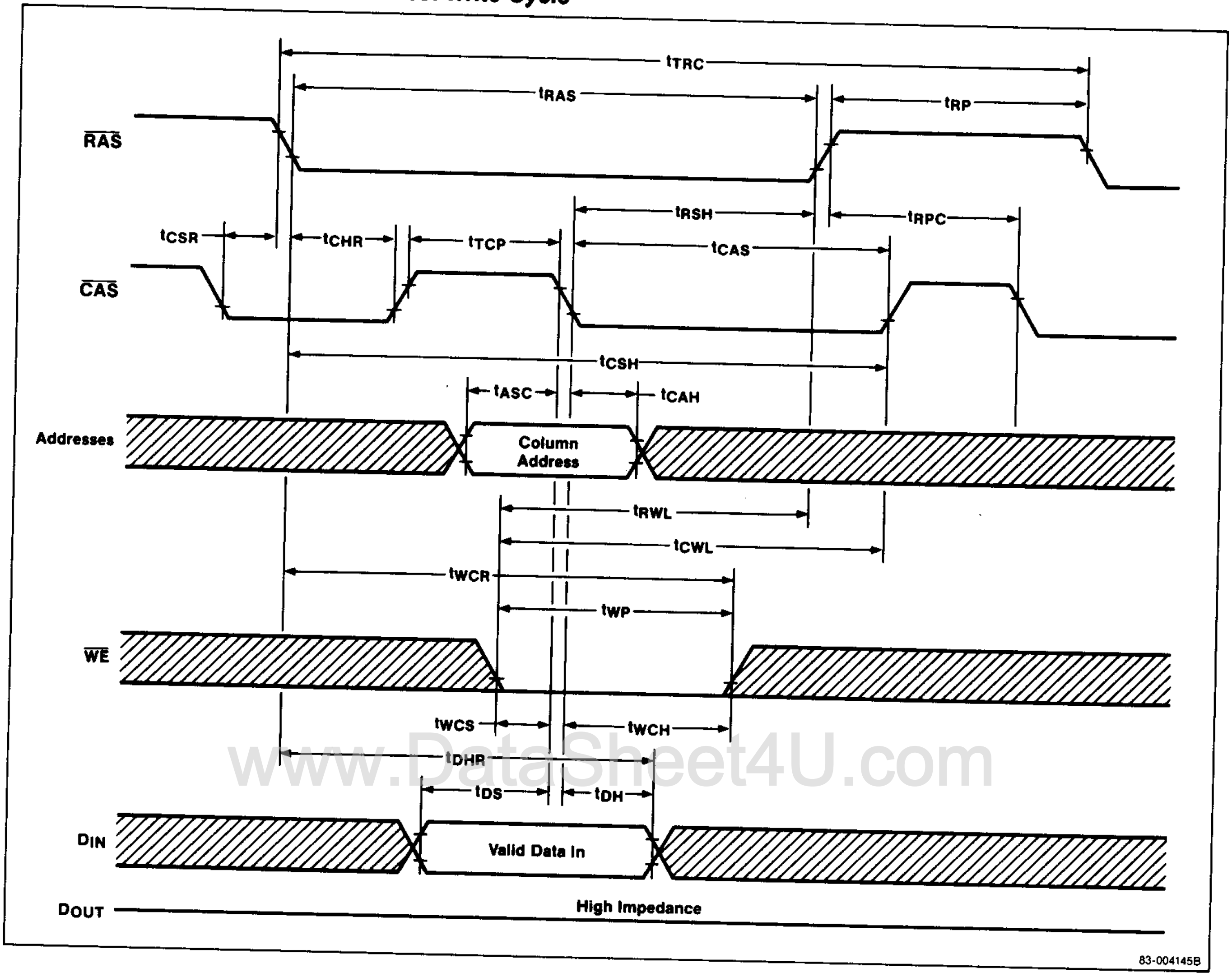
(5) Complement the test pattern data and repeat operations (2), (3), and (4).

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Counter Test Read Cycle



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Write Cycle



Timing Waveforms (cont)

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Counter Test Read-Modify-Write Cycle