

## Description

The μPD41416 is a 16,384-word by 4-bit dynamic N-channel MOS RAM designed to operate from a single +5 V power supply. The negative voltage substrate bias is internally generated; its operation is both automatic and transparent. The μPD41416 utilizes a double-polylayer, N-channel, silicon gate process which provides high storage cell density, high performance, and high reliability.

The μPD41416 uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, ensuring minimum power dissipation. Refresh is accomplished by performing RAS-only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 128 address combinations of A<sub>0</sub>-A<sub>6</sub> during the refresh period of 2 milliseconds.

Multiplexed address inputs permit the μPD41416 to be packaged in a standard 18-pin dual-in-line package for high system bit density.

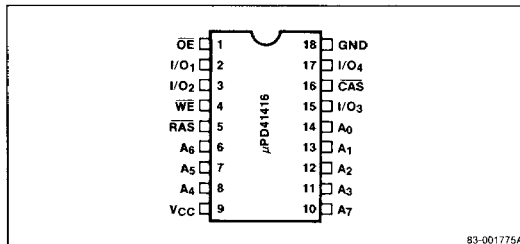
## Features

- ☐ 16,384-word × 4-bit organization
- ☐ Single +5 V power supply ±10%
- ☐ Standard 18-pin plastic package
- ☐ CAS, OE or early write mode to control D<sub>OUT</sub> buffer impedance
- ☐ Low power dissipation,
  - Active (t<sub>RC</sub> = min): 303 mW
  - Standby: 28 mW
- ☐ Read, write, read-write, read-modify-write. RAS-only refresh, hidden refresh, and page mode capabilities
- ☐ 128 refresh cycles during 2 ms period

## Performance Ranges

| Device      | t <sub>RAC</sub> | t <sub>CAC</sub> | t <sub>OEA</sub> |
|-------------|------------------|------------------|------------------|
| μPD41416-12 | 120 ns           | 60 ns            | 30 ns            |
| μPD41416-15 | 150 ns           | 75 ns            | 40 ns            |
| μPD41416-20 | 200 ns           | 100 ns           | 50 ns            |

## Pin Configuration



## Pin Identification

| No.         | Symbol                             | Function                                                                                                                                                                             |
|-------------|------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1           | OE                                 | Output enable                                                                                                                                                                        |
| 2-3, 15, 17 | I/O <sub>1</sub> -I/O <sub>4</sub> | Data input/output                                                                                                                                                                    |
| 4           | WE                                 | Write enable                                                                                                                                                                         |
| 5           | RAS                                | Row address strobe                                                                                                                                                                   |
| 6-8, 10-14  | A <sub>0</sub> -A <sub>7</sub>     | Address inputs:<br>A <sub>0</sub> -A <sub>5</sub> = Column address inputs<br>A <sub>0</sub> -A <sub>6</sub> = Refresh address<br>A <sub>0</sub> -A <sub>7</sub> = Row address inputs |
| 9           | V <sub>CC</sub>                    | +5 V power supply                                                                                                                                                                    |
| 16          | CAS                                | Column address strobe                                                                                                                                                                |
| 18          | GND                                | Ground                                                                                                                                                                               |



**AC Characteristics (Notes 2, 3, 4)** $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$  (Note 1)

| Parameter                                              | Symbol           | Limits      |        |             |        |             |        | Unit | Test Conditions                                                                      |
|--------------------------------------------------------|------------------|-------------|--------|-------------|--------|-------------|--------|------|--------------------------------------------------------------------------------------|
|                                                        |                  | μPD41416-12 |        | μPD41416-15 |        | μPD41416-20 |        |      |                                                                                      |
|                                                        |                  | Min         | Max    | Min         | Max    | Min         | Max    |      |                                                                                      |
| Operating supply current, average                      | I <sub>CC1</sub> |             | 55     |             | 50     |             | 45     | mA   | RAS, CAS cycling, t <sub>RC</sub> = t <sub>RC min.</sub> (Note 5)                    |
| Operating supply current, refresh mode, average        | I <sub>CC3</sub> |             | 45     |             | 40     |             | 35     | mA   | RAS cycling, CAS = V <sub>IH</sub> , t <sub>RC</sub> = t <sub>RC min.</sub> (Note 5) |
| Operating supply current, page mode operation, average | I <sub>CC4</sub> |             | 45     |             | 40     |             | 35     | mA   | RAS = V <sub>IL</sub> , CAS cycling, t <sub>PC</sub> = t <sub>PC min.</sub> (Note 5) |
| Random read or write cycle time                        | t <sub>RC</sub>  | 220         |        | 260         |        | 330         |        | ns   | (Note 6)                                                                             |
| Read-write cycle time                                  | t <sub>RWC</sub> | 300         |        | 355         |        | 445         |        | ns   | (Note 6)                                                                             |
| Page mode cycle time                                   | t <sub>PC</sub>  | 120         |        | 145         |        | 180         |        | ns   | (Note 6)                                                                             |
| Access time from RAS                                   | t <sub>RAC</sub> |             | 120    |             | 150    |             | 200    | ns   | (Notes 7, 8)                                                                         |
| Access time from CAS                                   | t <sub>CAC</sub> |             | 60     |             | 75     |             | 100    | ns   | (Notes 7, 9)                                                                         |
| Output turn-off delay from CAS                         | t <sub>OFF</sub> | 0           | 30     | 0           | 40     | 0           | 50     | ns   | (Note 10)                                                                            |
| Transition time, rise and fall                         | t <sub>T</sub>   | 3           | 50     | 3           | 50     | 3           | 50     | ns   | (Note 4)                                                                             |
| RAS precharge time                                     | t <sub>RP</sub>  |             | 90     |             | 100    |             | 120    | ns   |                                                                                      |
| RAS pulse width                                        | t <sub>RAS</sub> | 120         | 10,000 | 150         | 10,000 | 200         | 10,000 | ns   |                                                                                      |
| RAS hold time                                          | t <sub>RSH</sub> | 60          |        | 75          |        | 100         |        | ns   |                                                                                      |
| CAS pulse width                                        | t <sub>CAS</sub> | 60          | 10,000 | 75          | 10,000 | 100         | 10,000 | ns   |                                                                                      |
| CAS hold time                                          | t <sub>CSH</sub> | 120         |        | 150         |        | 200         |        | ns   |                                                                                      |
| RAS to CAS delay time                                  | t <sub>RCD</sub> | 25          | 60     | 25          | 75     | 30          | 100    | ns   | (Note 11)                                                                            |
| CAS to RAS precharge time                              | t <sub>CRP</sub> | 0           |        | 0           |        | 0           |        | ns   | (Note 12)                                                                            |
| CAS precharge time, non-page cycle                     | t <sub>CPN</sub> | 25          |        | 25          |        | 30          |        | ns   |                                                                                      |
| CAS precharge time, page cycle                         | t <sub>CP</sub>  | 50          |        | 60          |        | 70          |        | ns   |                                                                                      |
| RAS precharge, CAS hold time                           | t <sub>RPC</sub> | 0           |        | 0           |        | 0           |        | ns   |                                                                                      |
| Row address setup time                                 | t <sub>ASR</sub> | 0           |        | 0           |        | 0           |        | ns   |                                                                                      |
| Row address hold time                                  | t <sub>RAH</sub> | 15          |        | 15          |        | 20          |        | ns   |                                                                                      |
| Column address setup time                              | t <sub>ASC</sub> | 0           |        | 0           |        | 0           |        | ns   |                                                                                      |
| Column address hold time                               | t <sub>CAH</sub> | 20          |        | 25          |        | 30          |        | ns   |                                                                                      |
| Column address hold time referenced to RAS             | t <sub>AR</sub>  | 80          |        | 100         |        | 130         |        | ns   |                                                                                      |
| Read command setup time                                | t <sub>RCS</sub> | 0           |        | 0           |        | 0           |        | ns   |                                                                                      |
| Read command hold time referenced to RAS               | t <sub>RRH</sub> | 20          |        | 20          |        | 20          |        | ns   | (Note 13)                                                                            |
| Read command hold time referenced to CAS               | t <sub>RCH</sub> | 0           |        | 0           |        | 0           |        | ns   | (Note 13)                                                                            |
| Write command hold time                                | t <sub>WCH</sub> | 35          |        | 45          |        | 55          |        | ns   |                                                                                      |
| Write command hold time referenced to RAS              | t <sub>WCR</sub> | 95          |        | 120         |        | 155         |        | ns   |                                                                                      |
| Write command pulse width                              | t <sub>WP</sub>  | 35          |        | 45          |        | 55          |        | ns   |                                                                                      |
| Write command to RAS lead time                         | t <sub>RWL</sub> | 40          |        | 45          |        | 55          |        | ns   |                                                                                      |
| Write command to CAS lead time                         | t <sub>CWL</sub> | 40          |        | 45          |        | 55          |        | ns   |                                                                                      |
| Data-in setup time                                     | t <sub>DS</sub>  | 0           |        | 0           |        | 0           |        | ns   | (Note 14)                                                                            |

## μPD41416

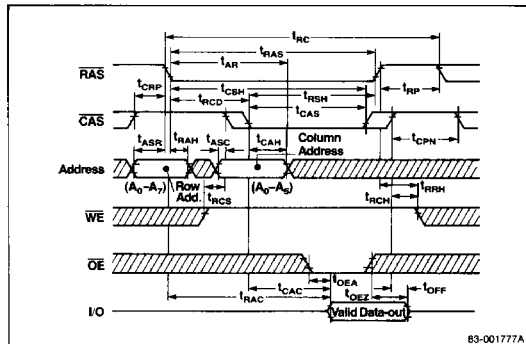
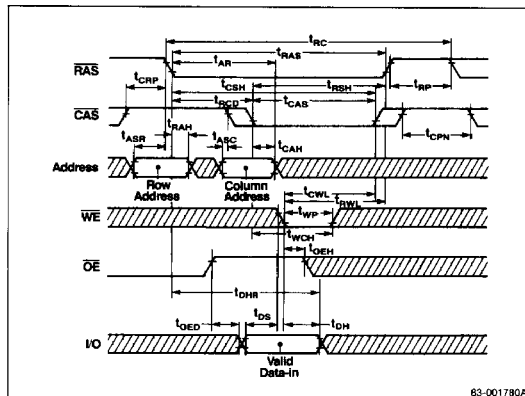
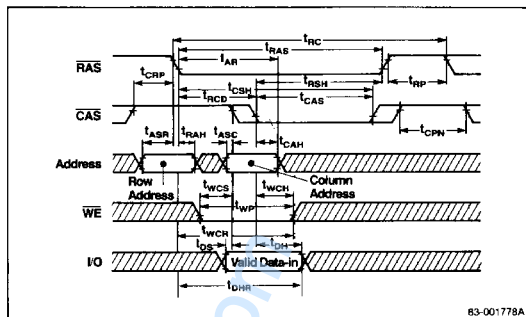
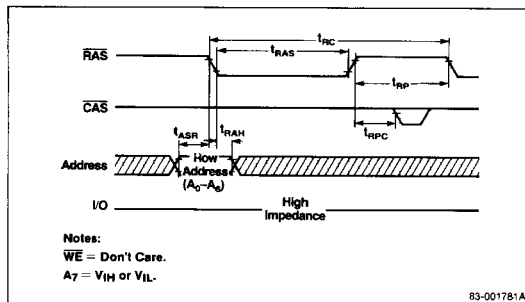
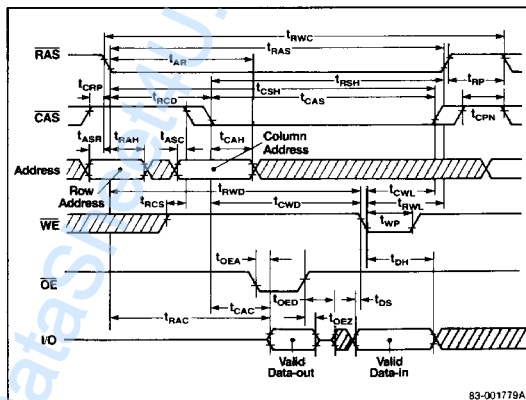
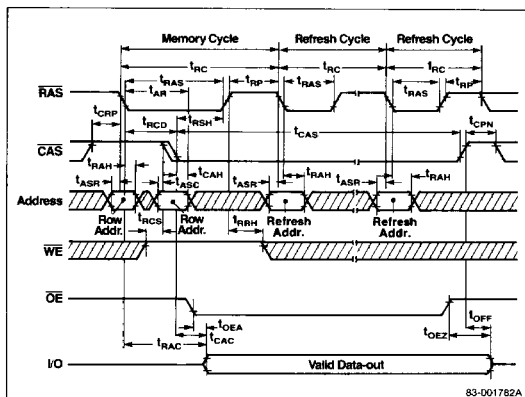
### AC Characteristics (Notes 2, 3, 4) (cont)

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$  (Note 1)

| Parameter                           | Symbol           | Limits      |     |             |     |             |     | Unit | Test Conditions |
|-------------------------------------|------------------|-------------|-----|-------------|-----|-------------|-----|------|-----------------|
|                                     |                  | μPD41416-12 |     | μPD41416-15 |     | μPD41416-20 |     |      |                 |
|                                     |                  | Min         | Max | Min         | Max | Min         | Max |      |                 |
| Data-in hold time                   | t <sub>DH</sub>  | 35          |     | 45          |     | 55          |     | ns   | (Note 14)       |
| Data-in hold time referenced to RAS | t <sub>DHR</sub> | 95          |     | 120         |     | 155         |     | ns   |                 |
| Refresh period                      | t <sub>REF</sub> |             | 2   |             | 2   |             | 2   | ms   |                 |
| WE command setup time               | t <sub>WCS</sub> | 0           |     | 0           |     | 0           |     | ns   |                 |
| CAS to WE delay                     | t <sub>CWD</sub> | 95          |     | 120         |     | 155         |     | ns   |                 |
| RAS to WE delay                     | t <sub>RWD</sub> | 155         |     | 195         |     | 255         |     | ns   |                 |
| Access time from OE                 | t <sub>OEA</sub> | 30          |     | 40          |     | 50          |     | ns   |                 |
| Data delay time                     | t <sub>OED</sub> | 30          |     | 40          |     | 50          |     | ns   |                 |
| OE command hold time                | t <sub>OEH</sub> | 0           |     | 0           |     | 0           |     | ns   |                 |
| Output turn-off delay from OE       | t <sub>OEZ</sub> | 0           | 30  | 0           | 40  | 0           | 50  | ns   | (Note 10)       |

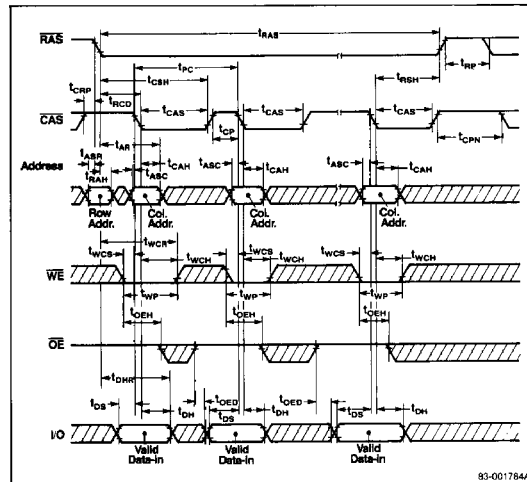
#### Notes:

- (1) All voltages referenced to GND.
- (2) An initial pause of 100  $\mu\text{s}$  is required after power-up followed by any 8  $\overline{RAS}$  cycles before proper device operation is achieved.
- (3) AC measurements assume  $t_T = 5\text{ ns}$ .
- (4)  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- (5)  $I_{CC1}$ ,  $I_{CC3}$  and  $I_{CC4}$  depend on output loading and cycle rates. Specified values are obtained with the outputs open.
- (6) The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ) is assured.
- (7) Load = 2 TTL loads and 100 pF.
- (8) Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds the value shown.
- (9) Assumes that  $t_{RCD} \geq t_{RCD}(\text{max})$ .
- (10)  $t_{OFF}(\text{max})$  and  $t_{OEZ}(\text{max})$  define the time at which the output achieves the open circuit condition and are not referenced to  $V_{OH}$  or  $V_{OL}$ .
- (11) Operation within the  $t_{RCD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met.  $t_{RCD}(\text{max})$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
- (12)  $t_{CRP}$  requirement should be applicable for  $\overline{RAS}$ ,  $\overline{CAS}$  cycles preceded by any cycle.
- (13) Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.
- (14) These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WE}$  leading edge in delayed write or read-modify-write cycles.

**Timing Waveforms****Read Cycle** **$\overline{OE}$ -Controlled Write Cycle****Write Cycle (Early Write)****"RAS-Only" Refresh Cycle****Read-Write / Read-Modify-Write Cycle****Hidden Refresh Cycle**

## Timing Waveforms (cont)

### Page Mode Write Cycle (Early Write)



### Page Mode Read-Write / Read-Modify-Write Cycle

