NEC
μPD421
μPD421-1
μPD421-2
μPD421-3
μPD421-5

8K BIT STATIC RAM

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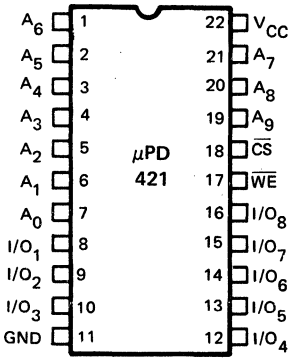
DESCRIPTION

The NEC μPD421 is a very high speed 8192 bit static Random Access Memory organized as 1024 words by 8 bits. Features include a power down mode controlled by the chip select input for an 80% power saving.

FEATURES

- 1024 x 8-bit Organization
- Very Fast Access Time: 150/200/250/300/450 ns
- Single +5V Power Supply
- Low Power Standby Mode
- N-Channel Silicon Gate Process
- Fully TTL Compatible
- 6-Device Static Cell
- Three State Common I/O
- Compatible with 8108 and Equivalent Devices
- Available in 22 Pin Ceramic Dual-in-Line Package

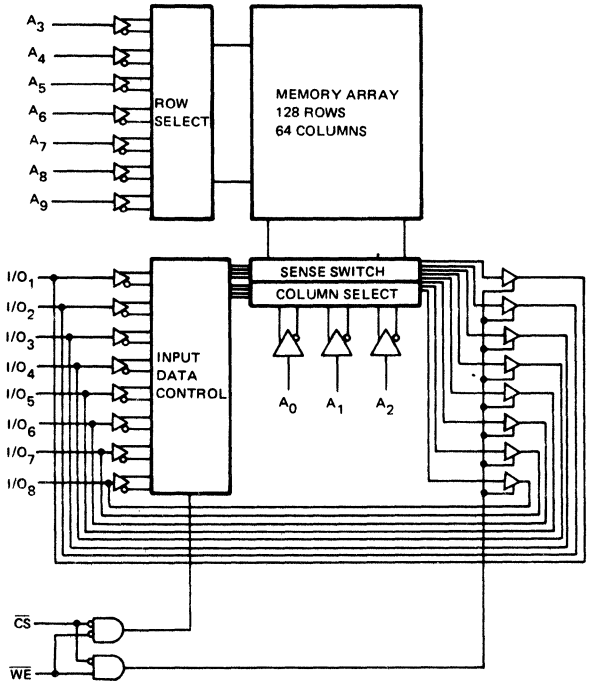
PIN CONFIGURATION



PIN NAMES

A_0-A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_8	Data Input Output
V_{CC}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin . . . . . −0.5 to +7 Volts ①

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%, unless otherwise specified

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Load Current (All Inputs Pins)	I_{LI}			10	μA	V_{IN} = 0 to +5.5V
I/O Leakage Current	I_{LO}			50	μA	
Operating Current	I_{CC}			120	mA	V_{CC} = Max; $\overline{CS}$ = V_{IL}; Outputs Open
Stand-by Current	I_{SB}			20	mA	V_{CC} = Min. to Max. $\overline{CS}$ = V_{IH}
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Input High Voltage	V_{IH}	2.0		6.0	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4.0 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -1 mA

CAPACITANCE $T_a = 25°C; f = 1.0\ MHz$

PARAMETER	SYMBOL	LIMITS		UNIT	TEST CONDITIONS
		MIN	MAX		
Input/Output Capacitance	$C_{I/O}$		7	pF	$V_{I/O} = 0V$
Input Capitance	C_{IN}		5	pF	$V_{IN} = 0V$

AC CHARACTERISTICS

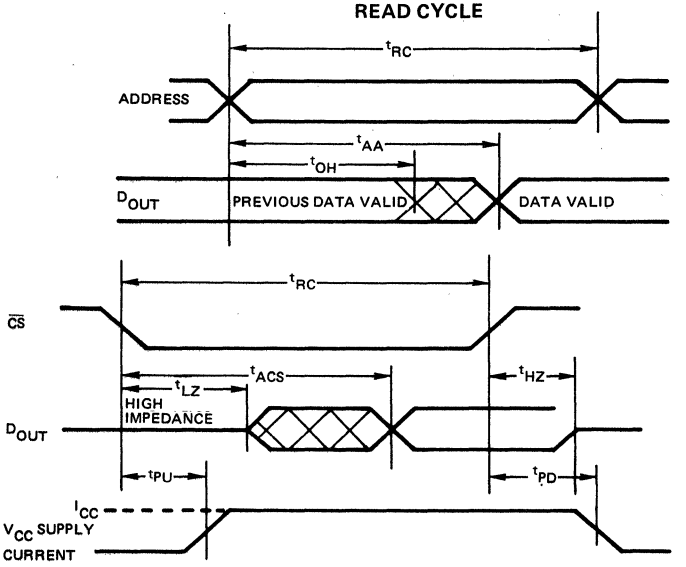
$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$, unless otherwise specified

PARAMETER	SYMBOL	LIMITS										UNIT
		μPD421		μPD421-1		μPD421-2		μPD421-3		μPD421-5		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE												
Read Cycle Time	t_{RC}	450		300		250		200		150		ns
Address Access Time	t_{AA}		450		300		250		200		150	ns
Chip Select Access Time	t_{ACS}		450		300		250		200		150	ns
Output Hold from Address Change	t_{OH}	10		10		10		10		10		ns
Chip Selection To Output in Low Z	t_{LZ}	10		10		10		10		10		ns
Chip Deselection to Output in High Z	t_{HZ}	0	100	0	80	0	70	0	60	0	50	ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		0		0		ns
Chip Deselection to Power Down Time	t_{PD}①		100		80		70		60		50	ns
WRITE CYCLE												
Write Cycle Time	t_{WC}	450		300		250		200		150		ns
Chip Selection to End of Write	t_{CW}	360		240		200		160		130		ns
Address Valid to End of Write	t_{AW}	360		240		200		160		130		ns
Address Setup Time	t_{AS}	10		10		10		10		10		ns
Write Pulse Width	t_{WP}	300		230		190		160		130		ns
Write Recovery Time	t_{WR}	10		10		10		10		10		ns
Data Valid to End of Write	t_{DW}	200		150		120		100		80		ns
Data Hold Time	t_{DH}	10		10		10		10		10		ns
Write Enabled to Output in High Z	t_{WZ}		100		80		70		60		50	ns
Output Active from End of Write	t_{OW}	10		10		10		10		10		ns

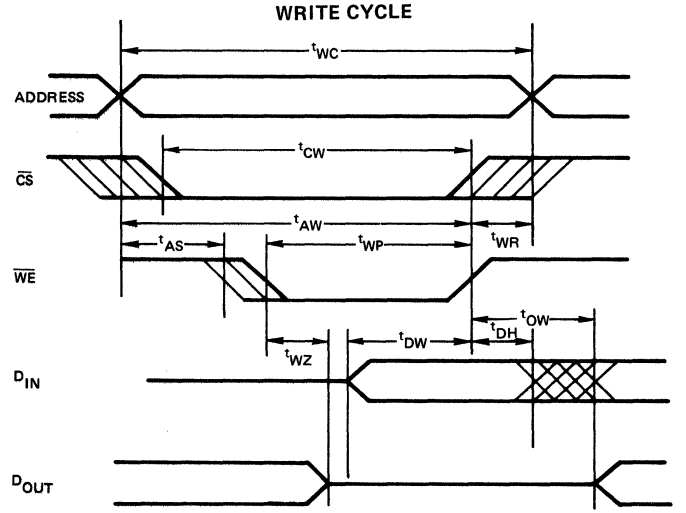
Note: ① I_{CC} $(t = t_{PD}) = 1/2\ I_{CC}$ Active.

TIMING WAVEFORMS

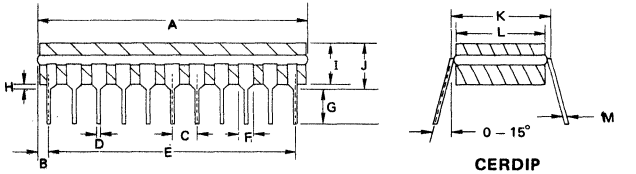
READ CYCLE



WRITE CYCLE



PACKAGE OUTLINE μPD421D



CERDIP

ITEM	MILLIMETERS	INCHES
A	27.43 Max.	1.079 Max.
B	1.27 Max.	0.05 Max.
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 Max.	0.165 Max.
J	5.08 Max.	0.200 Max.
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009