Description

The μPD42102 is a 1,135-word by 8-bit line buffer fabricated with a CMOS silicon-gate process. The device helps to create a PAL flicker-free television picture (non-interlaced scan conversion) by providing intermediate storage and very high-speed read and write operation.

The μPD42102 can also be used as a digital delay line. The delay length is variable from 2 bits (at maximum clock speed) to 1,135 bits.

Features

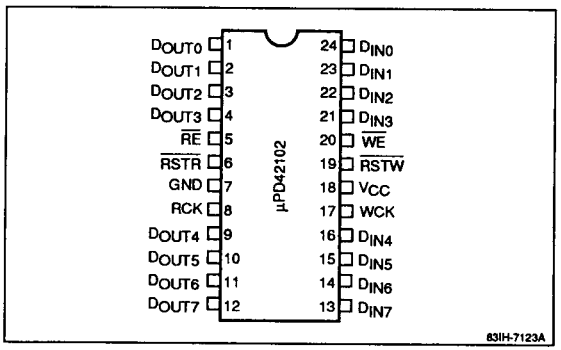
- 1,135-word x 8-bit organization
- Line buffer for PAL, $4f_{SC}$ digital television systems
- Asynchronous, simultaneous read/write operation
- 1H (1,135-bit) delay line capability
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- 24-pin plastic DIP and miniflat packaging

Ordering Information

Part Number	Read Cycle Time (min)	Write Cycle Time (min)	Package
μPD42102C-5	25 ns	25 ns	24-pin plastic DIP
C-3	34 ns	34 ns	
C-2	34 ns	69 ns	
C-1	69 ns	69 ns	
μPD42102G-5	25 ns	25 ns	24-pin plastic miniflat
G-3	34 ns	34 ns	
G-2	34 ns	69 ns	
G-1	69 ns	69 ns	

Pin Configuration

24-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
D_{IN0} - D_{IN7}	Write data inputs
D_{OUT0} - D_{OUT7}	Read data outputs
$\overline{RSTW}$	Write address reset input
$\overline{RSTR}$	Read address reset input
$\overline{WE}$	Write enable input
$\overline{RE}$	Read enable input
WCK	Write clock input
RCK	Read clock input
GND	Ground
V_{CC}	+5-volt power supply

PIN FUNCTIONS

D_{IN0} - D_{IN7} (Data Inputs)

In a digital television application, the digital composite signal, luminance, chrominance, etc. information is written into these inputs.

D_{OUT0} - D_{OUT7} (Data Outputs)

The tri-state outputs are used to access the stored information. In a simple digital delay line application, a delay of one-half write clock cycle plus a maximum of 300 ns is required to move data from the data inputs to the data outputs.

$\overline{RSTW}$ (Write Address Reset Input)

Bringing this signal low when $\overline{WE}$ is also low resets the internal write address to 0. If $\overline{WE}$ is at a high level when the $\overline{RSTW}$ input is brought low, the internal write address is set to 1,134. The state of this input is strobed by the rising edge of WCK.

$\overline{RSTR}$ (Read Address Reset Input)

This signal is strobed by the rising edge of RCK and resets the internal read address to 0 if $\overline{RE}$ is also low. If $\overline{RE}$ is at a high level when the $\overline{RSTR}$ input is brought low, the internal read address is set to 1,134.

$\overline{WE}$ (Write Enable Input)

This input controls write operation. If $\overline{WE}$ is low, all write cycles proceed. If $\overline{WE}$ is at a high level, no data is written to storage cells and the write address stops increasing. The state of $\overline{WE}$ is strobed by the rising edge of WCK.

$\overline{RE}$ (Read Enable Input)

This signal is similar to $\overline{WE}$ but controls read operation. If $\overline{RE}$ is at a high level, the data outpus become high impedance and the internal read address stops increasing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

WCK (Write Clock Input)

All write cycles are executed synchronously with WCK. The states of both $\overline{RSTW}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 1,134 to 0 and begin increasing again.

RCK (Read Clock Input)

All read cycles are executed synchronously with RCK. The states of both $\overline{RSTR}$ and $\overline{RE}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle unless $\overline{RE}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 1,134 to 0 and begin increasing again.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltages on any input pin, V_I	−1.5 to + 7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

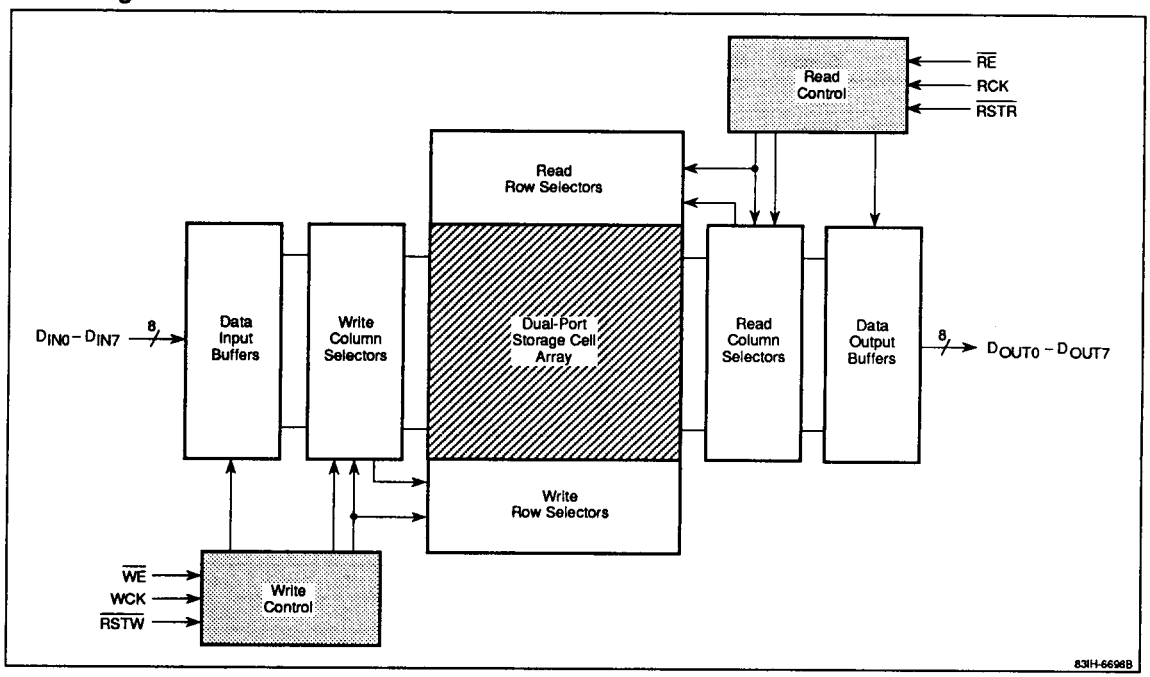
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.5		0.8	V
Operating temperature	T_A	−20		70	°C

Capacitance

T_A = 25°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Min	Max	Unit	Pins Under Test
Input capacitance	C_I		5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0} - D_{IN7}
Output capacitance	C_O		7	pF	D_{OUT0} - D_{OUT7}

Block Diagram



DC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_I	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; V_O = 0 to 5.5 V
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA

AC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD42102-5		μPD42102-3		μPD42102-2		μPD42102-1			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Write/read cycle operating current	I_{CC}		80		80		70		40	mA	t_{WCK} = t_{WCK} (min); t_{RCK} = t_{RCK} (min)
Write clock cycle time	t_{WCK}	25	880	28	880	56	880	56	880	ns	
WCK pulse width	t_{WCW}	10		12		20		20		ns	
WCK precharge time	t_{WCP}	10		12		20		20		ns	
Read clock cycle time	t_{RCK}	25	880	28	880	28	880	56	880	ns	
RCK pulse width	t_{RCW}	10		12		12		20		ns	
RCK precharge time	t_{RCP}	10		12		12		20		ns	
Access time	t_{AC}		18		21		21		40	ns	
Output hold time	t_{OH}	5		5		5		5		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD42102-5 Min	μPD42102-5 Max	μPD42102-3 Min	μPD42102-3 Max	μPD42102-2 Min	μPD42102-2 Max	μPD42102-1 Min	μPD42102-1 Max	Unit	Test Conditions
Access time after a reset cycle	t_{ACR}		18		21		21		40	ns	
Output hold time after a reset cycle	t_{OHR}	5		5		5		5		ns	
Output active time	t_{LZ}	5	18	5	21	5	21	5	40	ns	(Note 4)
Output disable time	t_{HZ}	5	18	5	21	5	21	5	40	ns	(Note 4)
Data-in setup time	t_{DS}	7		12		15		15		ns	
Data-in hold time	t_{DH}	3		5		5		5		ns	
Reset active setup time	t_{RS}	7		12		12		20		ns	(Note 7)
Reset active hold time	t_{RH}	3		5		5		5		ns	(Note 7)
Reset inactive hold time	t_{RN1}	3		5		5		5		ns	(Note 8)
Reset inactive setup time	t_{RN2}	7		12		12		20		ns	(Note 8)
Write enable setup time	t_{WES}	7		12		20		20		ns	(Note 9)
Write enable hold time	t_{WEH}	3		5		5		5		ns	(Note 9)
Write enable high delay from WCK	t_{WEN1}	3		5		5		5		ns	(Note 10)
Write enable low delay to WCK	t_{WEN2}	7		12		20		20		ns	(Note 10)
Read enable setup time	t_{RES}	7		12		12		20		ns	(Note 9)
Read enable hold time	t_{REH}	3		5		5		5		ns	(Note 9)
Read enable high delay from RCK	t_{REN1}	3		5		5		5		ns	(Note 10)
Read enable low delay to RCK	t_{REN2}	7		12		12		20		ns	(Note 10)
Write disable pulse width	t_{WEW}	0		0		0		0		ns	(Note 5)
Read disable pulse width	t_{REW}	0		0		0		0		ns	(Note 5)
Write reset time	t_{RSTW}	0		0		0		0		ns	(Note 5)
Read reset time	t_{RSTR}	0		0		0		0		ns	(Note 5)
Transition time	t_T	3	35	3	35	3	35	3	35	ns	

Notes:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume t_T = 5 ns. Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V.
For the –5 version only, t_T = 3 ns; input pulse levels = 0.4 to 2.4 V; transition times are measured between 0.4 and 2.4 V. See figures 1 and 2.

(3) Input timing reference levels = 1.5 V. Output timing reference levels are 0.8 and 2.0 V. See figure 3.

(4) This delay is measured at 200 mV from the steady-state voltage with the load specified in figure 5. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) t_{WEW} (max) and t_{REW} (max) must be satisfied by the following equations in 1-line cycle operation:
$t_{WEW} + t_{RSTW} + 1{,}135\ (t_{WCK}) \leq 1$ ms
$t_{REW} + t_{RSTR} + 1{,}135\ (t_{RCK}) \leq 1$ ms

(6) This parameter applies when $t_{RCK} \geq t_{ACR}$ (max).

(7) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(8) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(9) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(10) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

(11) Data is guaranteed to remain valid for a minimum of 1 ms after it is written. After this time, the data stored may be invalid, since this device uses a dynamic storage element.

Figure 1. Input Timing

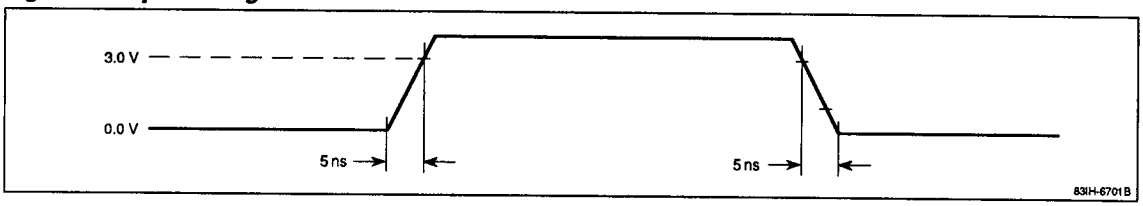


Figure 2. Input Timing for μPD42102-5

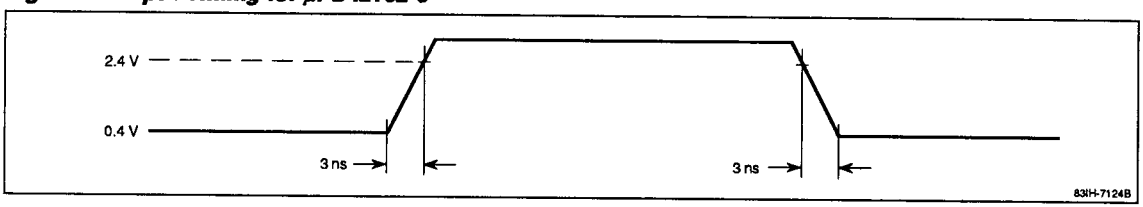


Figure 3. Output Timing

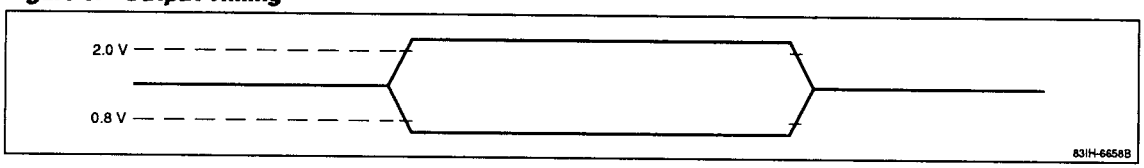


Figure 4. Output Load for t_{AC}, t_{ACR}, t_{OH} and t_{OHR}

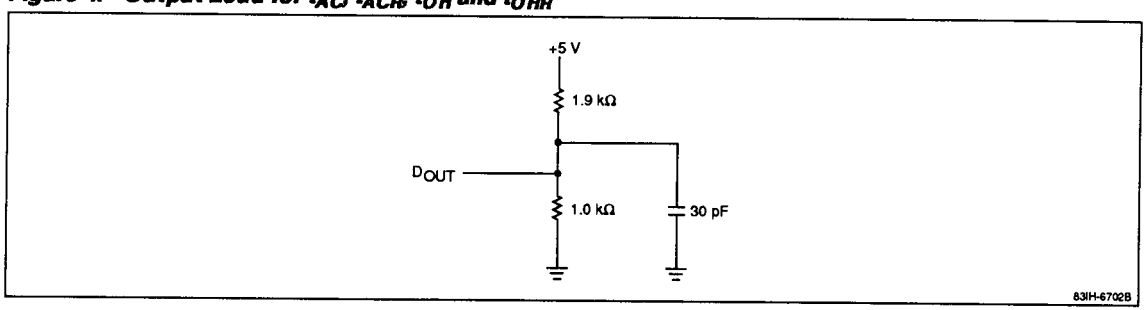
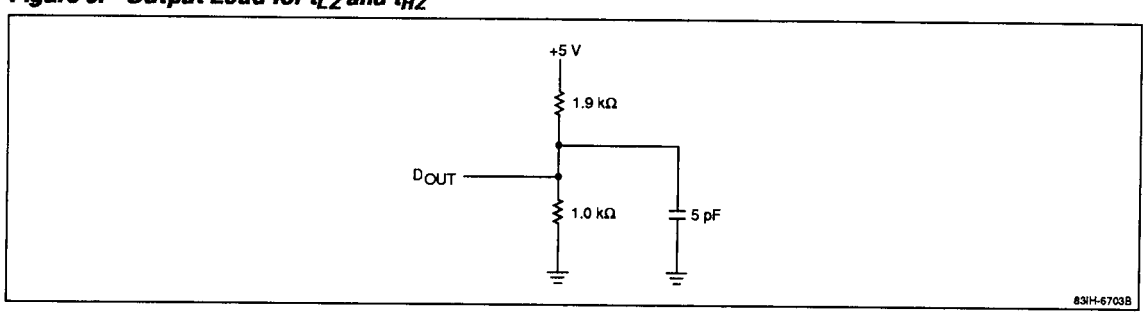
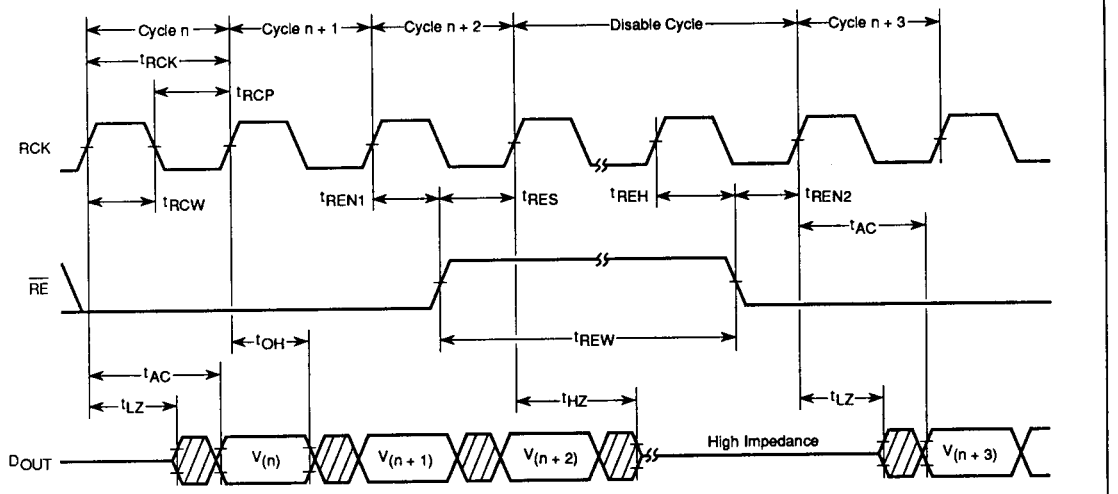


Figure 5. Output Load for t_{LZ} and t_{HZ}



Timing Waveforms

Read Cycle



Notes:
[1] $\overline{RSTR} = V_{IH}$.
[2] V = valid data.

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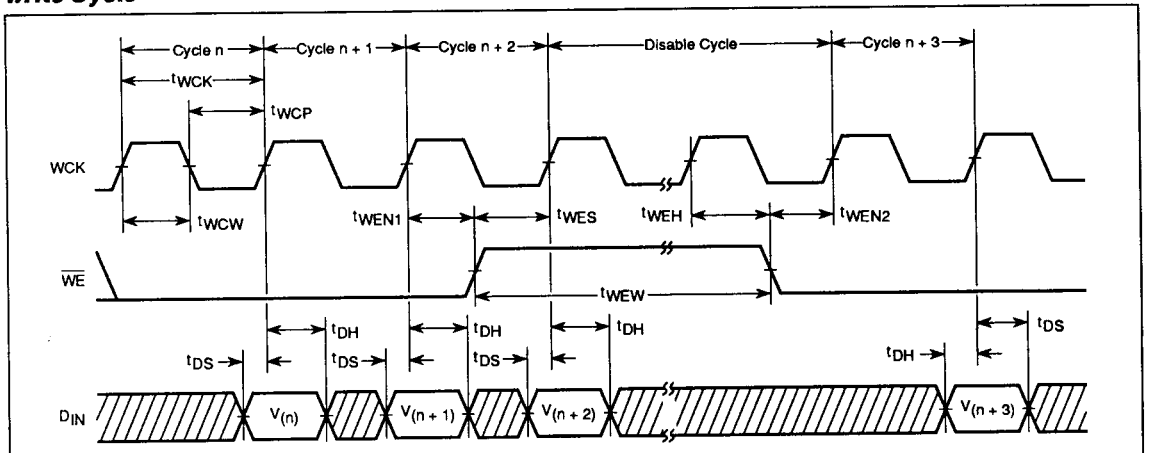
Write Cycle



Notes:
[1] $\overline{RSTW} = V_{IH}$.
[2] V = valid data.

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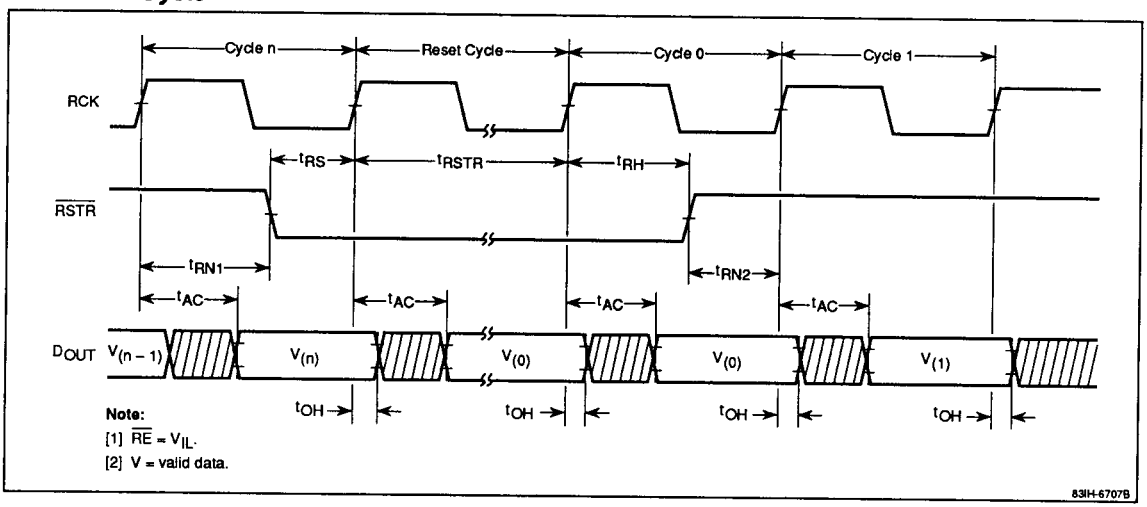
Timing Waveforms (cont)

Read Reset Cycle



Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = valid data.

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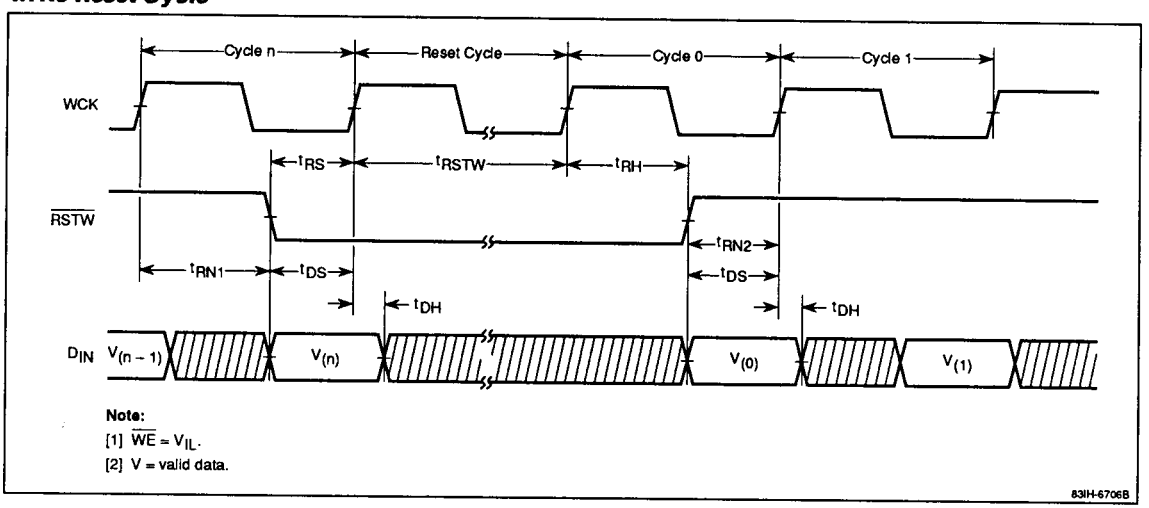
Write Reset Cycle



Note:
[1] $\overline{WE} = V_{IL}$.
[2] V = valid data.

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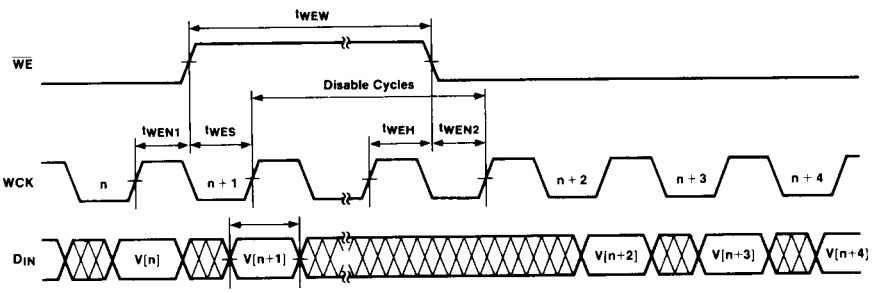
Timing Waveforms (cont)

Write Disable Cycle



Note:
[1] V = Valid Data.

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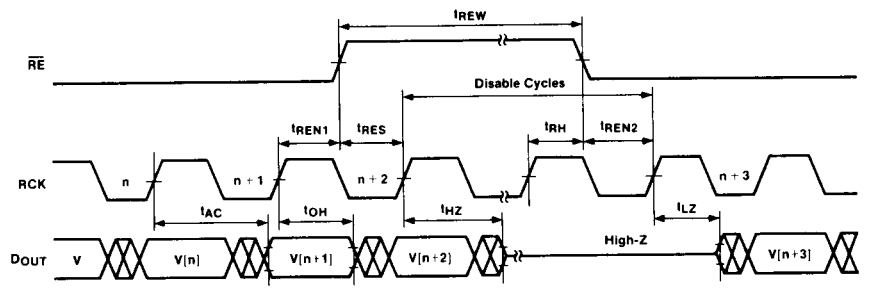
Read Disable Cycle



Note:
[1] V = Valid Data.

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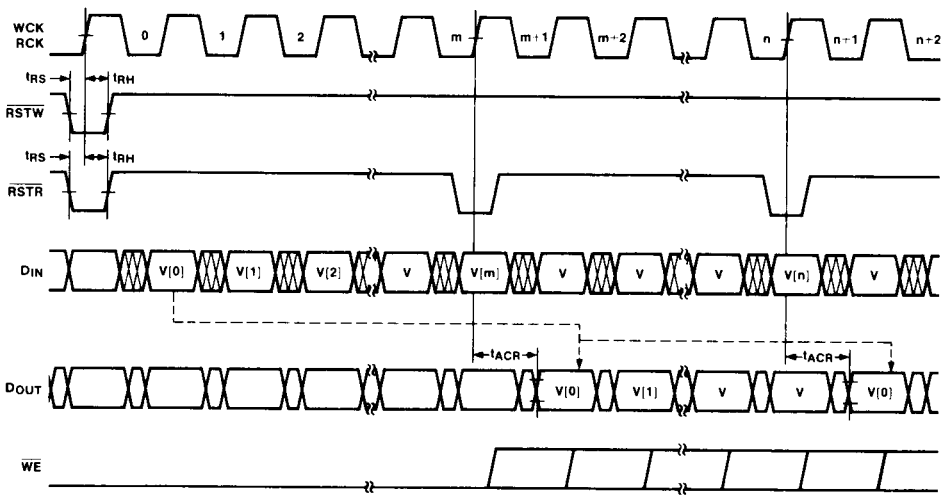
Timing Waveforms (cont)

Re-Read Cycle



Note:

[1] $\overline{RE} = V_{IL}$.

[2] V = Valid Data.

[3] The data stored in any location can be re-read as many times as desired within a period of 1 ms following the writing of data into that location provided that a second write operation has not re-written new data into that location.

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