

Description

The μ PD4227x (42271 and 42272) is a picture-in-picture generator designed for use in NTSC and PAL broadcasting systems. Picture-in-picture describes the device's ability to combine multiple video signals into a single signal for display on a television monitor, for input to a VCR, or for use in any manner that a single video signal is used. The format may be selected so that one primary picture is displayed over the entire picture area. The other subpicture(s) can then be superimposed onto the primary one to allow multiple picture sources to be viewed simultaneously.

The picture-in-picture generator is available in two versions. The μ PD42272 is the full-featured version that can display a border in one of four colors around the subpicture. The μ PD42271 has exactly the same features except that it is not able to display a border around the subpicture.

The μ PD4227x has an onboard controller, field storage, buffer storage, two line buffers, and two oscillators. The controller sets the timing, performs vertical filtering, and stores and retrieves subpicture signal(s) for insertion into the primary picture signal. A line of the subpicture signal is placed in buffer storage before being written into field storage, which contains that portion of the signal to be displayed. The line buffers store a weighted average of three lines of the subpicture signal to provide vertical filtering, while the onboard oscillators facilitate interfacing to the μ PD4227x.

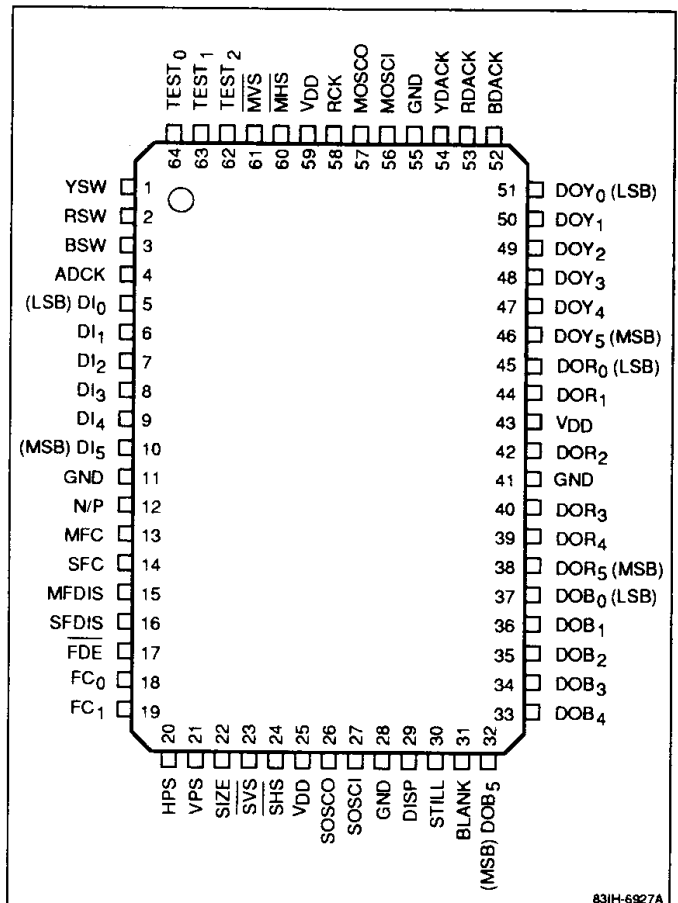
The level of integration provided by the μ PD4227x means that picture-in-picture can be achieved more quickly and easily than with standard video buffers and control circuitry.

Ordering Information

Part Number	Subpicture		Package
	Frame	Border	
μ PD42271AGF-3BE	No		64-pin plastic quad flatpack
μ PD42272AGF-3BE	Yes		

Pin Configuration

64-Pin Plastic QFP



Features

- NTSC and PAL compatibility
- Built-in vertical filter
- Selectable subpicture display size
- 134,676-bit field buffer and two line buffers
- Built-in input and output oscillators
- Four selectable screen positions
- Four-color selection of subpicture frame border (μ PD42272 only)
- Selectable freeze-frame display
- Automatic self-refreshing
- 6-bit resolution of Y, R-Y and B-Y signals
- Low power consumption of 75 mA max
- CMOS silicon-gate fabrication process
- Three-state outputs; TTL-compatible I/O
- Single +5-volt power supply

μPD42271, 42272**Absolute Maximum Ratings** $T_A = 25^\circ\text{C}$

Pin voltage, V_T	-0.1 to $V_{DD} + 0.5$ V
Supply voltage, V_{DD}	-0.1 to +7.0 V
Output current, I_O	50 mA
Operating temperature, T_{OPT}	-20 to +70°C
Storage temperature, T_{STG}	-55 to +125°C

Table 1. Description of Features

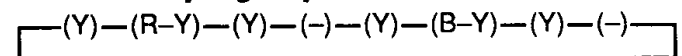
Feature	Description
Field memory capacity	7,568 words by 8 bits (86 x 88)
Quantization	6 bits
Frame colors	White, yellow, light blue, green (μPD42272 only)
Screen positions	Top left, bottom left, top right, bottom right
Field-to-field line offset sampling processing	Adjusts the starting location of the first line of a field to increase vertical resolution
Line array correction	Adjusts lines between even and odd fields
Display ON/OFF switching	Allows insertion or removal of subpicture
Still picture display	Freezes the subpicture display

Table 2. Subpicture Display Area

Video Standard	Full Screen	
	Display (1/9)	80% Screen Display (1/12)
NTSC	49.3 μs x 74 lines	41.3 μs x 62 lines
PAL	49.3 μs x 87 lines	41.3 μs x 73 lines

Table 3. Sampling Rate

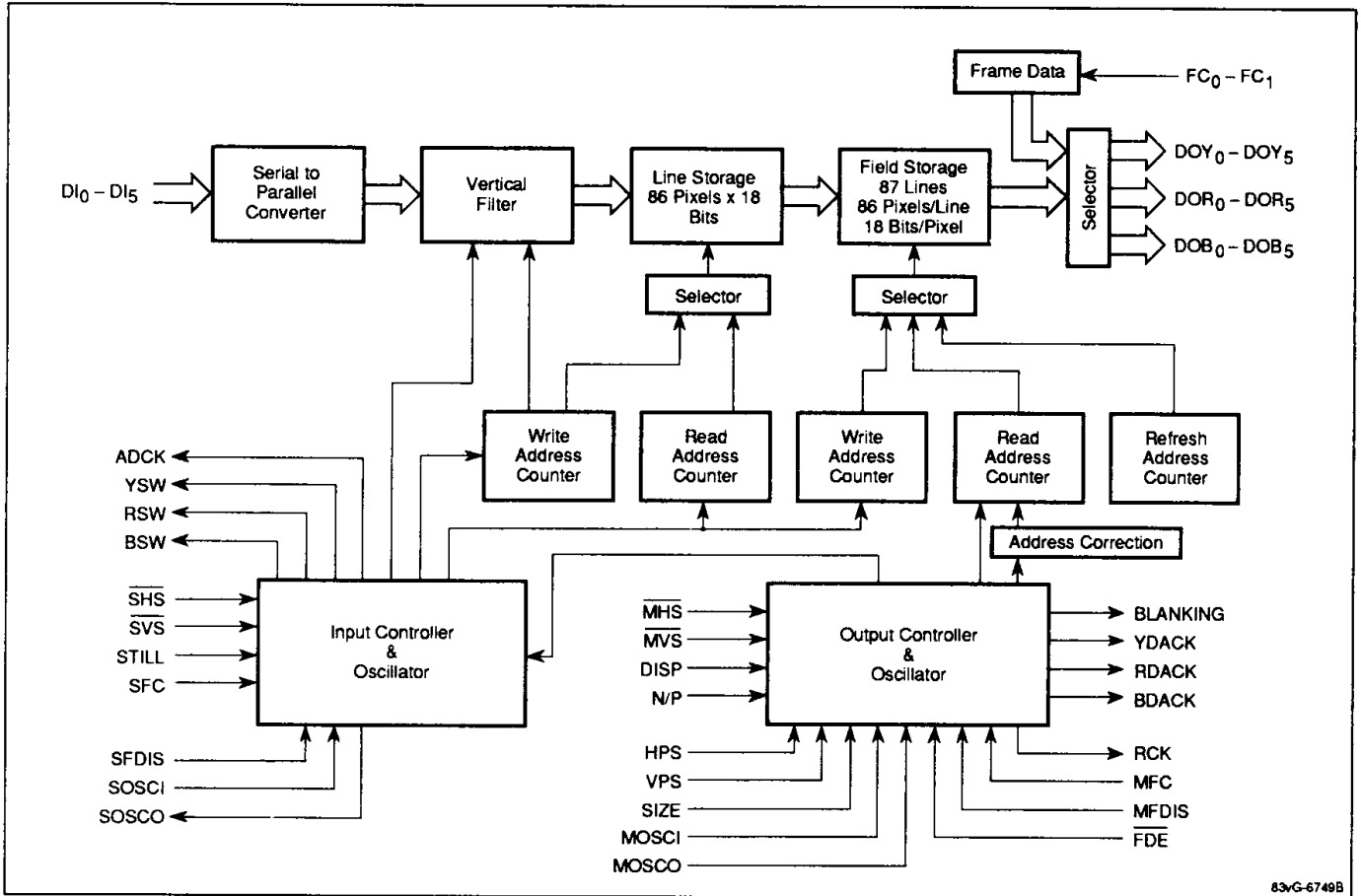
Signal	Input	Output
Y	3 MHz	9 MHz
R-Y	0.75 MHz	2.25 MHz
B-Y	0.75 MHz	2.25 MHz

Table 4. Sampling Sequence**Table 5. Average Vertical Filtering**

Line Number	Coefficient
$n - 1$	1/4
n	1/2
$n + 1$	1/4

Notes:(1) n = line to be sampled.

Block Diagram



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Pin Identification

Symbol	Function
ADCK	Analog/digital clock output
BDACK	Digital/analog clock for B-Y component signal output
BLANK	Main picture blanking output
BSW	DI ₀ - DI ₅ output enable for B-Y component signals
DI ₀ - DI ₅	Multiplexed B-Y, R-Y, and Y data inputs
DISP	Subpicture on/off input
DOB ₀ - DOB ₅	B-Y data outputs
DOR ₀ - DOY ₅	R-Y data outputs
DOY ₀ - DOY ₅	Y data outputs
FC ₀ and FC ₁	Frame color selection input
FDE	Field distinction data enable input
HPS	Horizontal position input
MFC	Main picture field correction input
MFDIS	Main picture field distinction input
MHS	Main picture horizontal synchronous input
MOSCI	Main picture oscillator input
MOSCO	Main picture oscillator output
MVS	Main picture vertical synchronous input
N/P	NTSC/PAL switching input
RCK	Read clock output
RDACK	Digital/analog clock for R-Y component signal output
RSW	DI ₀ - DI ₅ output enable for R-Y component signals
SFC	Subpicture field correction input
SFDIS	Subpicture field distinction input
SHS	Subpicture horizontal synchronous input
SIZE	Size selection input
SOSCI	Subpicture oscillator clock input
SOSCO	Subpicture oscillator clock output
STILL	Freeze frame input
SVS	Subpicture vertical synchronous input
TEST ₀ - TEST ₂	Test terminals
VPS	Vertical position input
YDACK	Digital/analog clock for Y component signal output
YSW	DI ₀ - DI ₅ output enable for Y component signals
V _{DD}	+ 5-volt power supply
GND	Ground

Pin Functions

ADCK. Y, R-Y and B-Y component signals selected with the analog switch are converted from analog to digital data in synchronization with this 6 MHz sampling clock. Digitized component signals are sequentially input to the DI₀ - DI₅ pins, also in synchronization with this clock.

BDACK. Digitized B-Y component signals are output from the DOB₀ - DOB₅ pins in synchronization with this 2.25 MHz sampling clock.

BLANK. When high, this output signal blanks the main picture, enabling the subpicture to be displayed.

BSW. A high logic level on BSW (while RSW and YSW are low) enables the DI₀ - DI₅ pins to be used for receiving 6-bit B-Y data from the A/D converter.

DI₀ through DI₅. These multiplexed pins are used for 6-bit digitized subvideo input, either B-Y, R-Y or Y, depending on the levels of BSW, RSW and YSW. DI₀ is the least significant bit and DI₅ is the most significant bit.

DISP. This pin controls the BLANK signal. A high logic level enables BLANK, while DISP low inhibits it. The level of DISP has no effect on the DOB₀ - DOB₅, DOR₀ - DOR₅, and DOY₀ - DOY₅ pins.

DOB₀ through DOB₅. These pins are used for 6-bit B-Y color difference output and depend on the status of BDACK. When no B-Y data is being output, the pins are in high impedance.

DOR₀ through DOR₅. These pins are used for 6-bit R-Y color difference output and depend on the status of RDACK. When no R-Y data is being output, the pins are in high impedance.

DOY₀ through DOY₅. These pins are used for 6-bit Y luminance output and depend on the status of YDACK. When no Y data is being output, the pins are in high impedance.

FC₀ and FC₁. The combination of signals from these pins is used to specify subvideo frame color, as shown below:

Pin	White	Light Blue	Yellow	Green
FC ₀	high	low	high	low
FC ₁	high	high	low	low

FDE. This pin is used to select external or internal field distinction. FDE high enables external field distinction, while FDE low inhibits the MFDIS and SFDIS pins and causes field distinction to be executed internally.

HPS and VPS. These horizontal and vertical input pins specify positioning of the subpicture. One of the four corners on the main picture can be selected by combining the input levels on HPS and VPS, as shown below.

Pin	Top Left	Bottom Left	Top Right	Bottom Right
HPS	high	high	low	low
VPS	high	low	high	low

MFC. Fields of the main picture are distinguished by the μPD4227x based on the phase relationship of the MHS and MVS signals. Field distinction may therefore be distorted if the signals are not in proper phase. In these cases, a high logic level on MFC can be used to reverse field distinction. MFC low has no effect on field distinction.

MFDIS. The even and odd fields of the main picture signal are distinguished based on the phase relationship of MHS and MVS. MFDIS can be used to provide an external signal indicating either an odd (high) or even (low) field.

MHS. This pin is used to input a horizontal synchronization signal for the main picture. The internal read clock oscillator is synchronized to the rising edge of MHS and increments the field buffer's read address counter, which is used to determine the horizontal display size and position of the sub picture.

MOSCI. This pin is used as an oscillator input for the main picture read clock. To use the internal oscillator, an external coil and capacitor must be installed. Alternatively, an 18 MHz external clock may be input to MOSCI.

MOSCO. This pin is used as an output for the feedback circuit of the main picture's internal oscillator.

MVS. This pin is used to input a vertical synchronization signal for the main picture. The falling edge of MVS resets the field buffer's internal read address counter, which is used to determine the vertical display size and position of the subpicture.

N/P. A high logic level on this pin selects NTSC compatibility and a low selects PAL.

RCK. This pin is used as an output for the subpicture read clock, which is derived from MOSCI and MOSCO.

RDACK. Digital R-Y component signals are output from the DOR₀ - DOR₅ pins in synchronization with this 2.25 MHz sampling clock.

RSW. A high logic level on RSW (while BSW and YSW are low) enables the DI₀ - DI₅ pins to be used for receiving 6-bit R-Y data from the A/D converter.

SFC. The μPD4227x distinguishes subpicture fields based on the phase relationship of the SHS and SVS signals. Field distinction of the subpicture may therefore be distorted if the signals are not in phase. SFC high can be used to reverse field distinction. SFC low has no effect on field distinction.

SFDIS. The even and odd fields of the subpicture signal(s) are distinguished based on the phase relationship of the SHS and SVS signals. This pin can be used to provide an external signal indicating either an odd (high) or even (low) field.

SHS. This pin is used to input the horizontal synchronization for the subpicture. The rising edge of this clock is used to synchronize the internal write clock oscillator which is then used to increment the write address counters for the line buffers and the field buffer.

SIZE. This input is used to specify size of the subpicture display area. SIZE high sets a full screen display and occupies 1/9 of the main picture. SIZE low displays 80% of the subpicture and occupies 1/12 of the main picture.

SOSCI. This pin is used as an oscillator input for the subpicture write clock. To use the internal oscillator, an external coil and capacitor must be installed. Alternatively, an 6 MHz external clock may be input to SOSCI.

SOSCO. This pin is used as an output for the feedback circuit of the subpicture's internal oscillator.

STILL. A high logic level selects a still picture, while STILL low selects a moving picture.

SVS. This pin is used to input the vertical synchronization signal for the subpicture. The falling edge of this signal resets the internal write address counters for the line buffers and the field buffer.

TEST₀ - TEST₂. These are test pins and must be open.

YDACK. Digital Y component signals are output from the DOY₀ - DOY₅ pins in synchronization with this 9 MHz sampling clock.

YSW. A high logic level on YSW (while BSW and RSW are low) enables the DI₀ - DI₅ pins to be used for receiving 6-bit Y data from the A/D converter.

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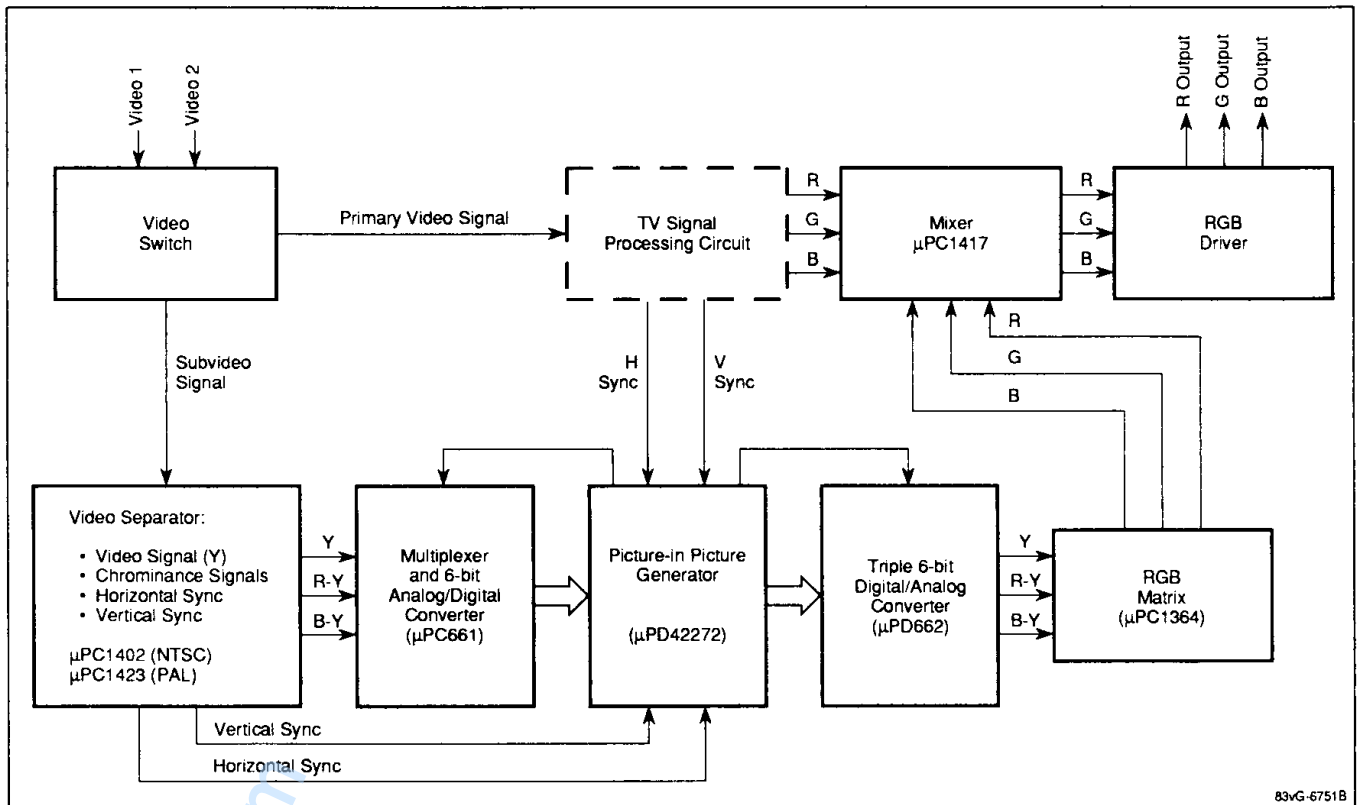
Application

The following block diagram illustrates one application for the μ PD4227x in an NTSC television system.

The video signals for the subpicture are separated into Y, B-Y, and R-Y component signals and horizontal and vertical synchronization signals by the μ PC1402 decoder. The Y, B-Y, and R-Y component signals are input in parallel to the μ PC661 A/D converter, after which they are switched to the sequence Y, R-Y, Y, -, Y, B-Y, Y, - using time-division multiplexing and converted to digital signals. In this instance, timing for the Y, R-Y, and B-Y conversion process is regulated by the μ PD4227x.

After the μ PD4227x receives the 6-bit digital data output by the μ PC661, it compresses the subpicture data and stores one field. The output signals are sent by the μ PD4227x to the μ PC662, which contains three D/A converters assigned respectively to the Y, R-Y, and B-Y signals. If the analog component signals output by the D/A converters are to be used by the TV, they then are converted to an RGB signal by the μ PC1364 matrix circuit. If they are to be used by the VCR, they are combined with the main picture signal after being converted into composite signals in the encoder circuit.

Application Example



Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{DD}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		$V_{DD} + 0.5$	V	
Input voltage, low	V_{IL}	-1.0		0.8	V	
Input oscillation frequency	$f_{OSC IN}$		6		MHz	
Output oscillation frequency	$f_{OSC OUT}$		18		MHz	
Horizontal synchronizing pulse width	t_{HSYNC}		4.8		μs	\overline{SHS} and \overline{MHS} pins
Ambient temperature	T_A	-20		70	°C	

DC Characteristics $T_A = -20$ to $+70^\circ\text{C}$; $V_{DD} = +5.0\text{ V} \pm 10\%$

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply current	I_{DD}		75		mA	$f_{OSC IN} = 6\text{ MHz}$; $f_{OSC OUT} = 18\text{ MHz}$
Input leakage current	I_I	-10		10	μA	$V_{IN} = 0\text{ V}$ to V_{DD} ; all other pins not under test = 0 V
Output leakage current	I_O	-10		10	μA	Outputs disabled; $V_{OUT} = 0\text{ V}$ to V_{DD}
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -1\text{ mA}$
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 2\text{ mA}$

Capacitance $T_A = 25^\circ\text{C}$; $f = 1\text{ MHz}$

Parameter	Symbol	Min	Typ	Max	Unit	Pins Under Test
Input capacitance	C_I			5	pF	All inputs except SOSC1 and MOSCI
Output capacitance	C_O			7	pF	All outputs except SOSCO and MOSCO
Oscillator input capacitance	C_{SOSC1}		8		pF	SOSC1
	C_{MOSCI}		10		pF	MOSCI
	C_{SOSCO}		8		pF	SOSCO
	C_{MOSCO}		10		pF	MOSCO

AC Characteristics $T_A = -20$ to $+70^\circ\text{C}$; $V_{DD} = +5.0\text{ V} \pm 10\%$

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
ADCK pulse width, low	t_{ADL}	70			ns	
ADCK pulse width, high	t_{ADH}	70			ns	
YDACK pulse width, low	t_{YDAL}	50			ns	
YDACK pulse width, high	t_{YDAH}	50			ns	
RDACK pulse width, low	t_{RDAL}	200			ns	(Note 7)
RDACK pulse width, high	t_{RDAH}	200			ns	(Note 7)
BDACK pulse width, low	t_{BDAL}	200			ns	(Note 7)
BDACK pulse width, high	t_{BDAH}	200			ns	(Note 7)
RCK pulse width, low	t_{RCKL}	25			ns	
RCK pulse width, high	t_{RCKH}	25			ns	
Data input setup time	t_{DS}	25			ns	
Data input hold time	t_{DH}	30			ns	

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AC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Y data access time	t_{ACY}			5	ns	
Y data hold time	t_{OHY}	20			ns	
R-Y data access time	t_{ACR}			$7(RCK) + 25$	ns	
R-Y data hold time	t_{OHR}	20			ns	
B-Y data access time	t_{ACB}			$7(RCK) + 25$	ns	
B-Y data hold time	t_{OHB}	20			ns	
Output low impedance time	t_{LZ}	5		100	ns	(Note 4)
Output high impedance time	t_{HZ}	5		100	ns	(Note 4)
YSW, RSW, BSW low hold time from ADCK	t_{SW1}	5		30	ns	
YSW, RSW, BSW high hold time from ADCK	t_{SW2}	5		30	ns	
Rise and fall transition time	t_T	3		35	ns	

Notes:

- (1) All voltages are referenced to ground.
- (2) Ac measurements assume $t_T = 5$ ns.
- (3) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
- (4) t_{OFF} (max) defines the time at which the output becomes open-circuit and is not referenced to V_{OH} or V_{OL} .
- (5) The input/output signal reference level is 1.5 V.
- (6) $f_{OSC IN}$ equals 6 MHz; $f_{OSC OUT}$ is 18 MHz.
- (7) The frame border output period is either 0.5 or 1.5 times as large as the standard value.
- (8) $t_{LZ} \geq t_{HZ}$.

Figure 1. Input Timing

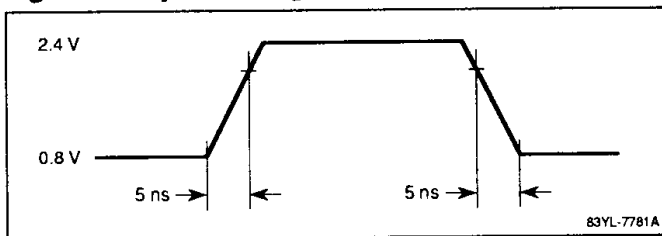


Figure 2. Output Timing

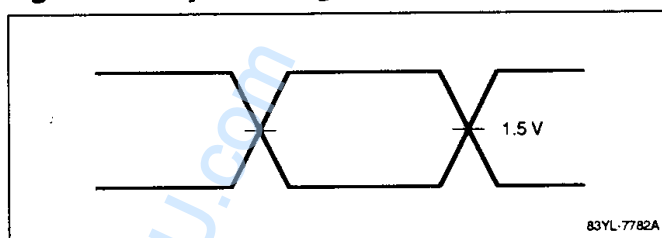


Figure 3. Output Load

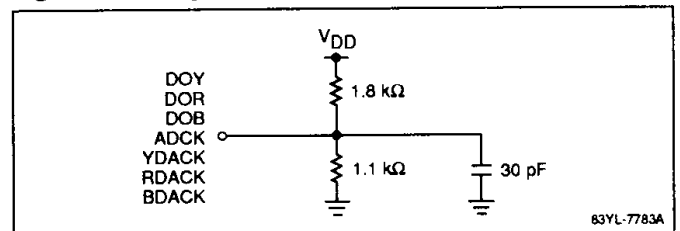
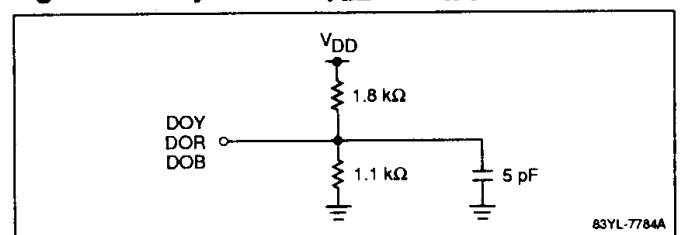


Figure 4. Output Load (t_{LZ} and t_{HZ})



Description

Serial/Parallel Converter (S → P). Converts the serially input 6-bit Y, R-Y, and B-Y subpicture signals into 18-bit parallel Y • R-Y • Y or Y • B-Y • Y signals, and then outputs them.

Vertical Filter. Executes averaging cycles and consists of two sets of line memory and an arithmetic circuit. If any one of the three lines is extracted to compress the screen vertically, the lines may become distorted on the screen. By averaging the data of the appropriate line with the preceding and succeeding lines, the filter prevents distortion.

Buffer Memory. Stores subpicture signals input during read operation and has a one-line capacity of 86 words by 18 bits.

Field Memory. Stores one 7,568-word by 18-bit field of a subpicture. Data is written into field memory when no subpicture is being displayed.

Buffer Memory Write Address Counter. Supplies write addresses to the buffer memory.

Buffer Memory Read Address Counter. Supplies read addresses to buffer memory in synchronization with the field memory write address counter and remains in standby during a field memory read cycle.

Buffer Memory Address Selector. Alternately outputs write and read addresses to buffer memory.

Field Memory Write Address Counter. Supplies write addresses to field memory and consists of horizontal and vertical address counters, the former of which is synchronized with the buffer memory read address counter. The counter remains in standby during a memory read cycle. When the address reaches its maximum value, the counter stops counting.

Field Memory Read Address Counter. Supplies read addresses to field memory and consists of horizontal and vertical address counters. Data read from field memory always takes priority over data written to it. Thus, the counter never enters standby in normal operation. When the address reaches its maximum value, the counter stops counting.

Refresh Address Counter. Supplies refresh addresses to field memory. When write/read operation to field memory terminates, this counter refreshes the memory location corresponding to its current value. The 6 MHz input clock is frequency-divided and supplied to the counter. It remains in standby while data is being read from or written into field memory. When the address reaches its maximum value, this counter stops counting and the address returns to the initial address.

Field Memory Address Selector. Alternately supplies the write, read, and refresh addresses.

Output Data Selector. Switches the subpicture signal read from field memory with the frame color signal selected by FC₀ and FC₁ and outputs the signal. This selector also concurrently executes parallel/serial conversion (12 bits → 6 bits) of the Y subpicture signal.

Input Controller and Oscillator. Controls the subpicture signal until it is written into field memory. This circuit oscillates the 6 MHz input clock synchronously with SHS. Using this clock as the reference, the circuit controls vertical filtering, i.e., buffer memory write/read operation, and field memory write operation. This circuit also generates the ADCK, YSW, RSW, and BSW control signals transmitted to the 6-bit A/D converter.

Output Controller and Oscillator. Controls the subpicture signal during the time in which the signal is read and then output from field memory. This circuit oscillates the 18 MHz output clock synchronously with MHS. Using this clock as the reference, the circuit controls field memory read operation and the data selector, and also generates the YDACK, RDACK and BDACK control signals transmitted to the 6-bit D/A converter. The BLANK and RCK signals are also generated by this circuit.

OPERATION**Writing the Subpicture Signals**

Subpicture signals are converted by the 6-bit μPC661 A/D converter into digital data, and then input from DI. At this time, the subpicture signals are sequentially switched with the YSW, RSW, and BSW data switching signals and serially sampled as shown in table 4.

The (–) data is not actually transferred. Subpicture signals are converted by the serial/parallel converter into 18-bit Y • R-Y • Y or Y • B-Y • Y data. They are then averaged by the vertical filter, whose configuration is shown in figure 5.

After being averaged by the vertical filter, the subpicture signals are extracted line by line from the three lines. They are then written into buffer memory. Once field memory read operation terminates, the subpicture signals are subsequently read from buffer memory and written into field memory at a rate of 1.5 MHz.

Two types of subpicture write areas, one for NTSC applications and the other for PAL, are shown in figures 6 and 7. The odd and even fields deviate by one line in the vertical write area to enable field-to-field line offset sampling and improve vertical resolution.

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Figure 5. Vertical Filter Configuration

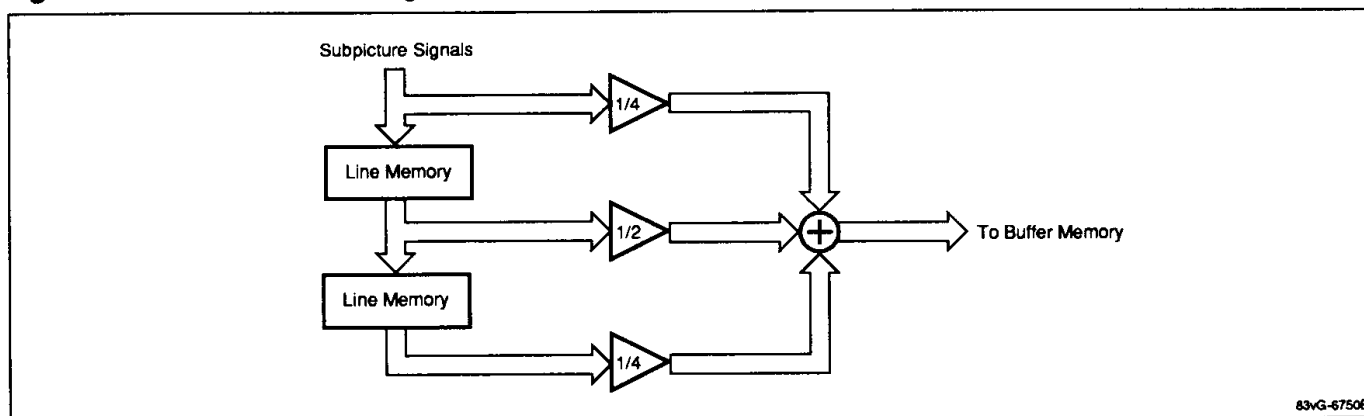
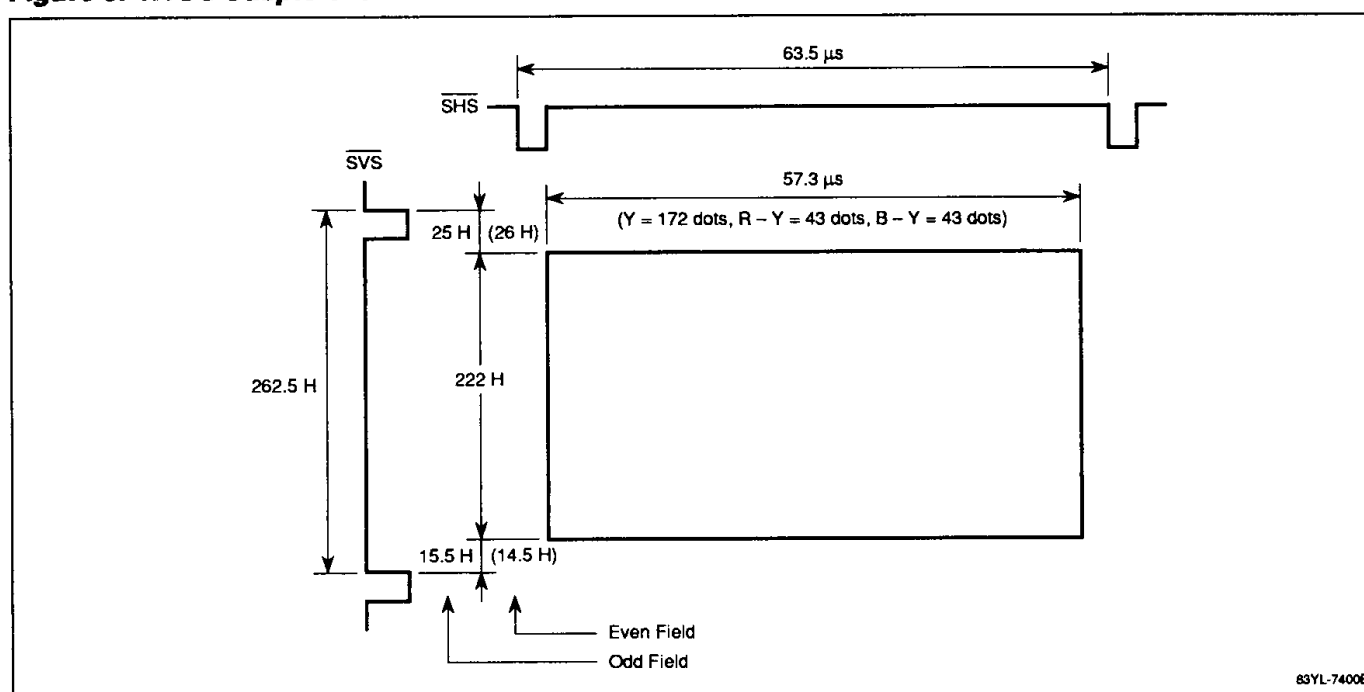


Figure 6. NTSC Subpicture Write Area

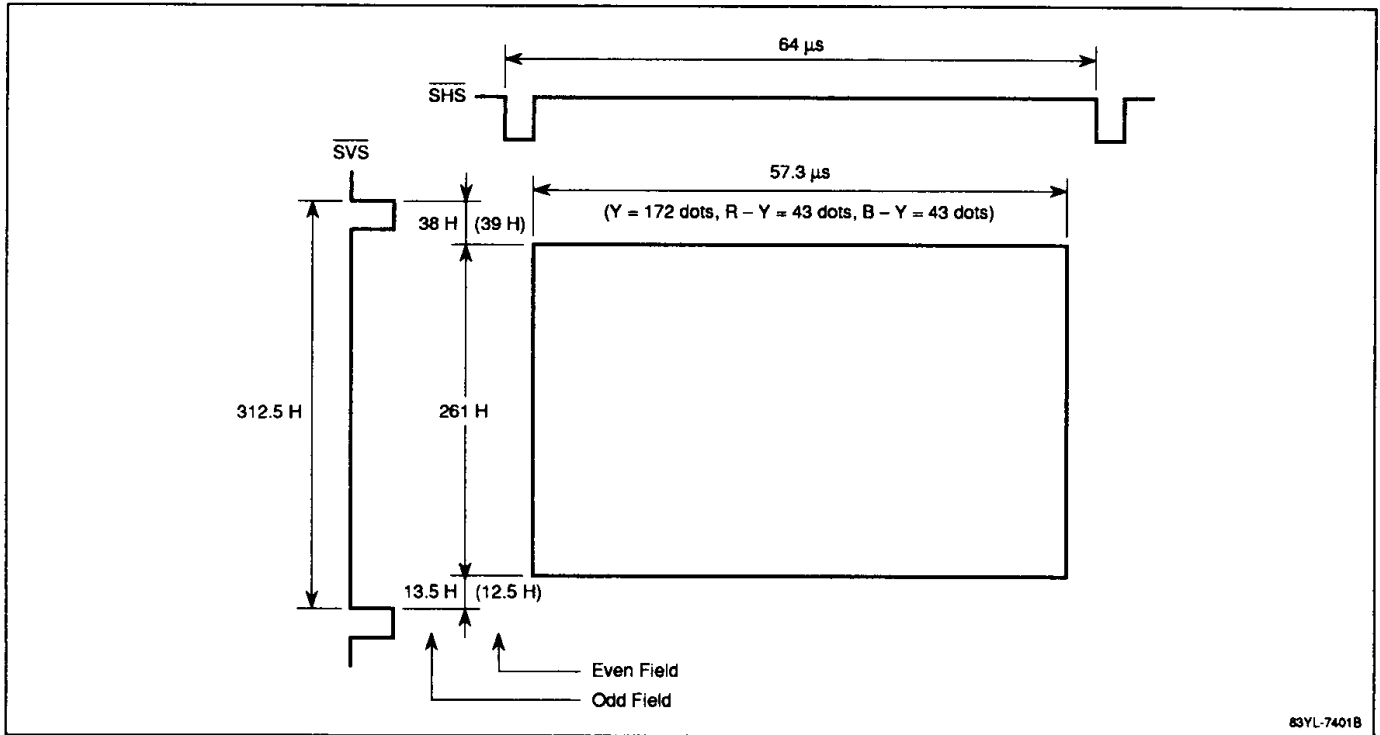


Reading the Subpicture Signals

After being written into field memory, subpicture signals are read synchronously with the signals from \overline{MHS} and \overline{MVS} . Reading of subpicture signals is executed for all data written (the 4.5 MHz reading rate is three times as high as the writing rate). Subpicture signals then pass the selector and are output through DOY, DOR, and DOB. In addition to switching and outputting the subpicture and frame signals, the selector executes 12 to 6 bit, parallel to serial conversion of the Y signal.

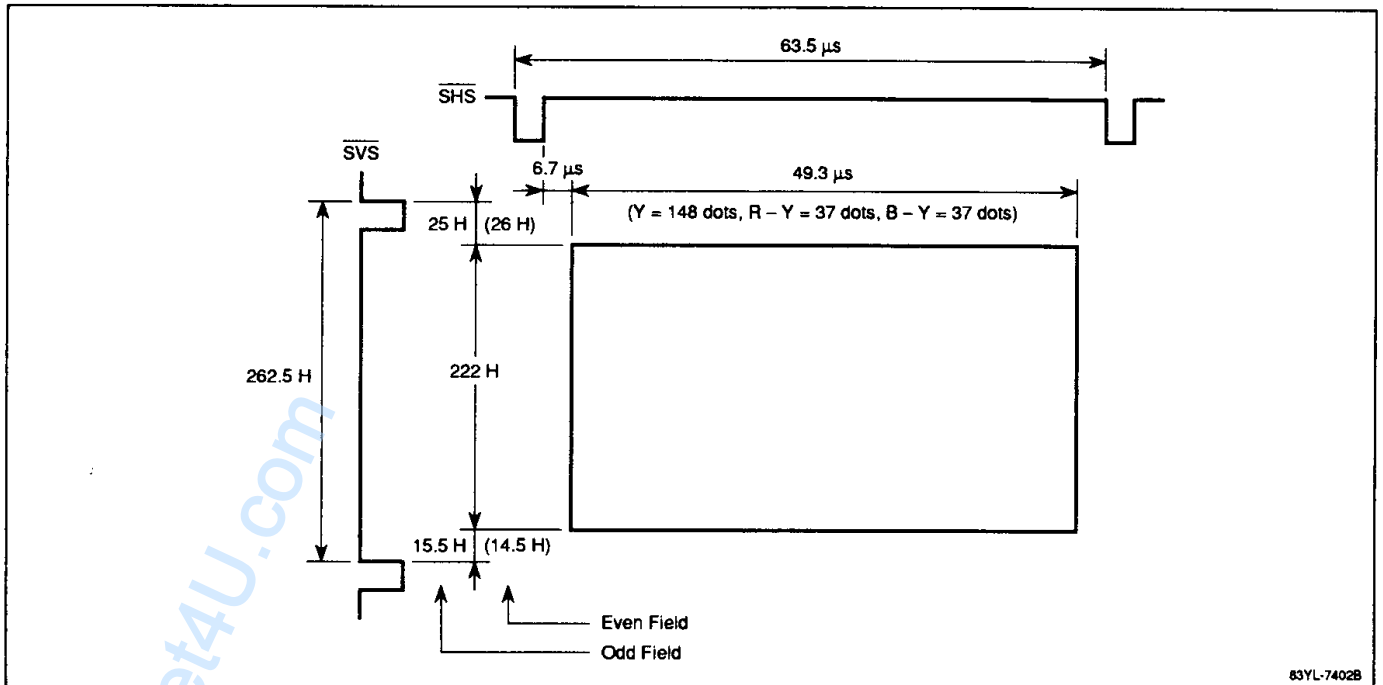
The playback area is determined by the blanking signal and not by the write area. The display position is controlled by changing the timing of the read address counter according to the state of the HPS and VPS input pins. The playback area and display position vary with the NTSC/PAL method and screen size (full versus 80% full) as shown in figures 8 through 15. Any value in the display position includes the frame signal, which has a 220 ns (horizontal) x 1 line (vertical) area.

Figure 7. PAL Subpicture Write Area



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Figure 8. Subpicture Playback Area in NTSC Applications with Full Screen Display



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Figure 9. Subpicture Playback Area in NTSC Applications with 80% Screen Display

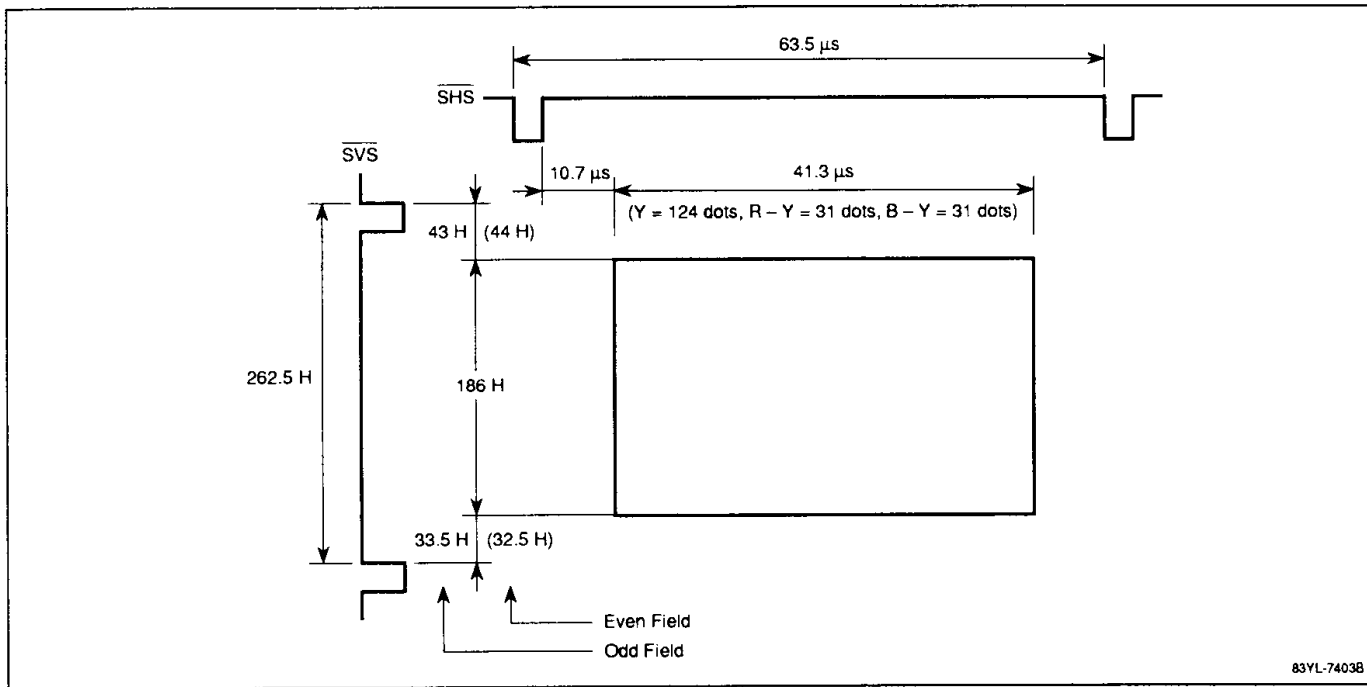


Figure 10. Subpicture Playback Area in PAL Applications with Full Screen Display

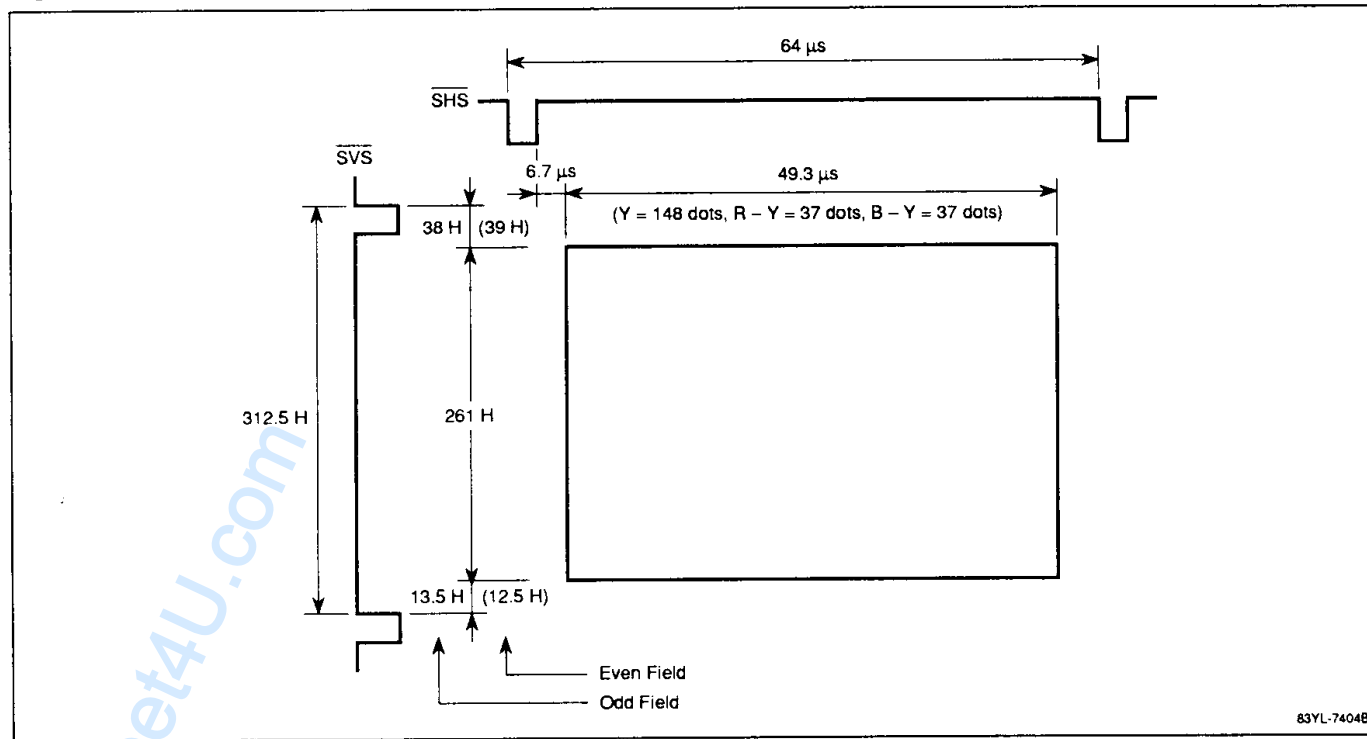
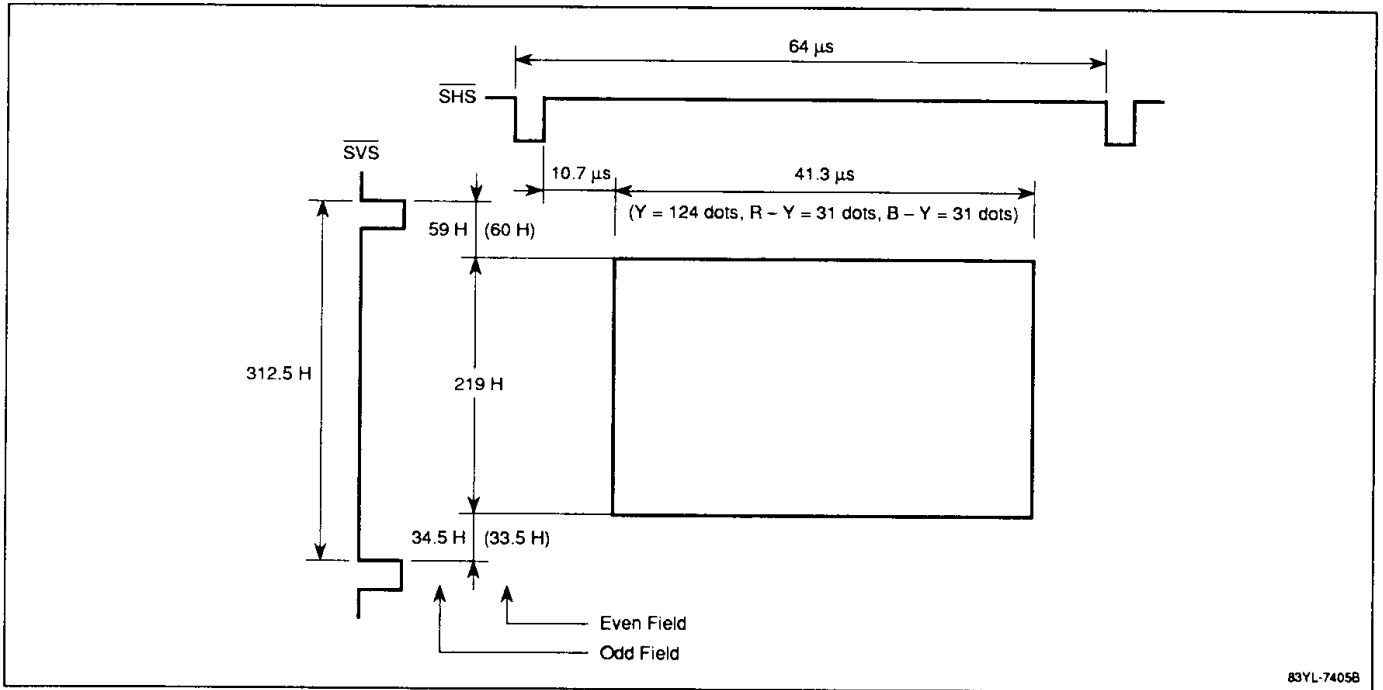
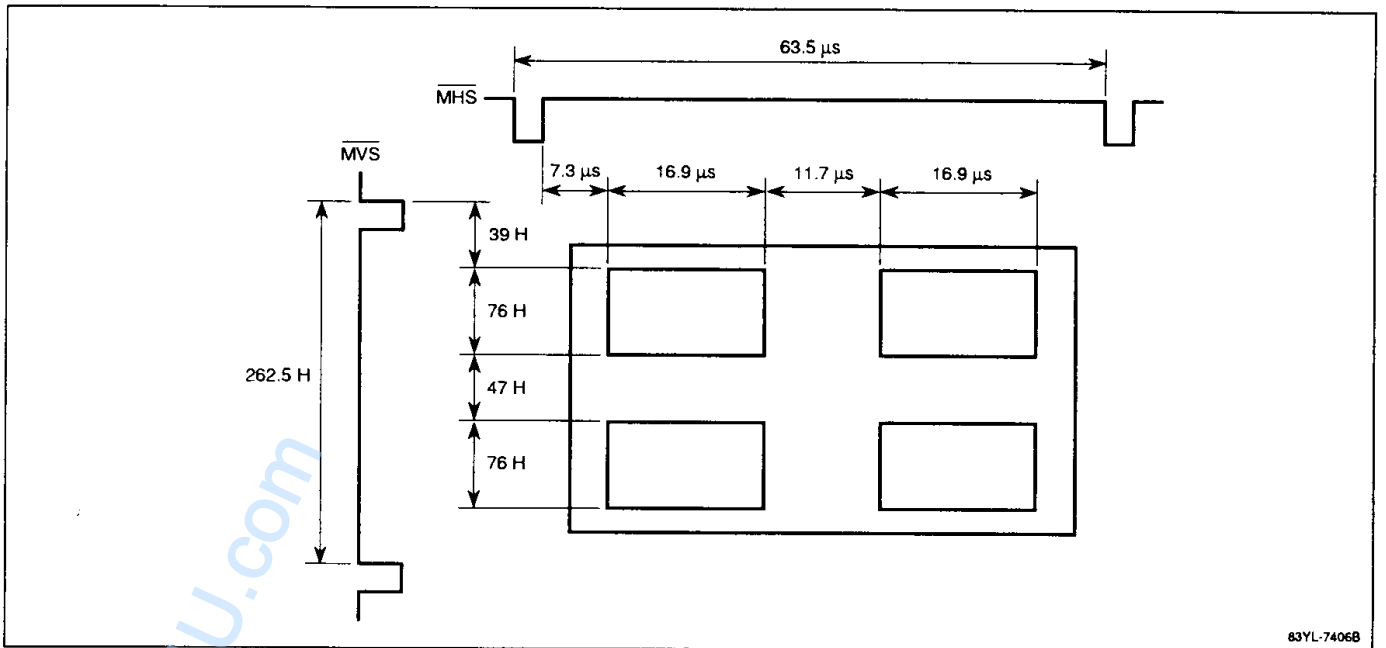


Figure 11. Subpicture Playback Area in PAL Applications with 80% Screen Display



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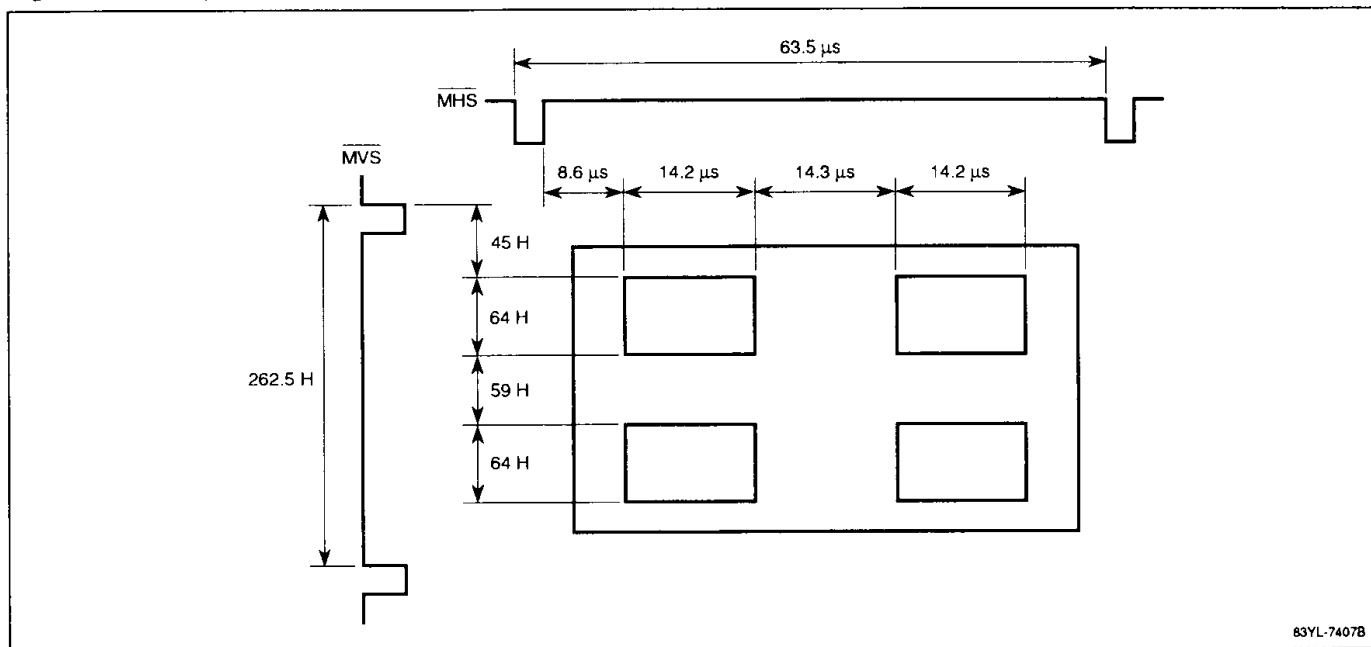
Figure 12. Subpicture Display Position in NTSC Applications with Full Screen Display



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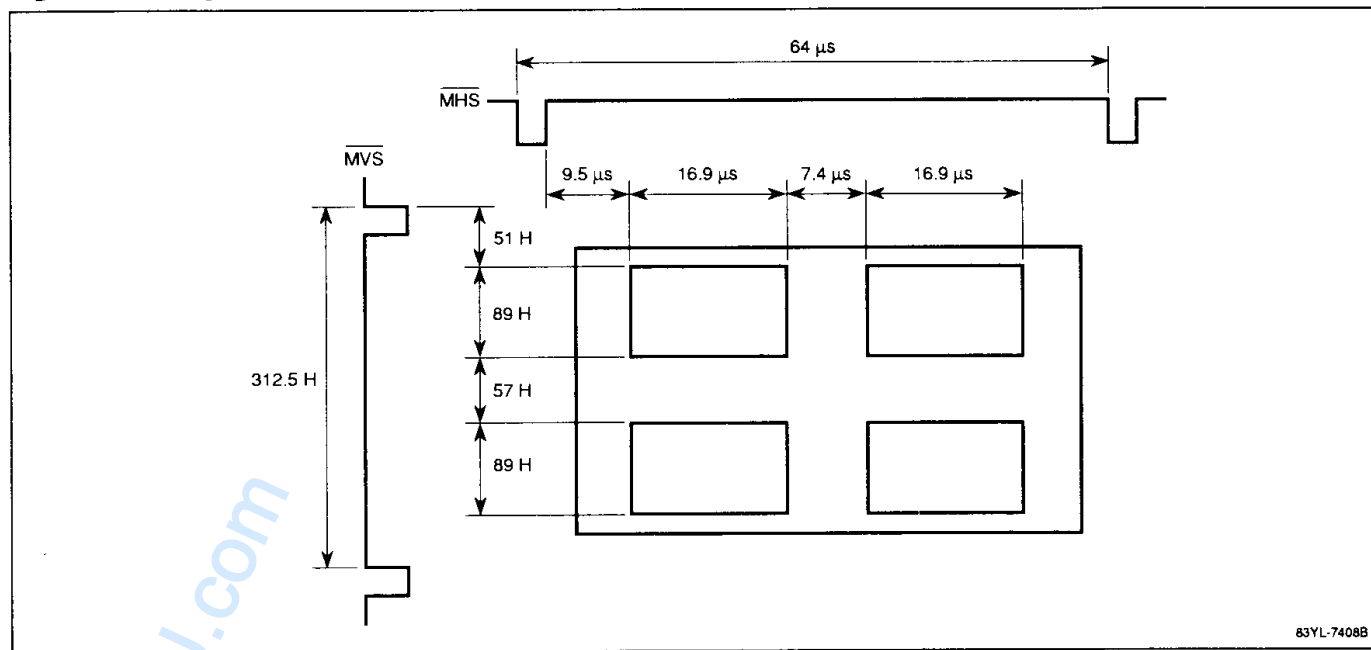
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Figure 13. Subpicture Display Position in NTSC Applications with 80% Screen Display



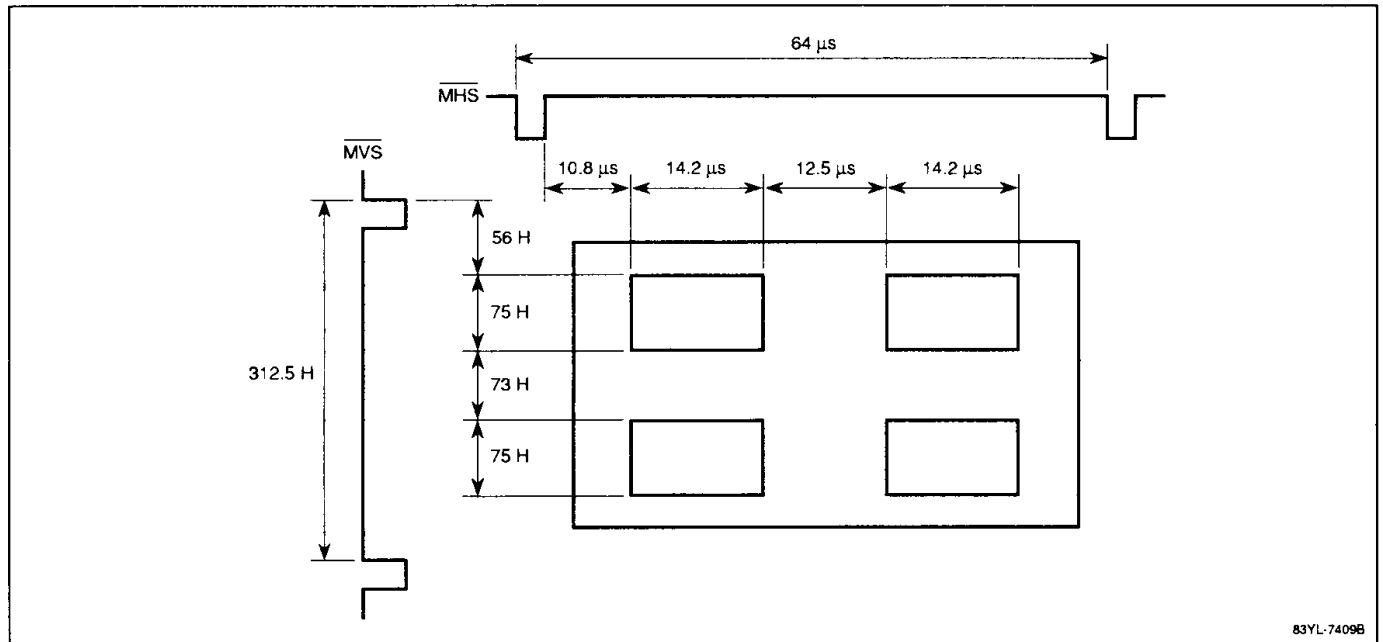
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Figure 14. Subpicture Display Position in PAL Applications with Full Screen Display



83YL-7408B

Figure 15. Subpicture Display Position with 80% Screen Display



Line Array Correction

Subpicture processing executes screen compression, in which the output data rate of the field memory is three times as high as the input data rate. A read cycle will catch up to, and then pass, a write cycle about midway on the screen. Afterward, old fields are read, and a field seam is produced where the two fields meet.

This problem is corrected during an old field read cycle by advancing the vertical address counter to its regular value and then incrementing it by one. The correction cycle varies depending on whether a main picture or subpicture field (odd versus even) field is involved (tables 6 and 7).

Table 6. Outrunning When the Main Picture and Subpicture Have the Same Fields

Main Picture	Subpicture	
	Odd	Even
Odd	— (before outrunning)	— (after outrunning)
Even	+ 1 (after outrunning)	— (before outrunning)

Notes:

- (1) + = address counter is incremented to its normal value plus 1.
- (2) — = no operation.

Table 7. Outrunning When the Main Picture and Subpicture Have Different Fields

Main Picture	Subpicture	
	Odd	Even
Odd	+ 1 (after outrunning)	— (before outrunning)
Even	+ 1 (before outrunning)	+ 1* (after outrunning)

Notes:

- (1) + = address counter is incremented to its normal value plus 1.
- (2) — = no operation.
- (3) * indicates that the address counter holds its status and is not incremented.

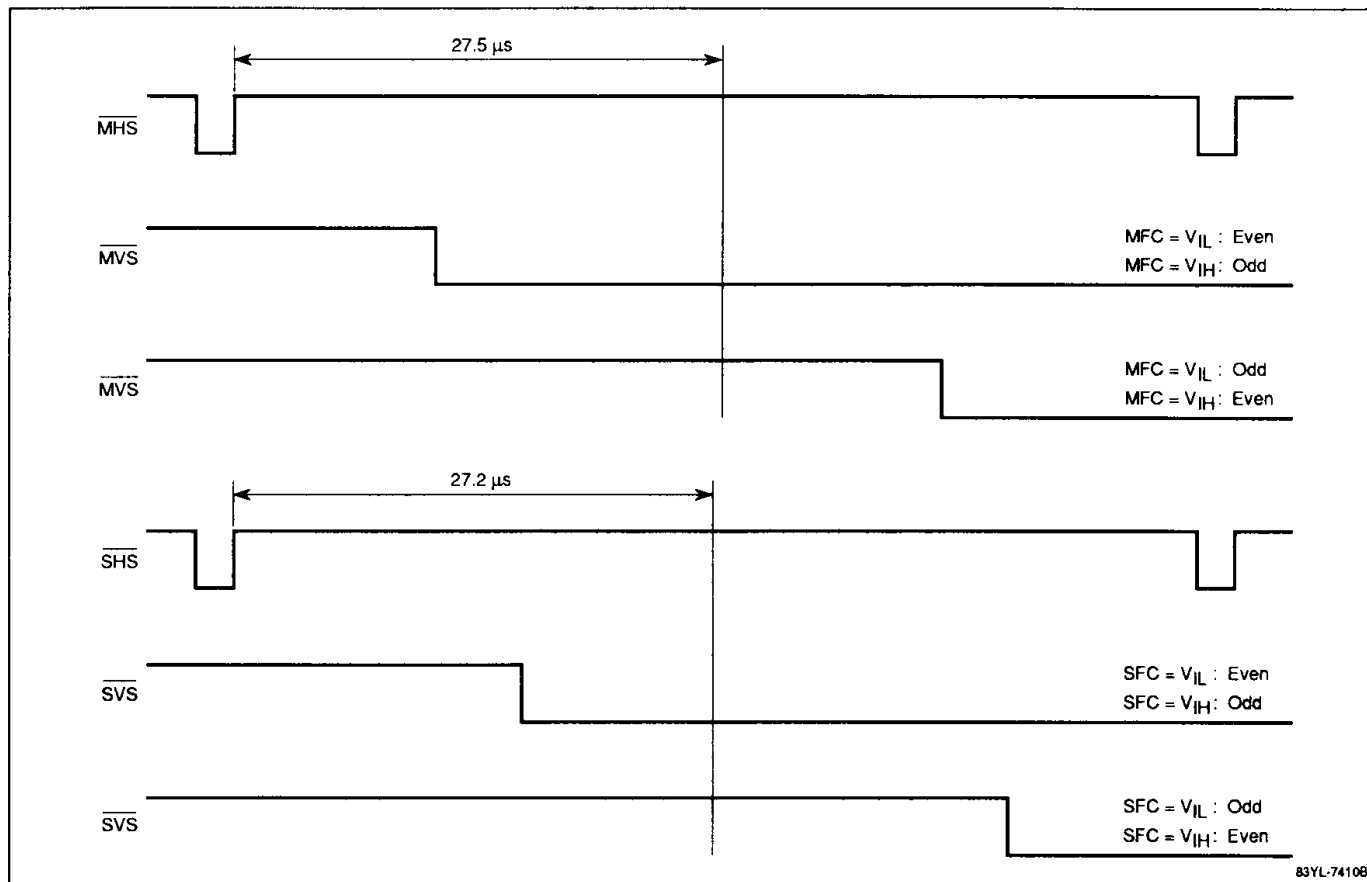
Field Distinction

The μPD4227x executes line offset sampling and line array correction. The former offsets write lines between the even and odd fields by one line. The latter advances the vertical read address counter to its normal value plus one by combining the main picture and subpicture fields. This prevents a seam line from appearing on the subpicture when part of it is displaying one field and the rest is displaying the other field.

In both cases, the μPD4227x executes field distinction to learn the status (odd or even) of the main picture and subpicture signals. The result is determined by the phase differences between MHS/SHS and MVS/SVS and by the state of MFC and SFC (figure 16).

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Figure 16. Field Distinction



Frame Signal Generation

The μPD42272 contains the data for four colors: white, yellow, light blue, and green. These colors are used for frame signals and are selected by the FC₀ and FC₁ frame color selection input signals. The data selector

switches the subpicture to the frame signal and then outputs it. The vertical width of the frame signal is one line; the horizontal width of 220 ns is determined by the YDACK, RDACK, and BDACK D/A clocks and the blanking signal (figure 17).

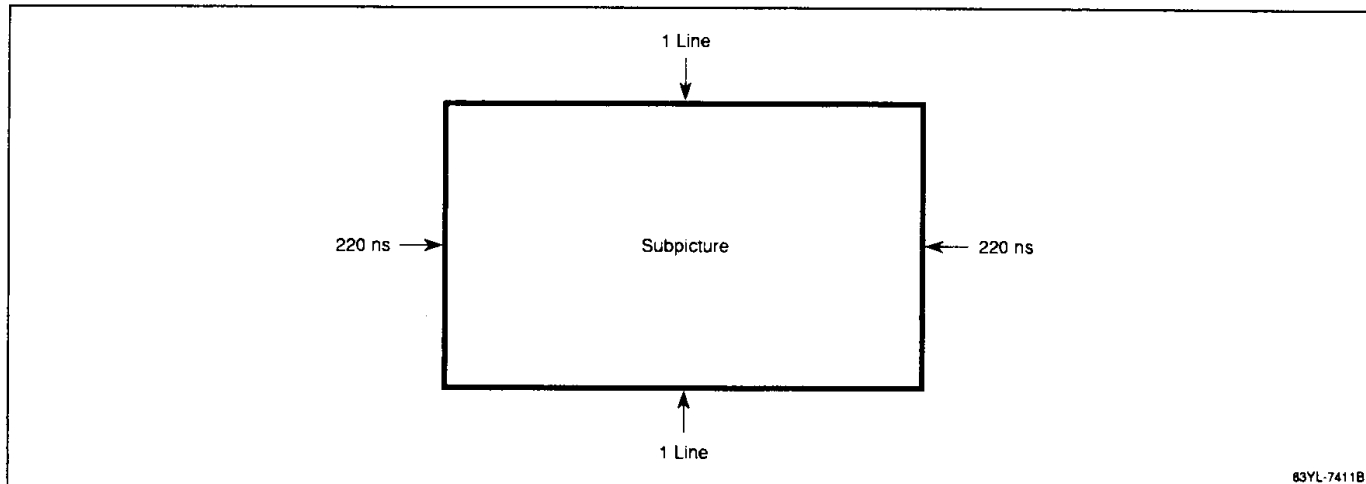
Table 8. Frame Signal Generation

Color:	Signal																	
	Y						R-Y						B-Y					
	DO ₅	DO ₄	DO ₃	DO ₂	DO ₁	DO ₀	DO ₅	DO ₄	DO ₃	DO ₂	DO ₁	DO ₀	DO ₅	DO ₄	DO ₃	DO ₂	DO ₁	DO ₀
White	1	0	1	0	1	1	1	0	0	0	0	0	1	0	0	0	0	0
Yellow	1	0	0	1	1	0	1	0	0	0	1	1	0	0	1	1	0	1
Light blue	0	1	1	1	1	0	0	0	1	1	0	1	1	0	0	1	1	1
Green	0	1	1	0	1	0	0	1	0	0	0	0	0	1	0	0	1	1

The μPD4227x writes the Y, R-Y, B-Y subpicture signals serially using the μPC661, a six-bit A/D converter with analog switching. For read operation, the R-Y and B-Y signal sampling phases are reversed. For the output signals, there is a 180° phase difference between the R-Y and B-Y signals. Frame signals containing phase

differences that are similarly output cause gradation because the frame signals deviate at the edges. To prevent this deviation, the μPD42272 aligns the edges of the frame signal by adjusting RDACK and BDACK during the frame signal output period (figure 18).

Figure 17. Frame Signal



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Data Output

Subpicture signals are compressed to the scale of 1:9 (horizontal = 1:3 and vertical = 1:3) and then output through the DOY, DOR, and DOB output pins. The output period is about one-ninth of one field period of the main picture, or 16.7 ms. DOY, DOR, and DOB are in high impedance for the remaining eight-ninths of the period and no data is output (figure 19).

The signal level of the high impedance period must meet the pedestal level, i.e., the level of the initial input signal. The signal level is determined by resistors that pull up or down the DOY, DOR, and DOB pins. In the μPD4227x, the D/A converter clocks are output cyclically (every 2.25 MHz) during the no signal period. The μPD6901 six-bit D/A converter converts into analog data the data determined by pull-up or pull-down resistors, enabling the signal to be at a constant level.

The input signal pedestal level is determined at clamp levels of the μPC661 six-bit A/D converter. For the μPD661, the Y signal clamp output is the R-Y and B-Y output. All Y outputs are thus pulled down. For R-Y and B-Y output, only DOR₅ and DOB₅ are pulled up, respectively, and the other outputs are pulled down (figures 20 and 21).

Outside Control

Specified Frame Color. The μPD42272 can generate one of four frame colors (white, yellow, light blue, and green) depending on the levels of FC₀ and FC₁ (table 9).

Table 9. Frame Color Input Levels

Pin	White	Light Blue	Yellow	Green
FC0	H	L	H	L
FC1	H	H	L	L

Specified Subpicture Size. The μPD4227x can select one of two subpicture sizes using the SIZE subpicture selection input. When its input level is high, the display area is set to one-ninth of the main picture (full screen display). A low level sets the display area to one-twelfth, or 80%, of the main picture.

Specified Subpicture Position. The μPD4227x can select one of four subpicture display positions (one of the four corners on the main picture) using a combination of signals from the VPS and HPS position selection input pins (table 10).

Table 10. VPS and HPS Input Levels

Pin	Top Left	Bottom Left	Top Right	Bottom Right
VPS	H	L	H	L
HPS	H	H	L	L

Specified Still Picture. The μPD4227x can display a still subpicture using the still picture request input. When the level of STILL is high, a freeze frame picture is displayed. When the input level is low, the moving picture is selected.

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Figure 18. Frame Signal Alignment

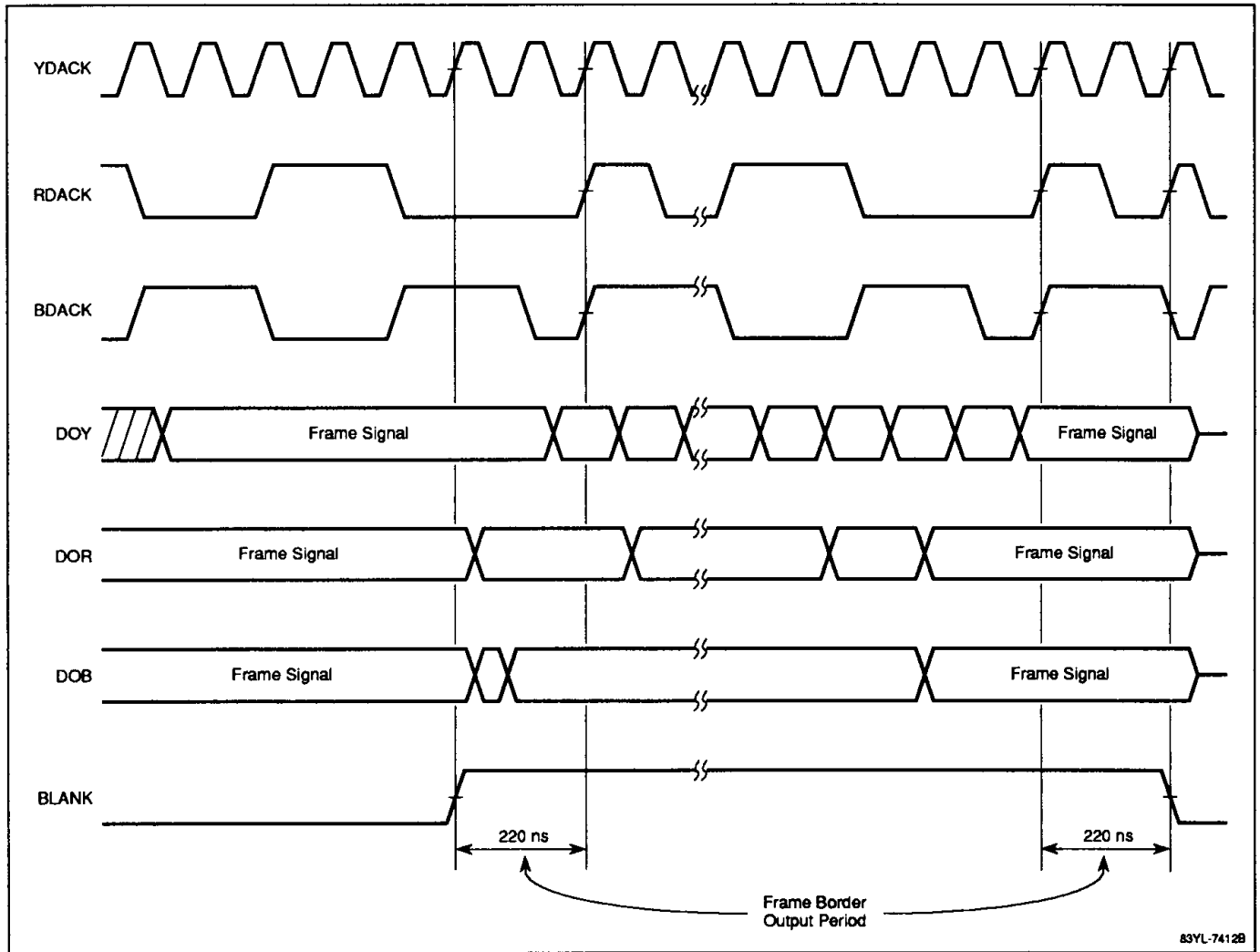


Figure 19. Subpicture Data Output

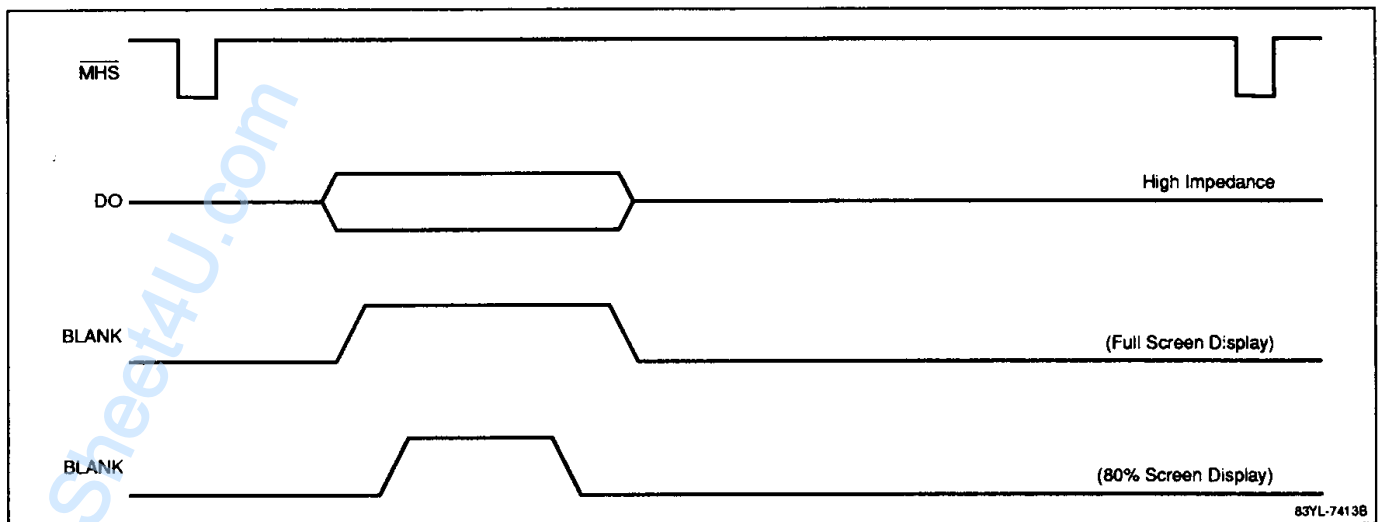
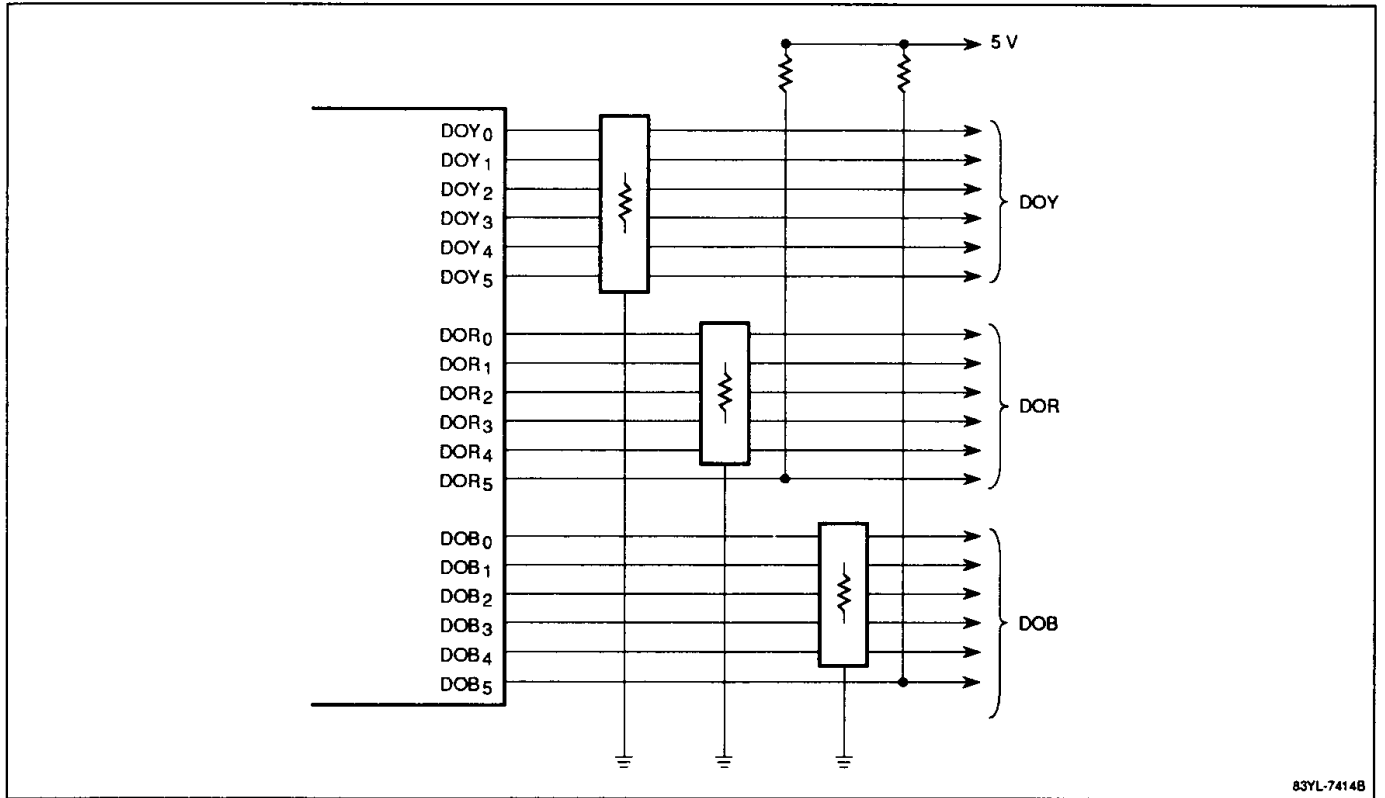
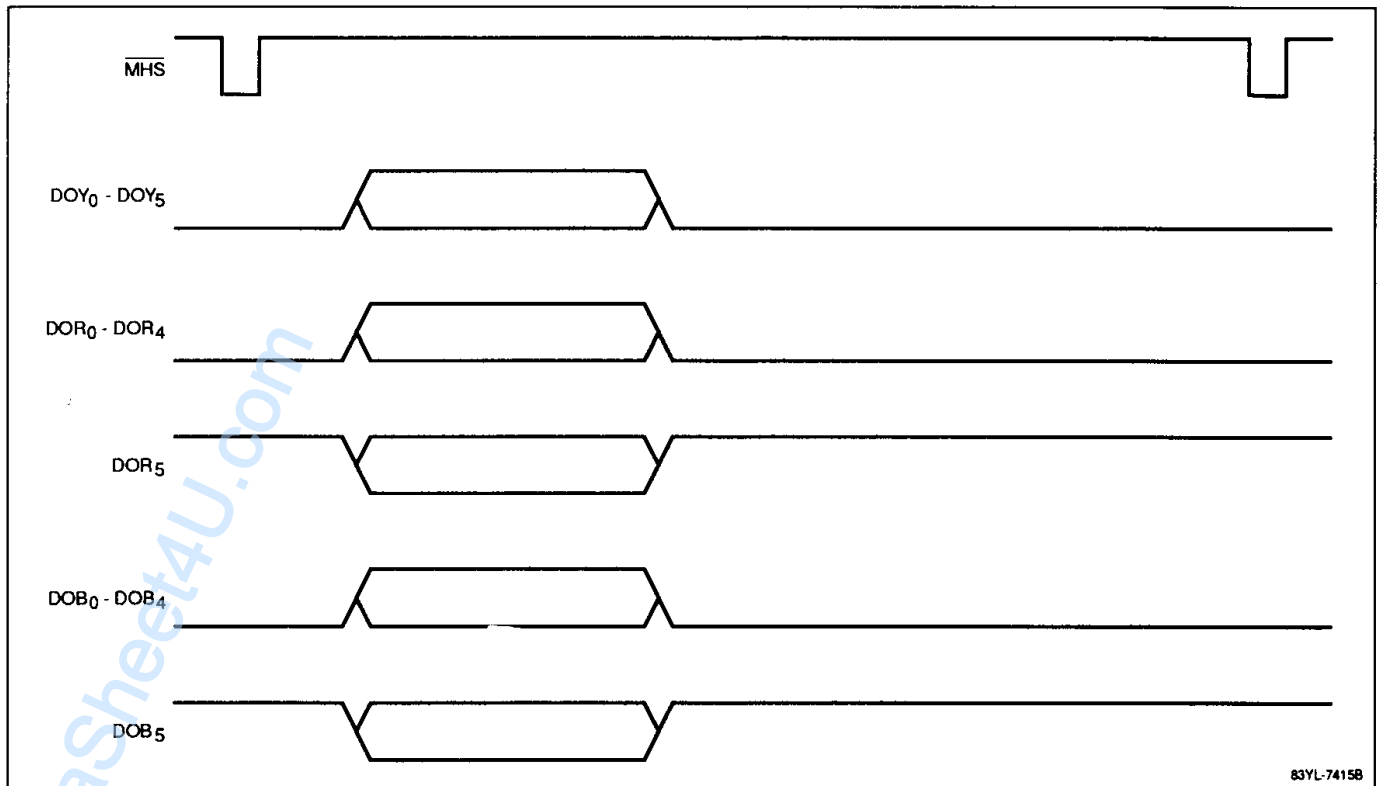


Figure 20. Data Output Signal Adjustment



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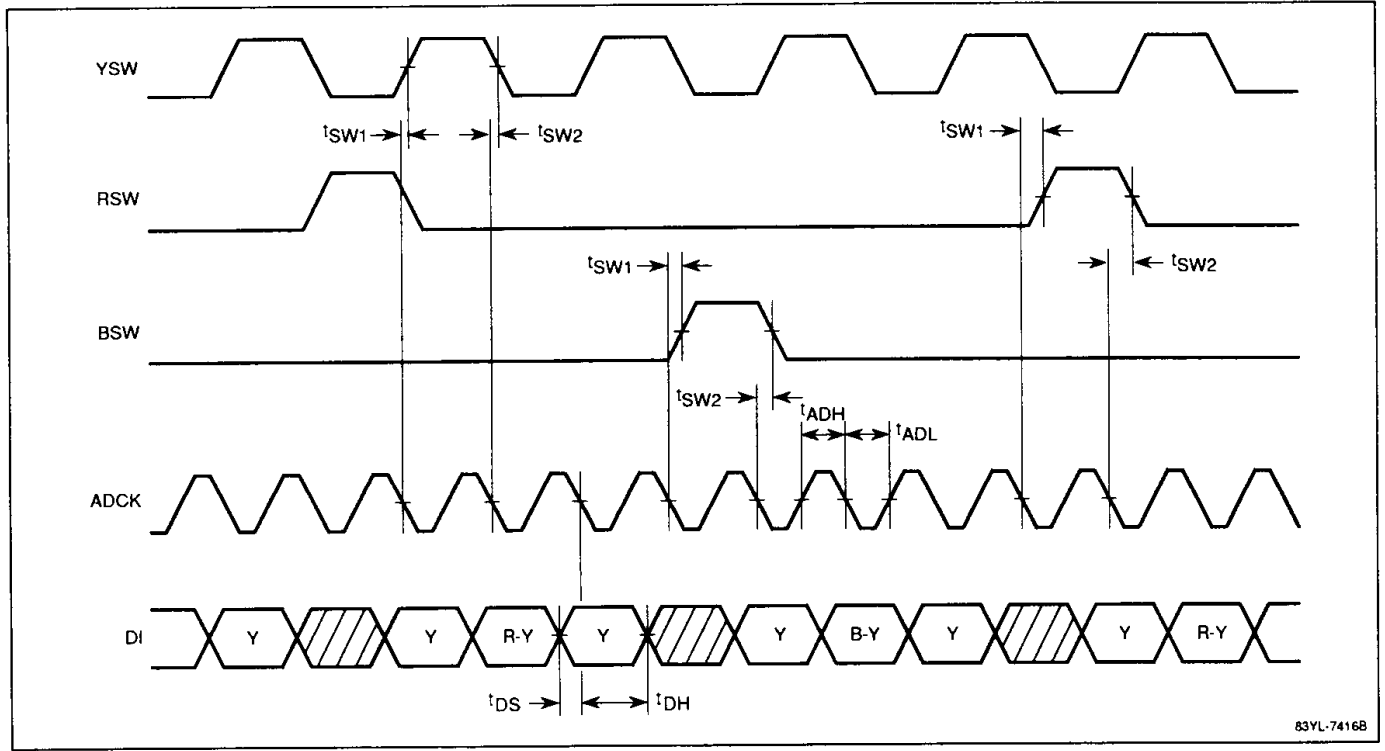
Figure 21. R-Y and B-Y Output Signal Adjustment



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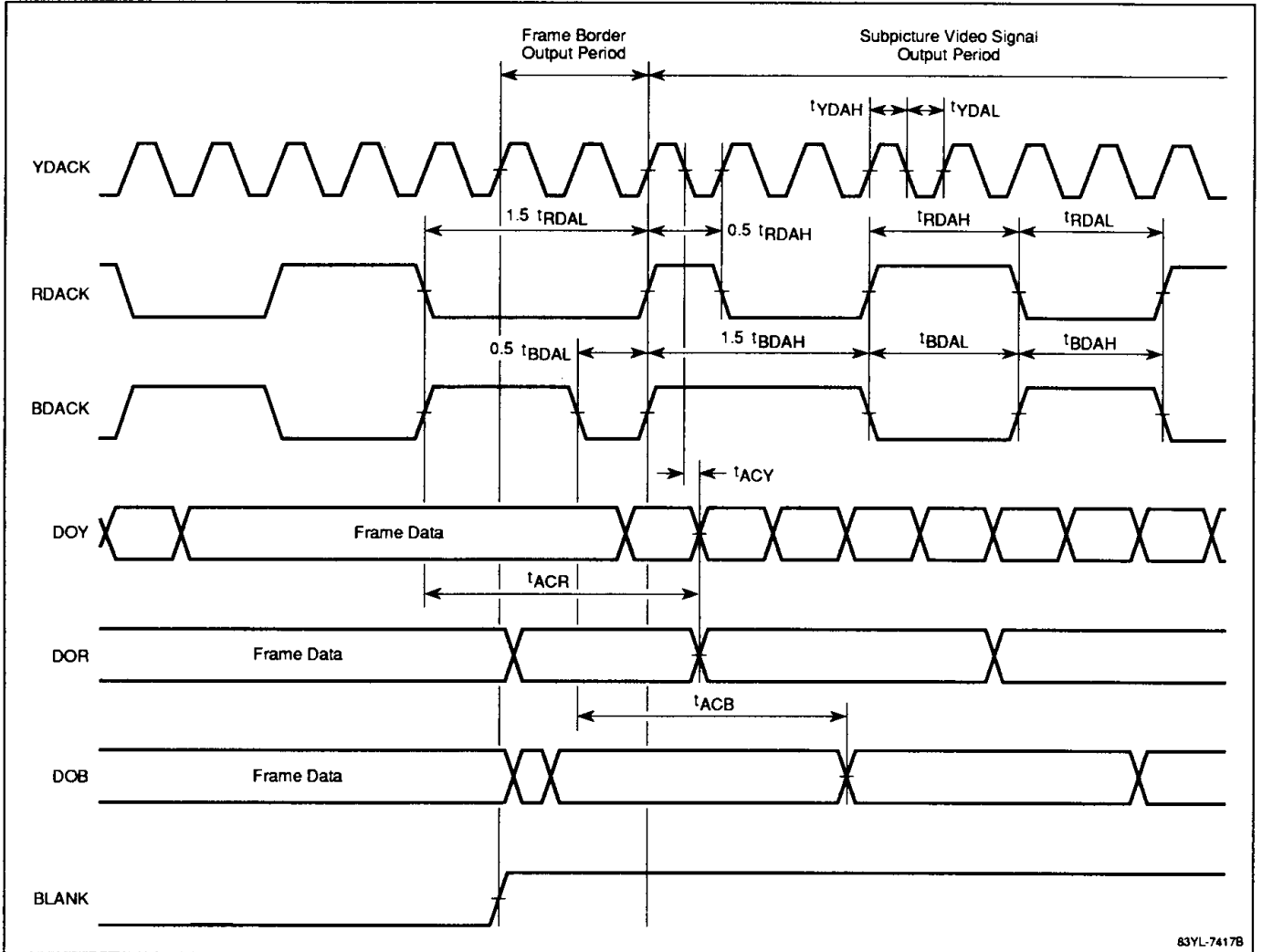
Timing Waveforms

Input Timing



Timing Waveforms (cont)

Output Timing



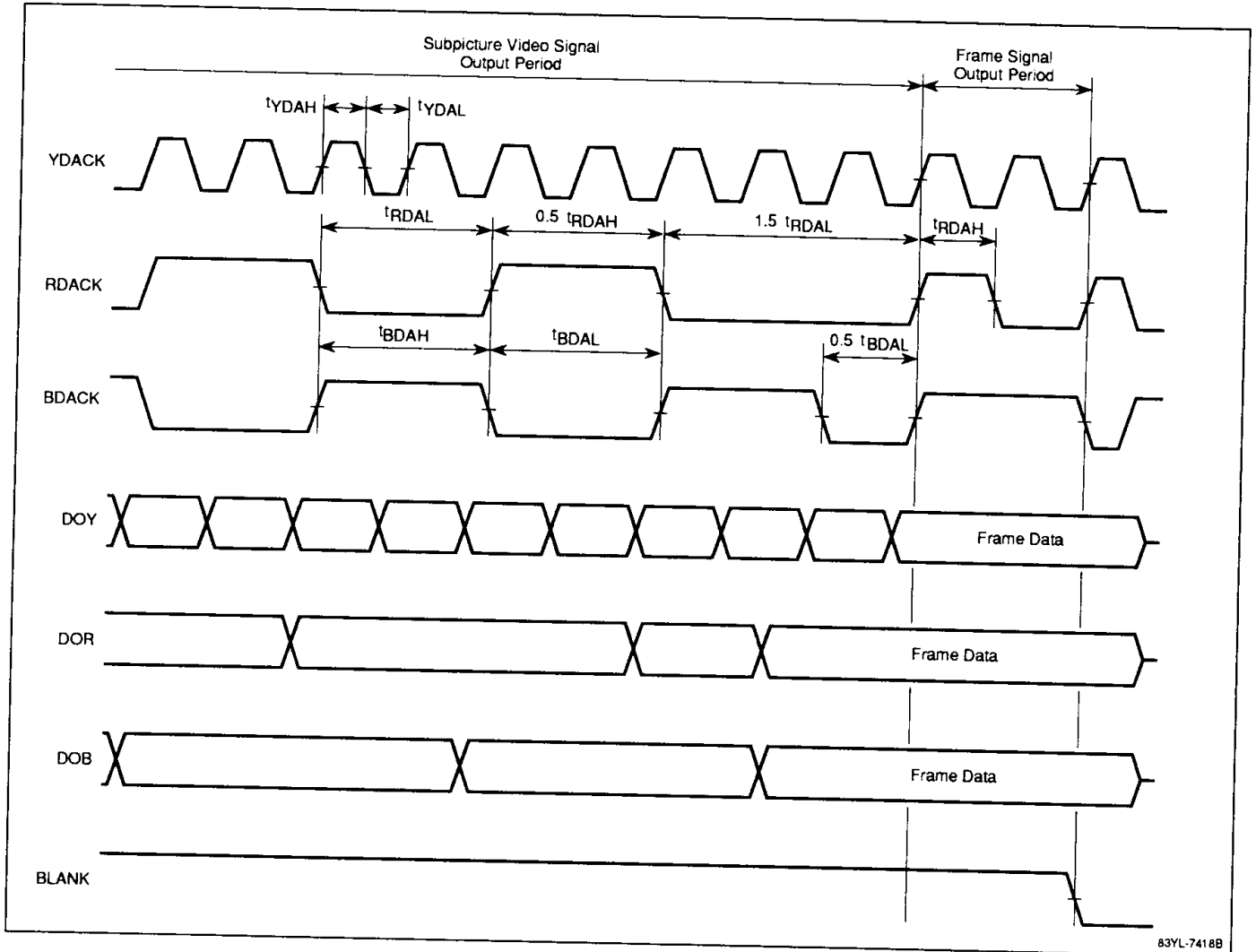
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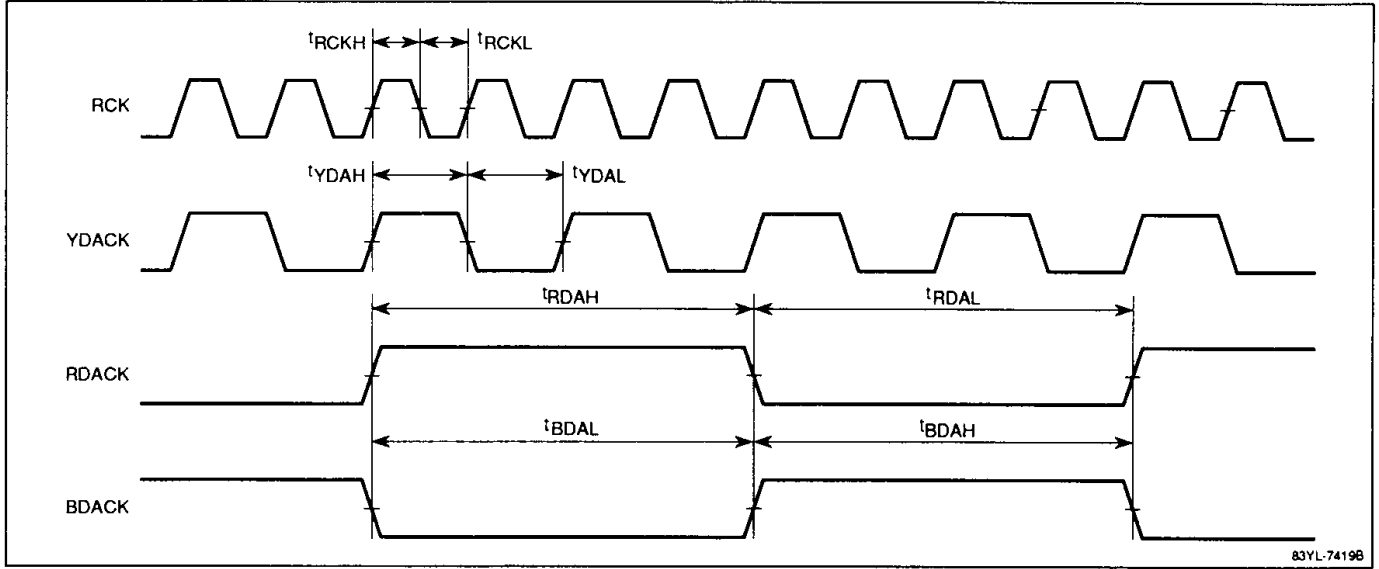
Timing Waveforms (cont)

Output Timing 2



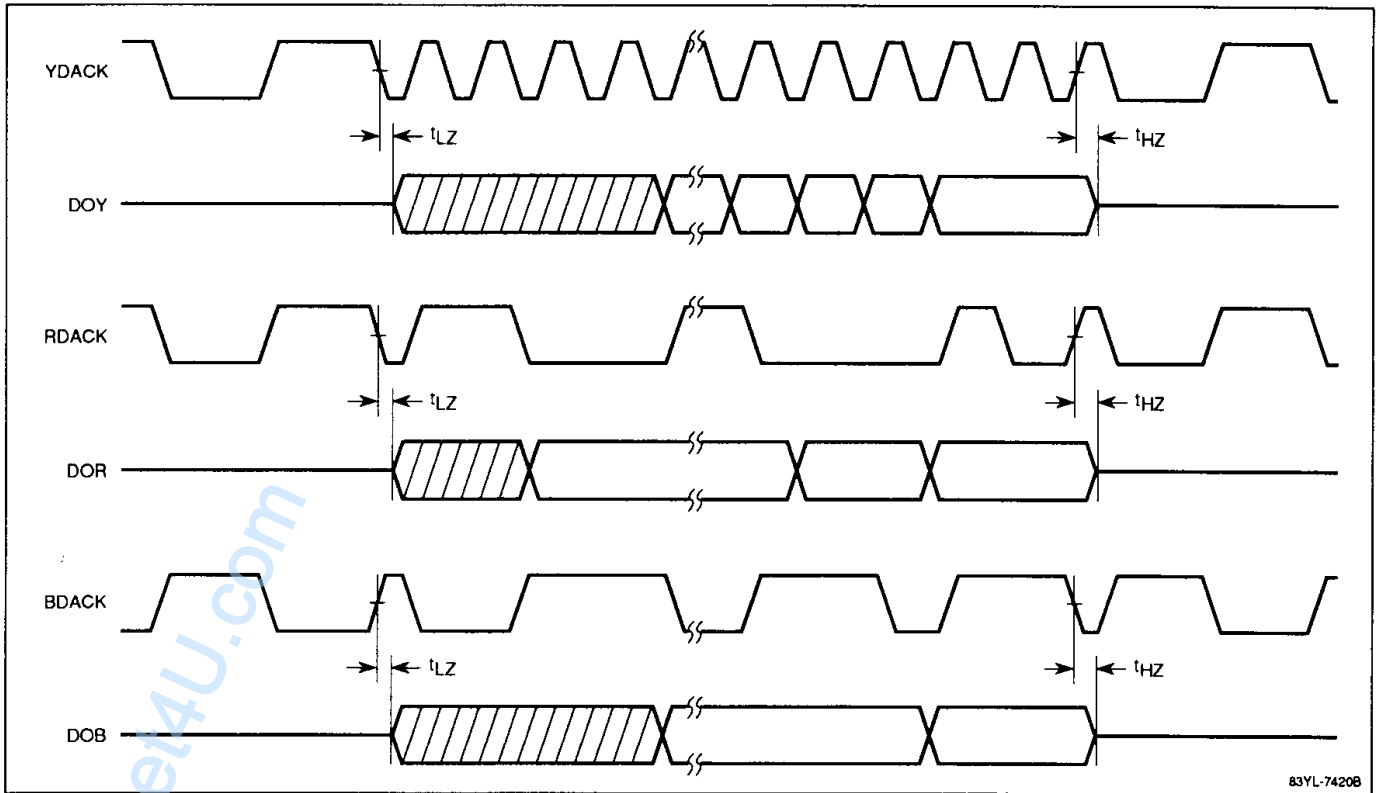
Timing Waveforms (cont)

Output Timing 3



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Output Timing 4



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