



MOS INTEGRATED CIRCUIT

μ PD42S4260, 424260

4 M-BIT DYNAMIC RAM

256 K-WORD BY 16-BIT, FAST PAGE MODE, BYTE READ/WRITE MODE

DESCRIPTION

The μ PD42S4260, 424260 are 262 144 words by 16 bits dynamic CMOS RAMs with optional fast page mode and byte read/write mode.

High performance CMOS sense amplifier, peripheral circuits and one transistor dynamic memory cell technique realize high speed access and low power consumption.

In addition to this, refresh is accomplished by performing $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh on the μ PD42S4260.

The μ PD42S4260 and μ PD424260 are packaged in 44-pin plastic TSOP, 40-pin plastic SOJ and 40-pin plastic ZIP.

FEATURES

- 262 144 words by 16 bits organization
- Fast access and cycle time

Part number	Refresh cycle	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μ PD42S4260-70	512 cycles/128 ms	880.0 mW	70 ns	130 ns	45 ns
μ PD424260-70	512 cycles/ 8 ms				
μ PD42S4260-80	512 cycles/128 ms	797.5 mW	80 ns	150 ns	50 ns
μ PD424260-80	512 cycles/ 8 ms				

- Low power consumption
 - Standby (CMOS level input) 1.1 mW MAX. (μ PD42S4260)
 - 5.5 mW MAX. (μ PD424260)
- Single +5.0 V \pm 10 % power supply
- Fast page mode and byte read/write mode capability
- The μ PD42S4260 has 4 types of refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{RAS}}$ only refresh, hidden refresh and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
- The μ PD424260 has 3 types of refresh
 - $\overline{\text{RAS}}$ only refresh, hidden refresh and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
- Multiplexed address inputs Row address: A0 to A8, Column address: A0 to A8
- On-chip substrate bias generator

The information in this document is subject to change without notice.

The mark ★ shows revised points.

★ ORDERING INFORMATION

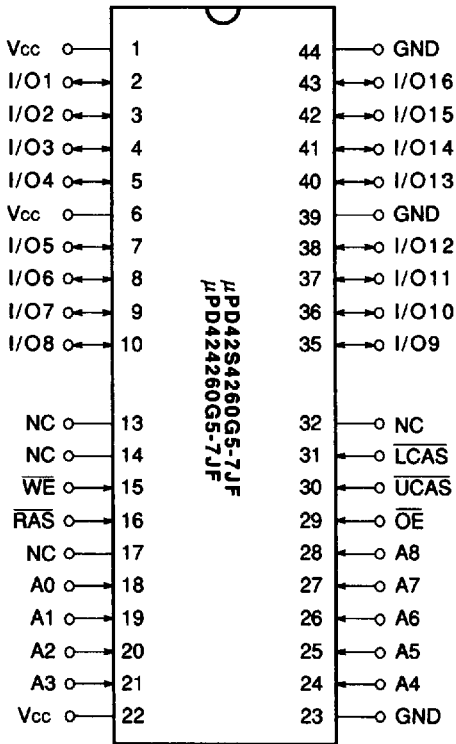
Part number	Access time (MAX.)	Package	Refresh
μPD42S4260G5-70-7JF	70 ns	44-pin Plastic TSOP	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{RAS}}$ only refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh hidden refresh
μPD42S4260G5-80-7JF	80 ns		
μPD42S4260G5-70-7KF	70 ns	44-pin Plastic TSOP (Reverse bent)	
μPD42S4260G5-80-7KF	80 ns		
μPD42S4260LE-70	70 ns	40-pin Plastic SOJ	
μPD42S4260LE-80	80 ns		
μPD42S4260V-70	70 ns	40-pin Plastic ZIP	
μPD42S4260V-80	80 ns		
μPD424260G5-70-7JF	70 ns	44-pin Plastic TSOP	$\overline{\text{RAS}}$ only refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh hidden refresh
μPD424260G5-80-7JF	80 ns		
μPD424260G5-70-7KF	70 ns	44-pin Plastic TSOP (Reverse bent)	
μPD424260G5-80-7KF	80 ns		
μPD424260LE-70	70 ns	40-pin Plastic SOJ	
μPD424260LE-80	80 ns		
μPD424260V-70	70 ns	40-pin Plastic ZIP	
μPD424260V-80	80 ns		

QUALITY GRADE
STANDARD

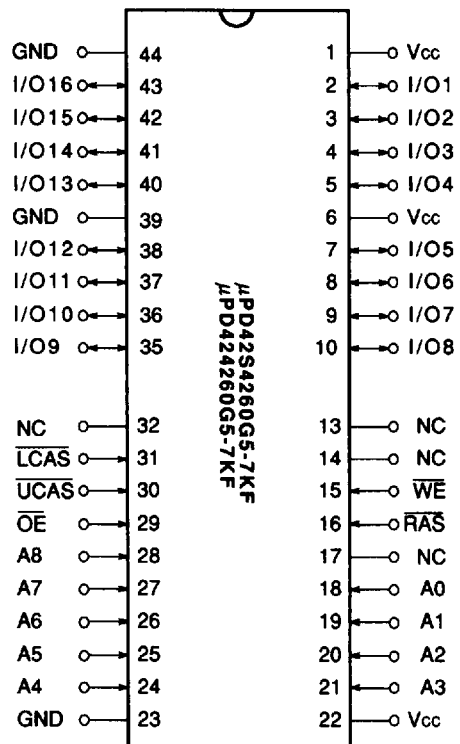
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PIN CONFIGURATIONS

44-pin Plastic TSOP
(Marking Side)

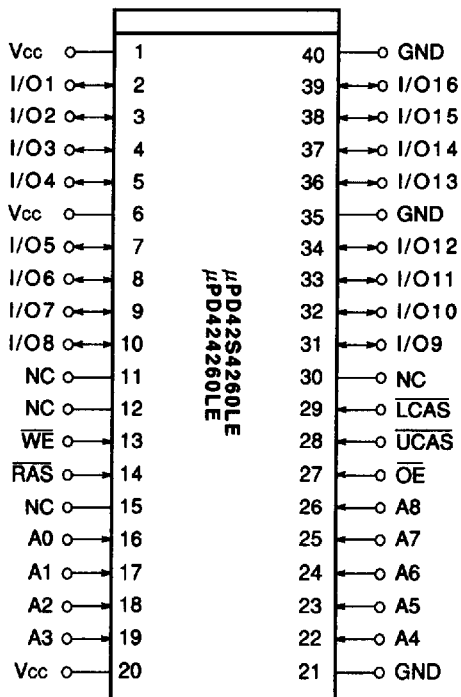


44-pin Plastic TSOP (Reverse bent)
(Marking Side)

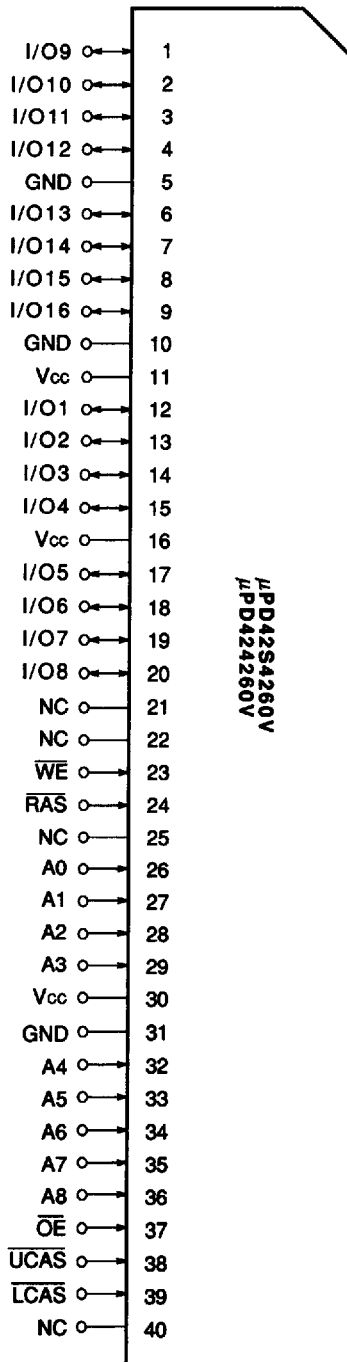


- A0 to A8 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- RAS : Row Address Strobe
- UCAS : Column Address Strobe (upper)
- LCAS : Column Address Strobe (lower)
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply (+5.0 V ± 10 %)
- GND : Ground
- NC : No Connection

40-pin Plastic SOJ
(Top View)



40-pin Plastic ZIP
(Front View)



- A0 to A8 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- RAS : Row Address Strobe
- UCAS : Column Address Strobe (upper)
- LCAS : Column Address Strobe (lower)
- WE : Write Enable
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- Vcc : Power Supply (+5.0 V ± 10 %)
- GND : Ground
- NC : No Connection



ELECTRICAL SPECIFICATIONS NOTE 1

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	RATING	UNIT
Voltage on Any Pin Relative to GND	V_T		-1.0 to +7.0	V
Supply Voltage	V_{CC}		-1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS NOTE 2, 3

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low Level Input Voltage	V_{IL}		-1.0		+0.8	V
Ambient Temperature	T_a		0		70	°C

CAPACITANCE ($T_a = +25\text{ °C}$, $f = 1\text{ MHz}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C_{I1}	A0 to A8			5	pF
	C_{I2}	\overline{RAS} , \overline{CAS} , \overline{WE} , \overline{OE}			7	pF
Data Input/Output Capacitance	C_D	I/O1 to I/O16			7	pF

★ DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	NOTE
Operating current		I _{CC1}	$\overline{RAS}, \overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$, $I_o = 0$ mA	$t_{RAC} = 70$ ns	160	mA	4, 5
				$t_{RAC} = 80$ ns	145		
Standby current	μPD42S4260	I _{CC2}	$V_{IH(MIN.)} \leq \overline{RAS}, \overline{CAS}$	$I_o = 0$ mA	2	mA	
			$V_{CC} - 0.2$ V $\leq \overline{RAS}, \overline{CAS}$	$I_o = 0$ mA	0.2		
	μPD424260		$V_{IH(MIN.)} \leq \overline{RAS}, \overline{CAS}$	$I_o = 0$ mA	2		
			$V_{CC} - 0.2$ V $\leq \overline{RAS}, \overline{CAS}$	$I_o = 0$ mA	1		
RAS only refresh current		I _{CC3}	RAS Cycling, $V_{IH(MIN.)} \leq \overline{CAS}$ $t_{RC} = t_{RC(MIN.)}$, $I_o = 0$ mA	$t_{RAC} = 70$ ns	160	mA	4, 5
	$t_{RAC} = 80$ ns			145			
Operating current (Fast page mode)		I _{CC4}	RAS $\leq V_{IL(MAX.)}$ CAS Cycling, $t_{PC} = t_{PC(MIN.)}$, $I_o = 0$ mA	$t_{RAC} = 70$ ns	140	mA	4, 5
				$t_{RAC} = 80$ ns	130		
CAS before RAS refresh current		I _{CC5}	RAS Cycling, $t_{RC} = t_{RC(MIN.)}$, $I_o = 0$ mA	$t_{RAC} = 70$ ns	160	mA	4, 5
				$t_{RAC} = 80$ ns	145		
CAS before RAS long refresh current (512 cycles/128 ms, only for μPD42S4260)		I _{CC6}	Standby : $V_{CC} - 0.2$ V $\leq \overline{RAS}$ $V_{CC} - 0.2$ V $\leq \overline{CAS}$ or $\overline{CAS} \leq 0.2$ V CAS before RAS refresh : 512 cycles/128 ms $\overline{RAS}, \overline{CAS} : 0$ V $\leq V_{IL} \leq 0.2$ V $V_{CC} - 0.2$ V $\leq V_{IH} \leq V_{IH(MAX.)}$ $\overline{WE}, \overline{OE} : V_{IH}$ Address input : V_{IH} or V_{IL} Output : Hi-Z	$t_{RAS} \leq 200$ ns	200	μA	4, 5
				$t_{RAS} \leq 1$ μs	300		
Self refresh current (CAS before RAS self refresh, only for μPD42S4260)		I _{CC7}	$I_o = 0$ mA $\overline{RAS}, \overline{CAS} : 0$ V $\leq V_{IL} \leq 0.2$ V $V_{CC} - 0.2$ V $\leq V_{IH} \leq V_{IH(MAX.)}$		150	μA	
Input leakage current		I _{I(L)}	$V_I = 0$ to 5.5 V all other pins except for testing pin = 0 V	-10	+10	μA	
Output leakage current		I _{O(L)}	Output is disabled (Hi-Z) $V_O = 0$ to 5.5 V	-10	+10	μA	
High level output voltage		V _{OH}	$I_o = -2.5$ mA	2.4		V	
Low level output voltage		V _{OL}	$I_o = 2.1$ mA		0.4	V	

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted) NOTE 6, 7

(1/2)



PARAMETER	SYMBOL	t _{RAC} = 70 ns		t _{RAC} = 80 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t _{RC}	130		150		ns	8
Read Modify Write Cycle Time	t _{RWC}	175		200		ns	8
Fast Page Mode Cycle Time	t _{PC}	45		50		ns	8
Read Modify Write Cycle Time (Fast Page Mode)	t _{PRWC}	90		105		ns	8
Access Time from $\overline{\text{RAS}}$	t _{RAC}		70		80	ns	9, 10
Access Time from $\overline{\text{CAS}}$	t _{CAC}		20		20	ns	9, 10
Access Time from Column Address	t _{AA}		35		40	ns	9, 10
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		40		45	ns	10
$\overline{\text{CAS}}$ to Output Data Setup Time	t _{CLZ}	0		0		ns	10
Output Buffer Turn-off Delay Time ($\overline{\text{CAS}}$)	t _{OFF}	0	15	0	20	ns	11
Transition Time (rise and fall)	t _T	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	50		60		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	70	10 000	80	10 000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	70	125 000	80	125 000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	20		20		ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	70		80		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	20	10 000	20	10 000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	50	20	60	ns	9
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	35	15	40	ns	9
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10		10		ns	12
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		ns	
Row Address Setup Time	t _{ASR}	0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		ns	
Column Address Setup Time	t _{ASC}	0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	15		15		ns	14
Write Command Pulse Width	t _{WP}	15		15		ns	14
Write Command Lead Time Referenced to $\overline{\text{RAS}}$	t _{RWL}	20		25		ns	
Write Command Lead Time Referenced to $\overline{\text{CAS}}$	t _{CWL}	15		20		ns	
Data-in Setup Time	t _{DS}	0		0		ns	15
Data-in Hold Time	t _{DH}	15		20		ns	15

(2/2)

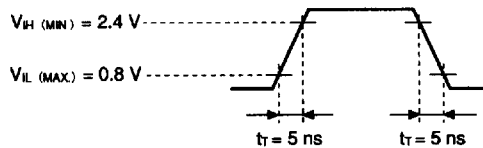
PARAMETER		SYMBOL	t _{TRAC} = 70 ns		t _{TRAC} = 80 ns		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
Refresh Time	μPD42S4260	t _{REF}		128		128	ms	17
	μPD424260			8		8	ms	
Write Command Setup Time		t _{WCS}	0		0		ns	16
CAS to WE Delay Time		t _{CWD}	40		45		ns	16
RAS to WE Delay Time		t _{RWD}	90		105		ns	16
CAS Precharge Delay Time Referenced to WE (Fast Page Mode)		t _{CPWD}	60		70		ns	16
Column Address Delay Time Referenced to WE		t _{AWD}	55		65		ns	16
CAS Setup Time (CAS before RAS Refresh)		t _{CSR}	10		10		ns	
CAS Hold Time (CAS before RAS Refresh)		t _{CHR}	15		15		ns	
RAS Precharge to CAS Hold Time		t _{RPC}	10		10		ns	
OE to RAS inactive Setup Time		t _{OES}	0		0		ns	
Access Time from OE		t _{OEA}		20		20	ns	
OE Data Delay Time		t _{OED}	15		20		ns	
Output Buffer Turn-off Delay Time (OE)		t _{OEZ}	0	15	0	20	ns	11
OE Output Data Setup Time		t _{OLZ}	0		0		ns	
OE Hold Time		t _{OEH}	0		0		ns	
RAS Hold Time Referenced to CAS Precharge		t _{RHCP}	40		45		ns	
Masked Byte Write Hold Time referenced to RAS		t _{MRH}	0		0		ns	
RAS Pulse Width (CAS before RAS Self Refresh)		t _{RASS}	100		100		μs	17
RAS Precharge Time (CAS before RAS Self Refresh)		t _{RPS}	130		150		ns	17
CAS Hold Time (CAS before RAS Self Refresh)		t _{CHS}	-50		-50		ns	17



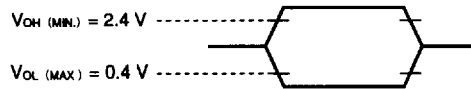
NOTES

1. CAS means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
2. All voltages are referenced to GND.
3. An initial pause of 100 μs is required after power up followed by 8 $\overline{\text{RAS}}$ only refresh cycles before proper device operation is achieved. In case of using internal address refresh counter, a minimum of 8 CAS before $\overline{\text{RAS}}$ refresh cycles instead of 8 $\overline{\text{RAS}}$ only refresh cycles are required.
4. I_{CC1} , I_{CC3} , I_{CC4} , I_{CC5} and I_{CC6} depend on t_{RC} and t_{PC} . Specified values are obtained with outputs open.
5. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$ and $\text{CAS} = V_{IH}$.
6. AC measurements assume $t_T = 5 \text{ ns}$.
7. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



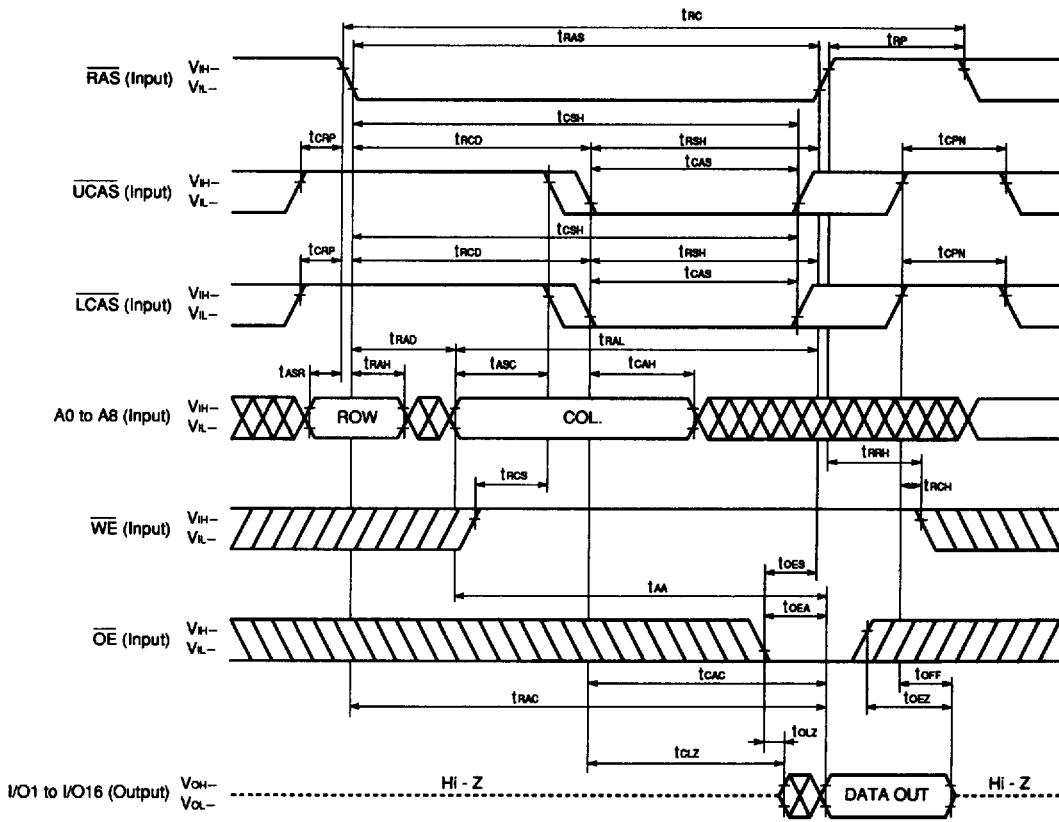
8. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($T_a = 0$ to 70°C) is assured.
9. In random read cycle, the access time is changed by the conditions of t_{RAD} and t_{RCD} as follows.

CONDITION	ACCESS TIME
$t_{RAD} \leq t_{RAD}(\text{MAX.})$ and $t_{RCD} \leq t_{RCD}(\text{MAX.})$	$t_{RAC}(\text{MAX.})$
$t_{RAD}(\text{MAX.}) \leq t_{RAD}$ and $t_{RCD} \leq t_{RCD}(\text{MAX.})$	$t_{AA}(\text{MAX.})$
$t_{RCD}(\text{MAX.}) \leq t_{RCD}$	$t_{CAC}(\text{MAX.})$

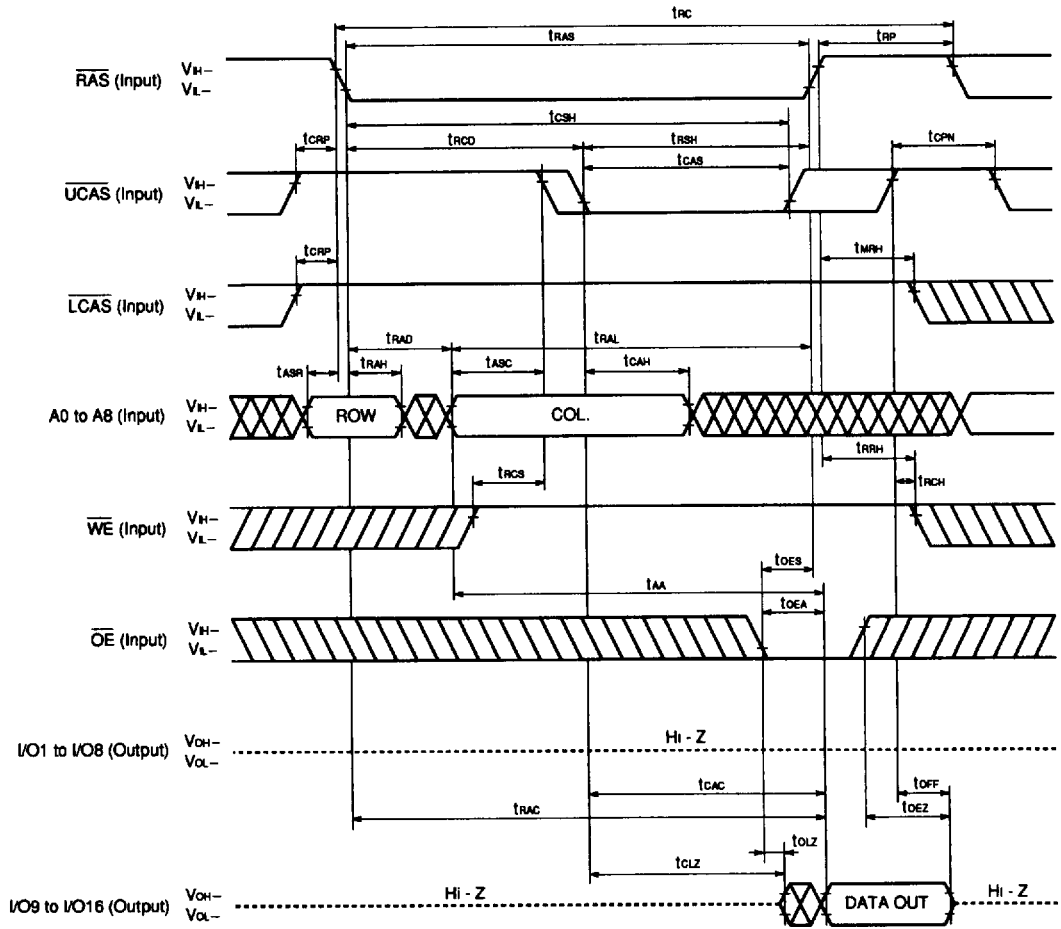
$t_{RAD}(\text{MAX.})$ and $t_{RCD}(\text{MAX.})$ indicate the point which the access time changes and are not the limits of operation.

10. Loading conditions are 1TTL and 100 pF.
11. $t_{OFF}(\text{MAX.})$ and $t_{OEZ}(\text{MAX.})$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL} .
12. $t_{CRP}(\text{MIN.})$ requirement should be applicable for $\overline{\text{RAS/CAS}}$ cycles preceded by any cycles.
13. Either $t_{RCH}(\text{MIN.})$ or $t_{RRH}(\text{MIN.})$ must be satisfied for a read cycle.
14. $t_{WP}(\text{MIN.})$ is applicable for late write cycle or read modify write cycle. In early write cycles, $t_{WCH}(\text{MIN.})$ should be satisfied.
15. This specification is referenced to $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{WE}}$ falling edge in late write or read modify write cycles.
16. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS}(\text{MIN.}) \leq t_{WCS}$, the cycle is an early write cycle and the data out pins will remain Hi-Z through the entire cycle. If $t_{RWD}(\text{MIN.}) \leq t_{RWD}$, $t_{CWD}(\text{MIN.}) \leq t_{CWD}$, $t_{AWD}(\text{MIN.}) \leq t_{AWD}$, $t_{CPWD}(\text{MIN.}) \leq t_{CPWD}$, the cycle is a read modify write cycle and condition of the data out (at access time) is indeterminate.
17. This specification is applicable only for μPD42S4260.

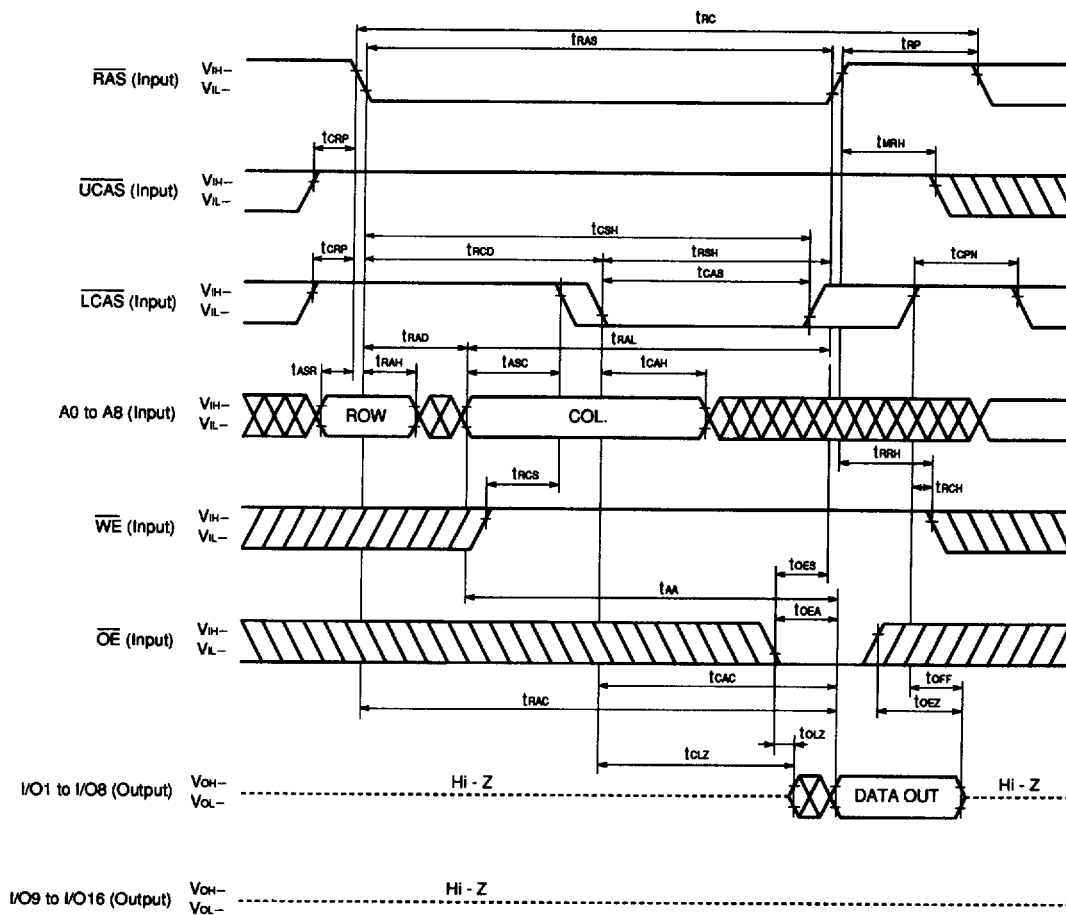
READ CYCLE



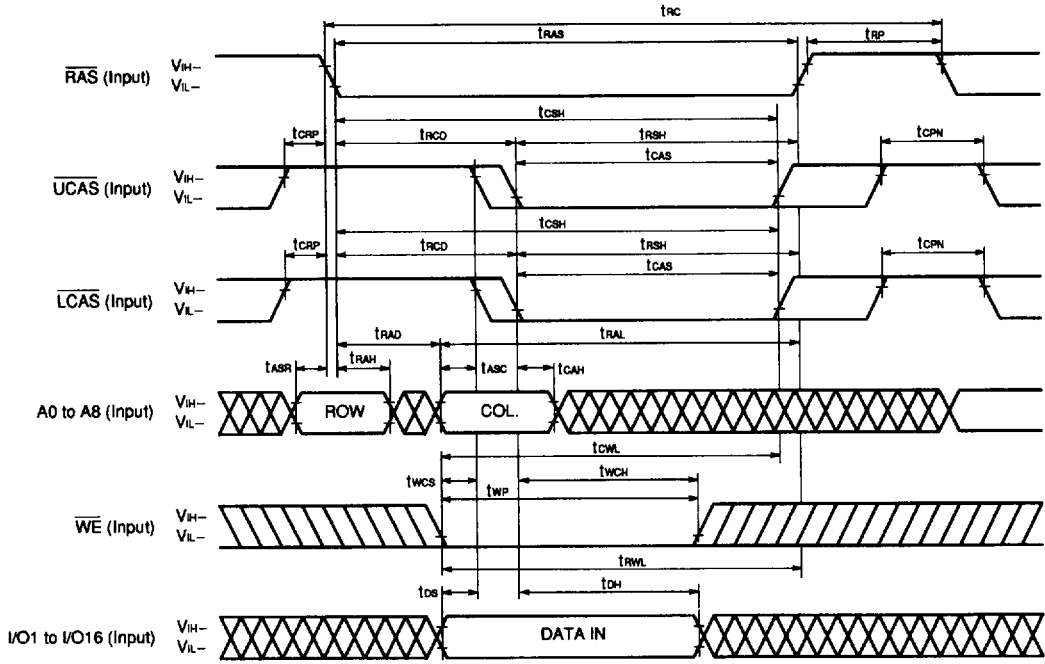
UPPER BYTE READ CYCLE



LOWER BYTE READ CYCLE

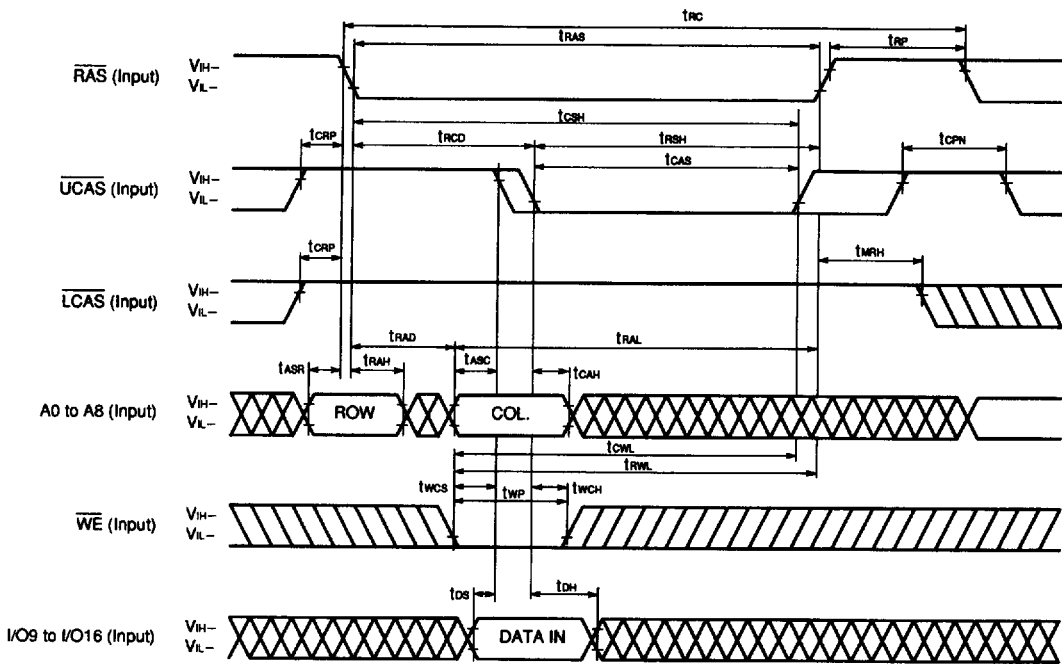


EARLY WRITE CYCLE



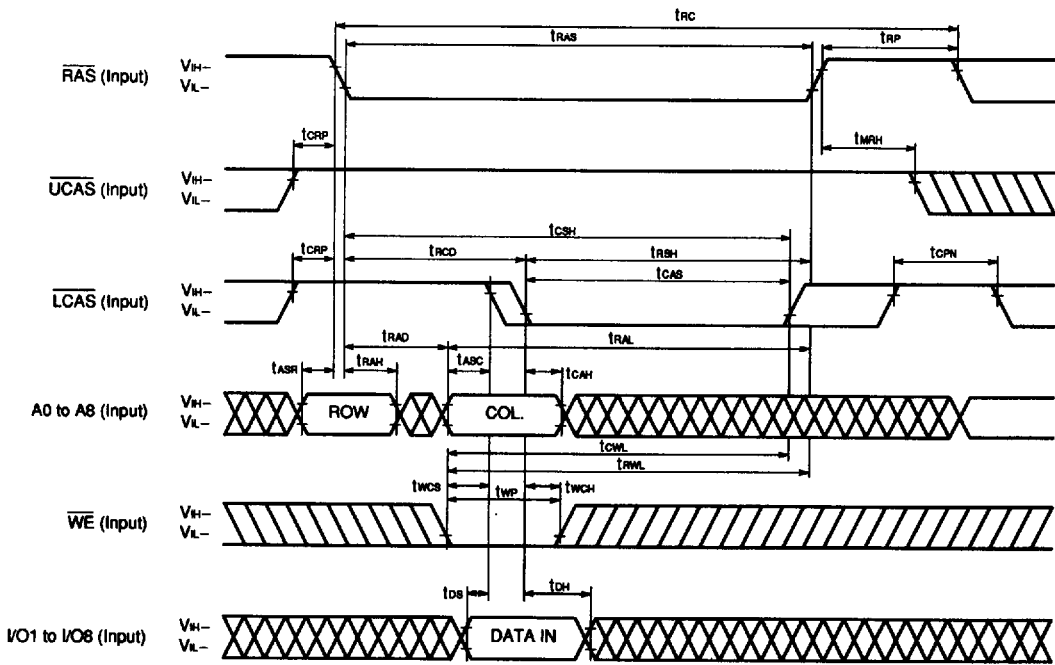
Remark \overline{OE} = Don't care

UPPER BYTE EARLY WRITE CYCLE



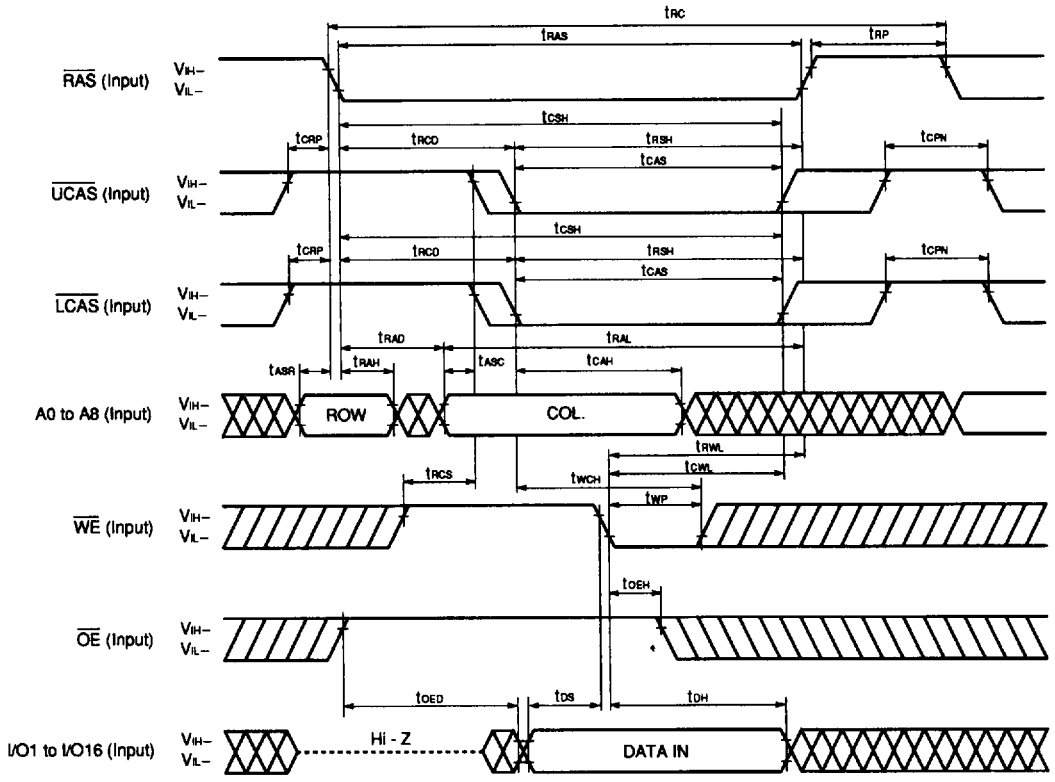
Remark \overline{OE} , I/O1 to I/O8 = Don't care

LOWER BYTE EARLY WRITE CYCLE

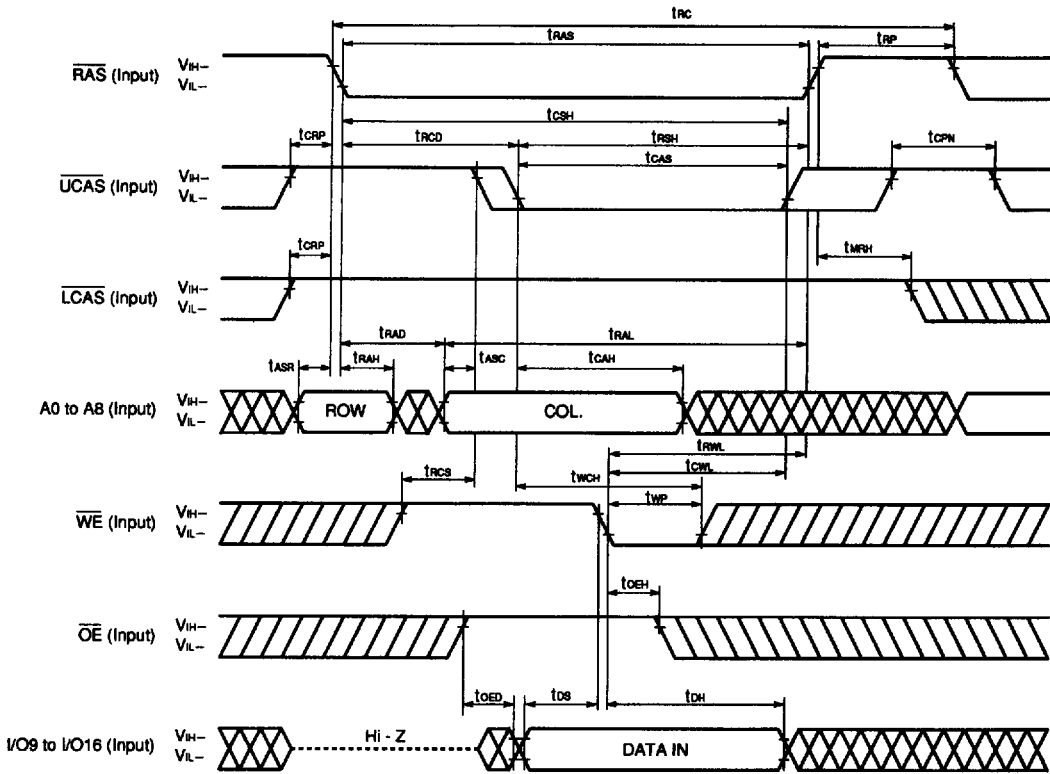


Remark \overline{OE} , I/O9 to I/O16 = Don't care

LATE WRITE CYCLE

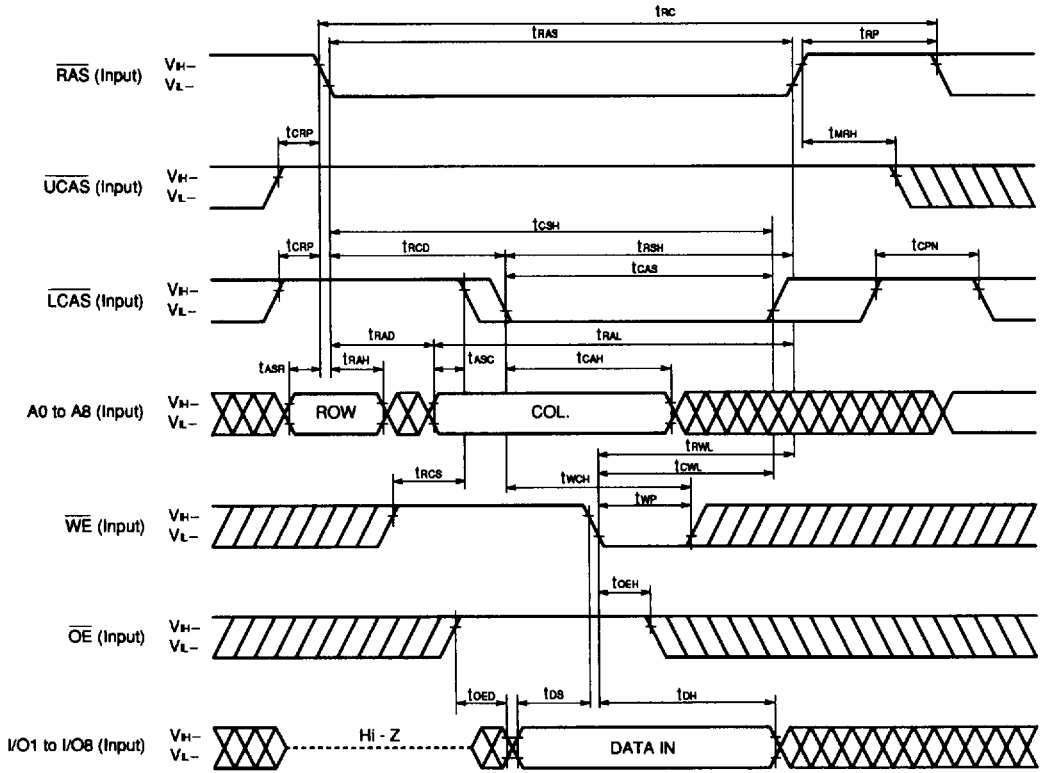


UPPER BYTE LATE WRITE CYCLE



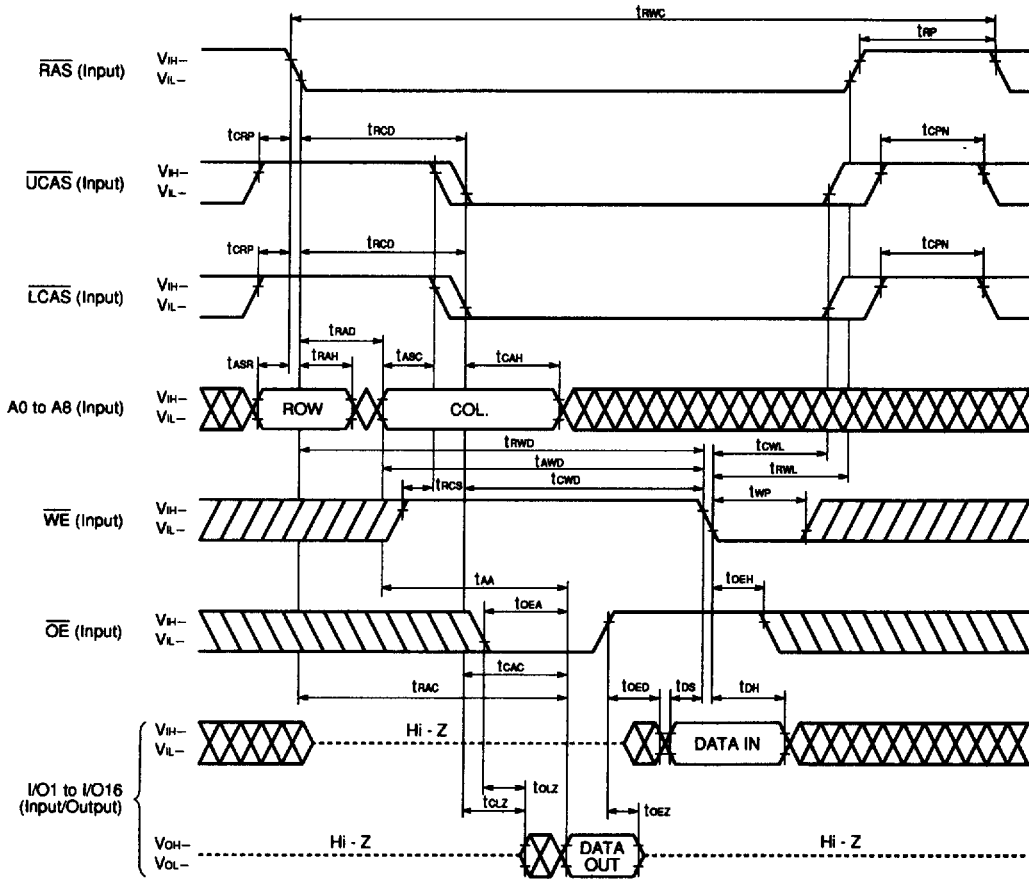
Remark I/O1 to I/O8 = Don't care

LOWER BYTE LATE WRITE CYCLE

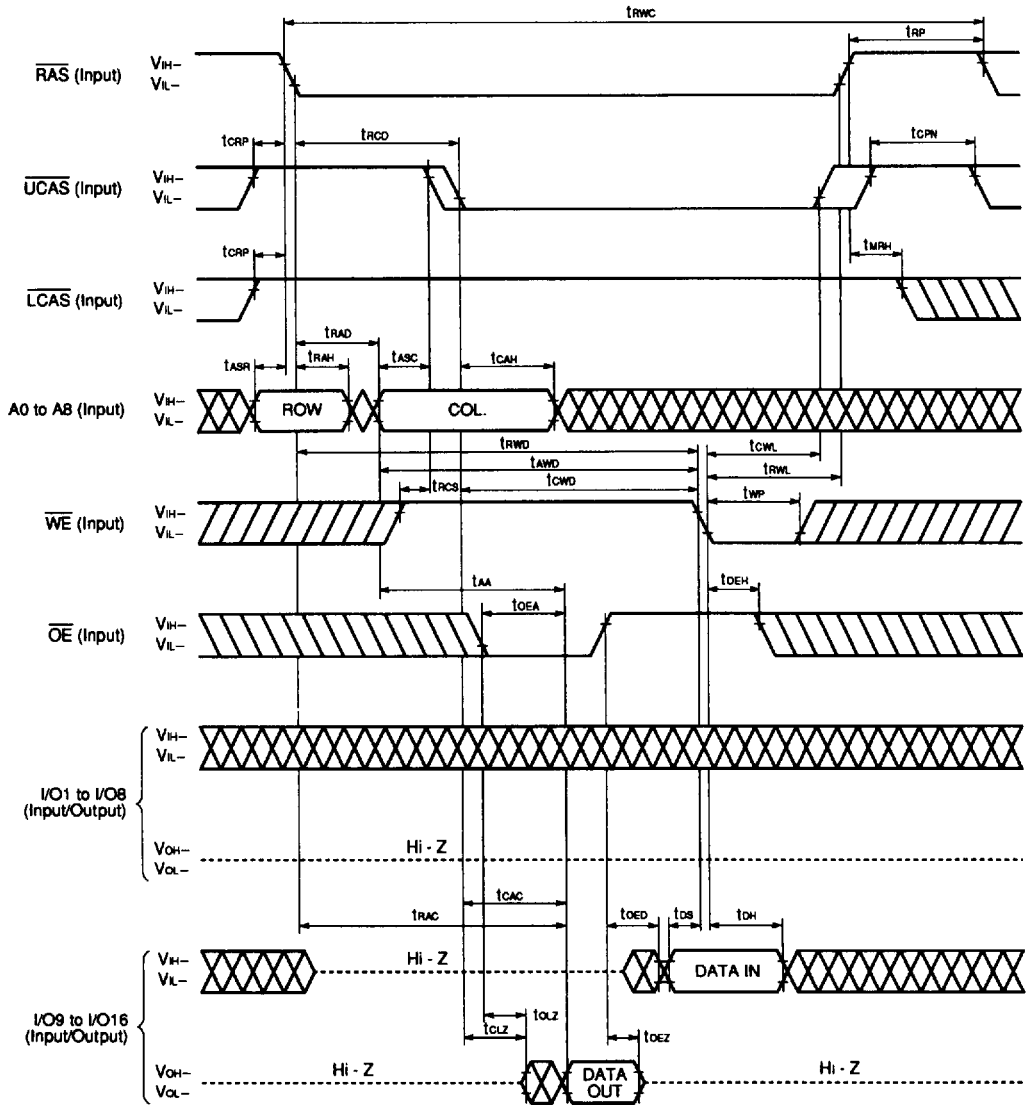


Remark I/O9 to I/O16 = Don't care

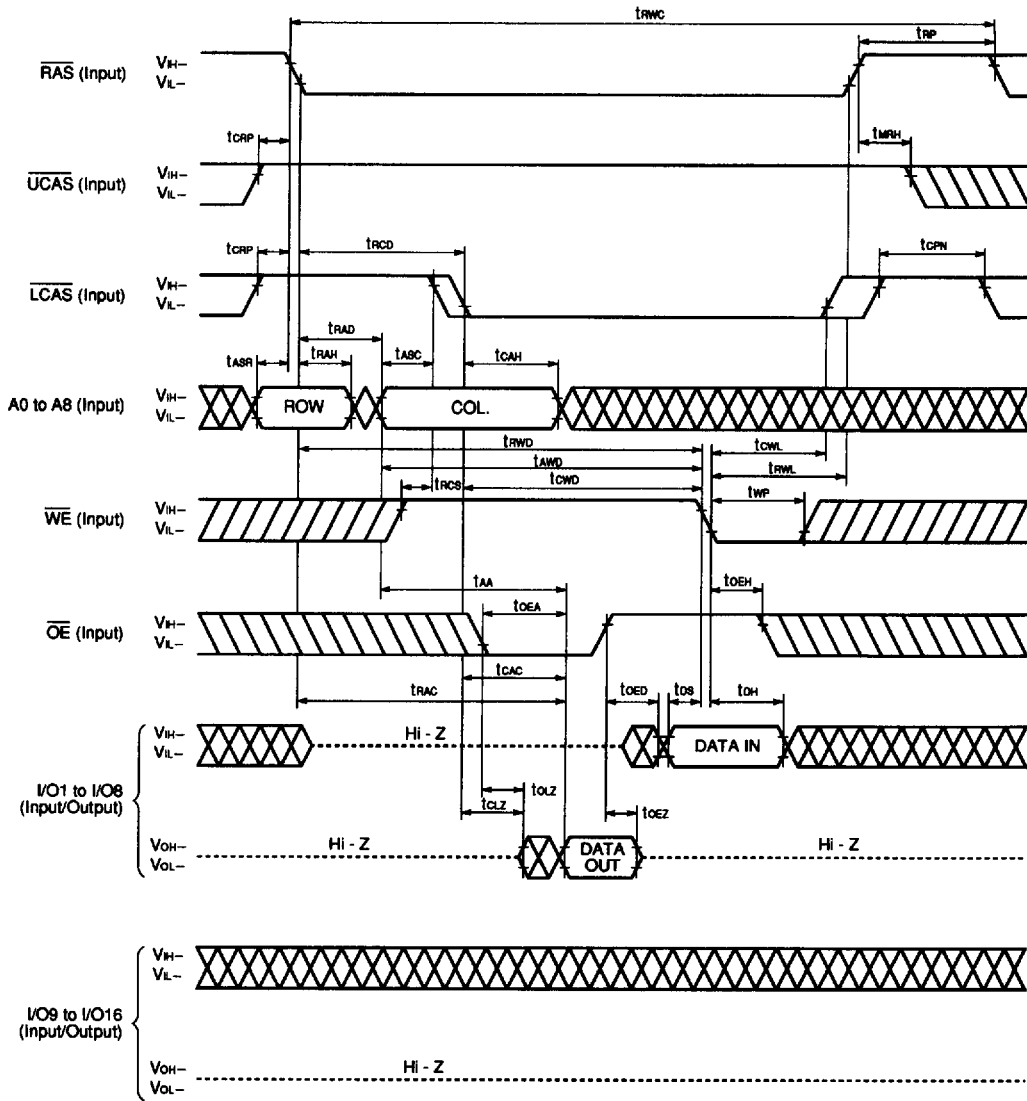
READ MODIFY WRITE CYCLE



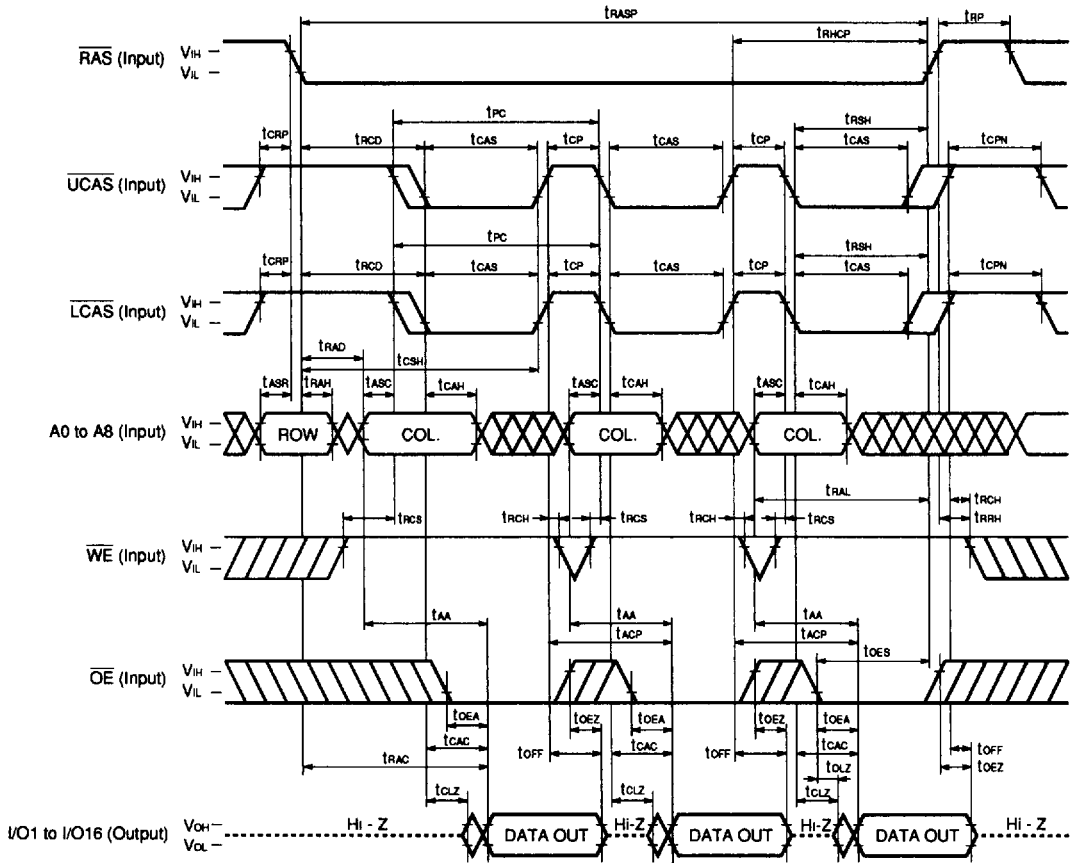
UPPER BYTE READ MODIFY WRITE CYCLE



LOWER BYTE READ MODIFY WRITE CYCLE

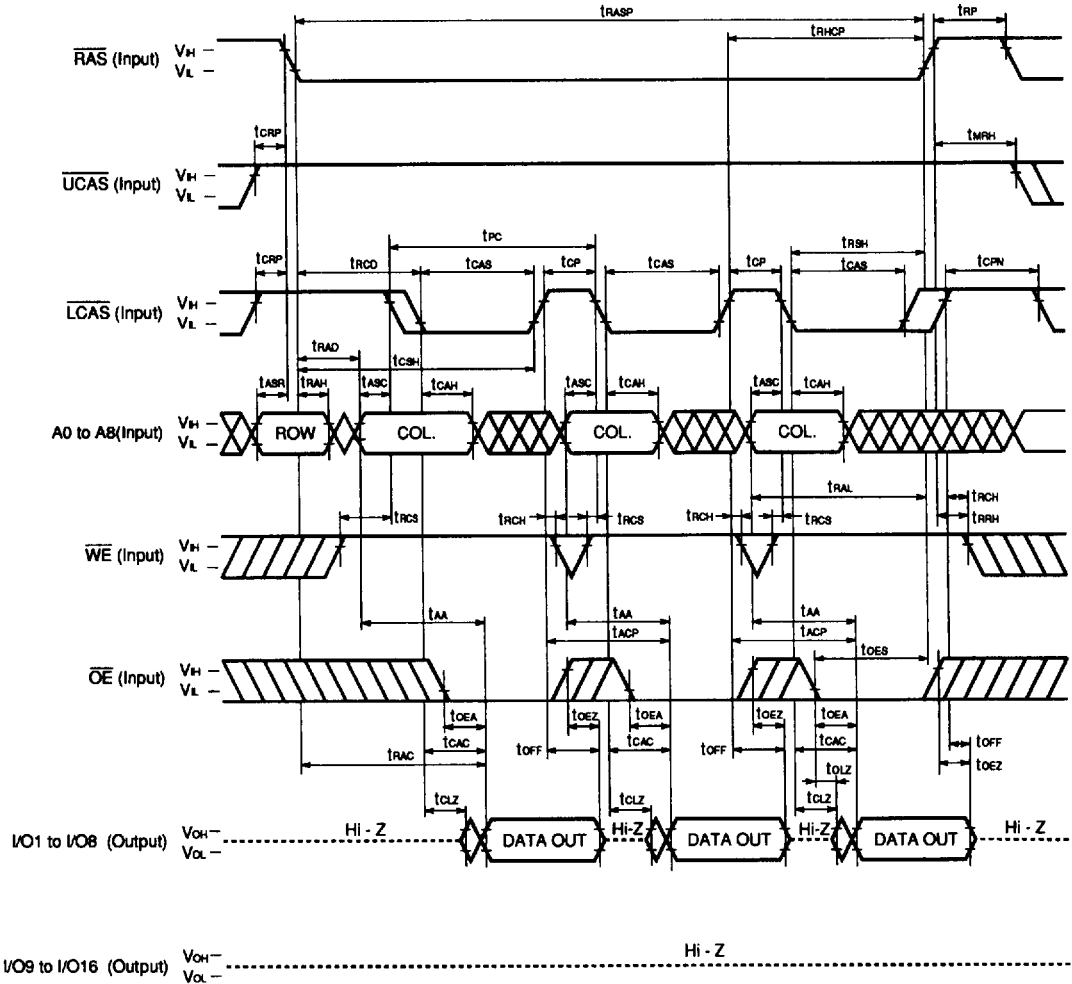


FAST PAGE MODE READ CYCLE



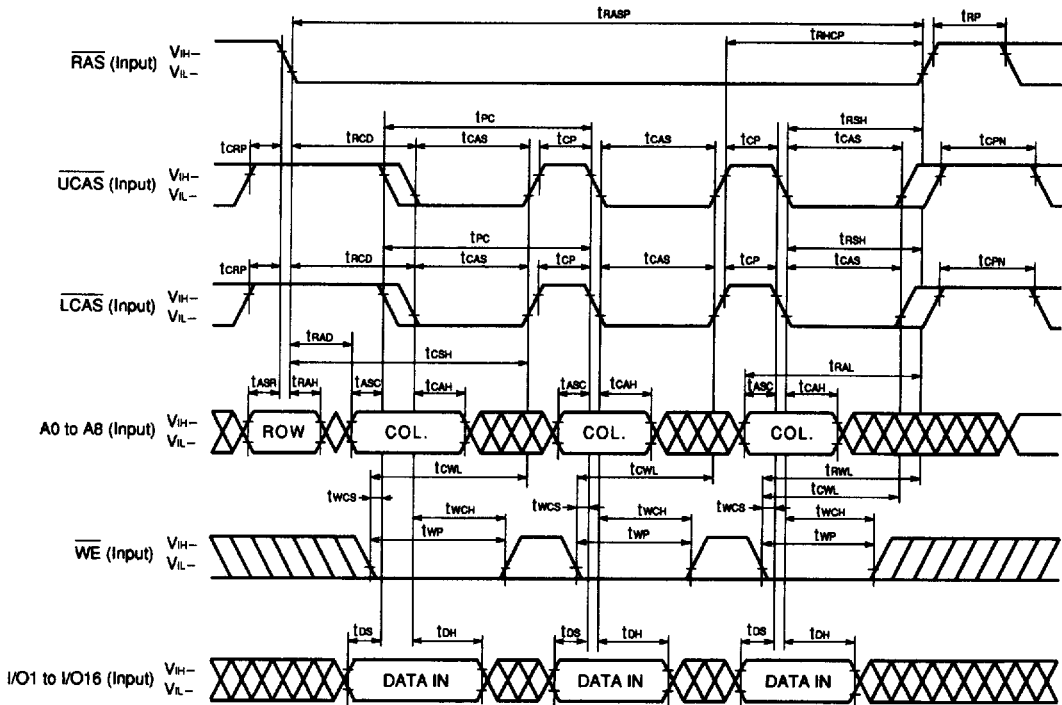
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

FAST PAGE MODE LOWER BYTE READ CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

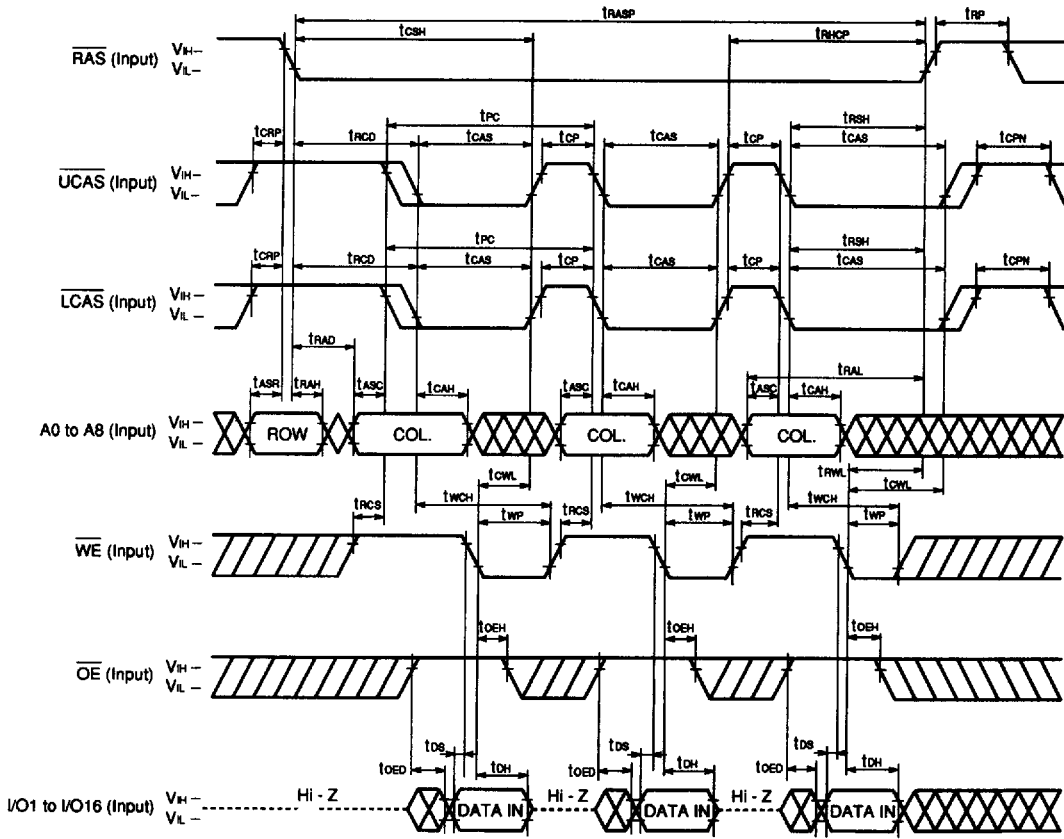
FAST PAGE MODE EARLY WRITE CYCLE



Remark \overline{OE} = Don't care

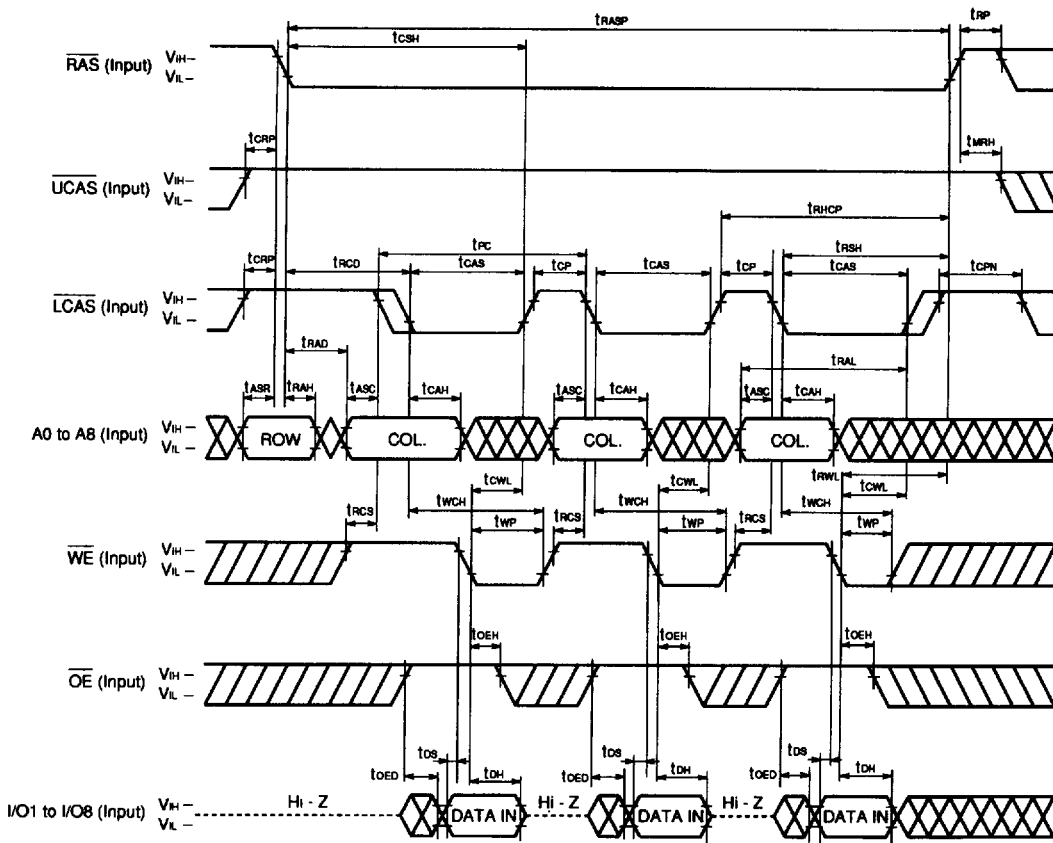
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

FAST PAGE MODE LATE WRITE CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

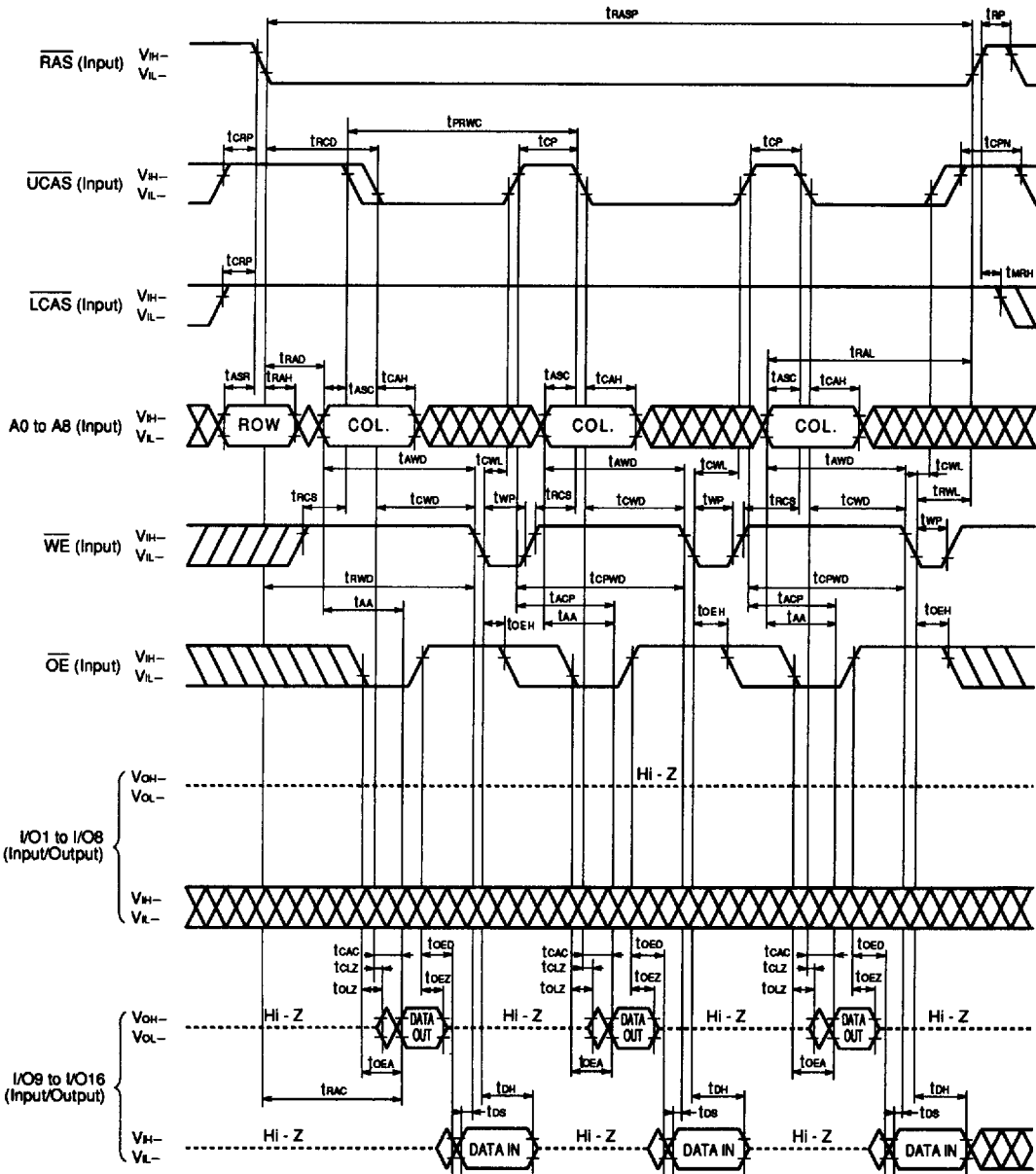
FAST PAGE MODE LOWER BYTE LATE WRITE CYCLE



Remark I/O9 to I/O16 = Don't care

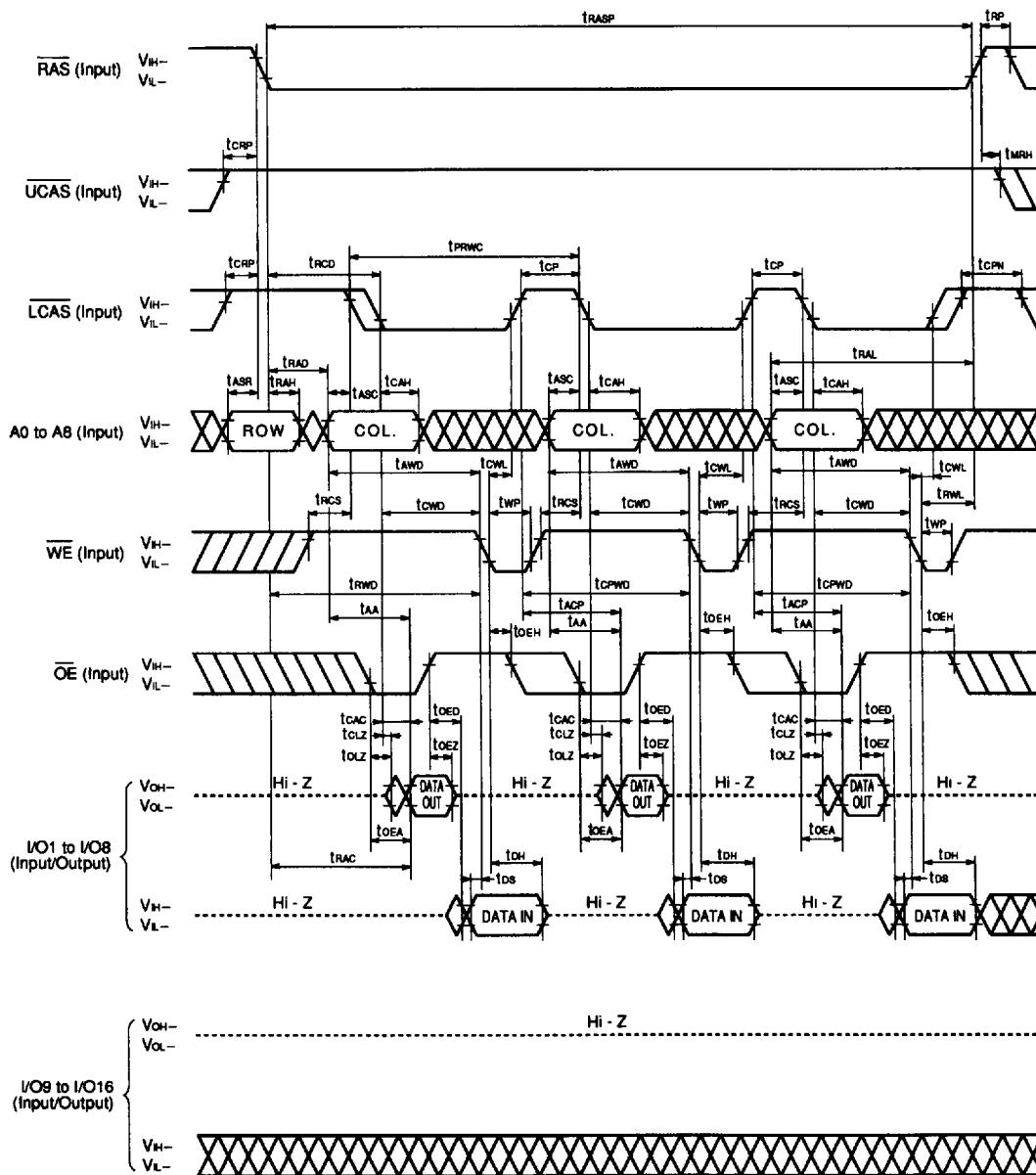
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

FAST PAGE MODE UPPER BYTE READ MODIFY WRITE CYCLE



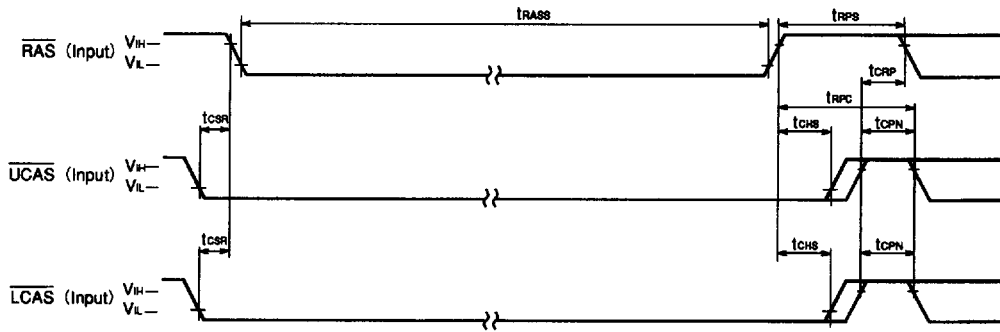
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

FAST PAGE MODE LOWER BYTE READ MODIFY WRITE CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive \overline{CAS} cycles within the same \overline{RAS} cycle.

★ **CAS BEFORE RAS SELF REFRESH CYCLE (Only for μPD42S4260)**



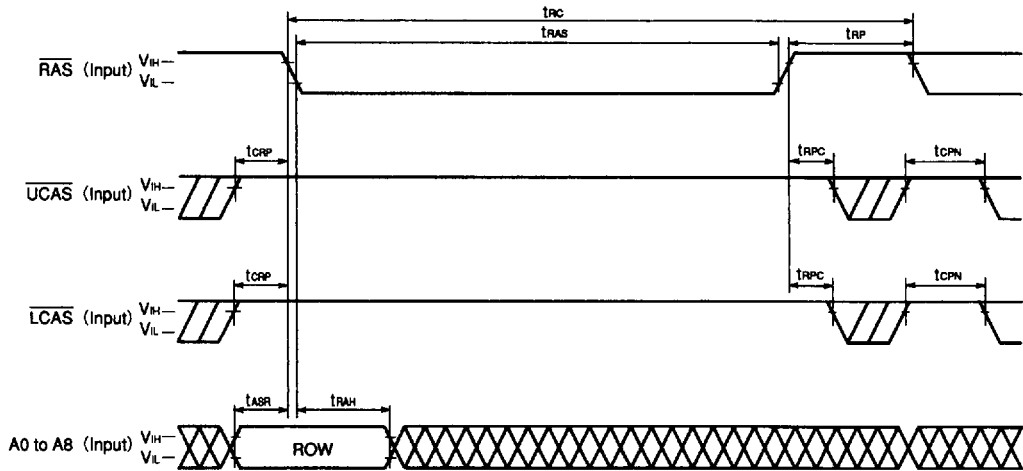
Remark Address, \overline{WE} , \overline{OE} = Don't care I/O1 to I/O16 = Hi - Z

How to use CAS before RAS self refresh mode.

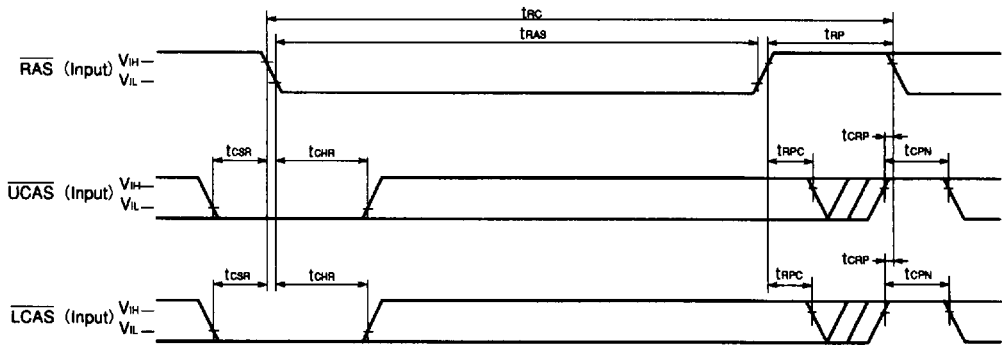
CAS before RAS self refresh mode can't be used by itself. It must be used with performing one of 3 refreshes below.

- **When using distributed CAS before RAS refresh**
Refresh 512 times during 128 ms before set into the CAS before RAS self refresh mode and after reset.
- **When using burst CAS before RAS refresh**
Refresh 512 times during 8 ms before set into the CAS before RAS self refresh mode and after reset.
- **When using RAS only refresh**
Refresh all refresh addresses during 8 ms before set into the CAS before RAS self refresh mode and after reset.

RAS ONLY REFRESH CYCLE

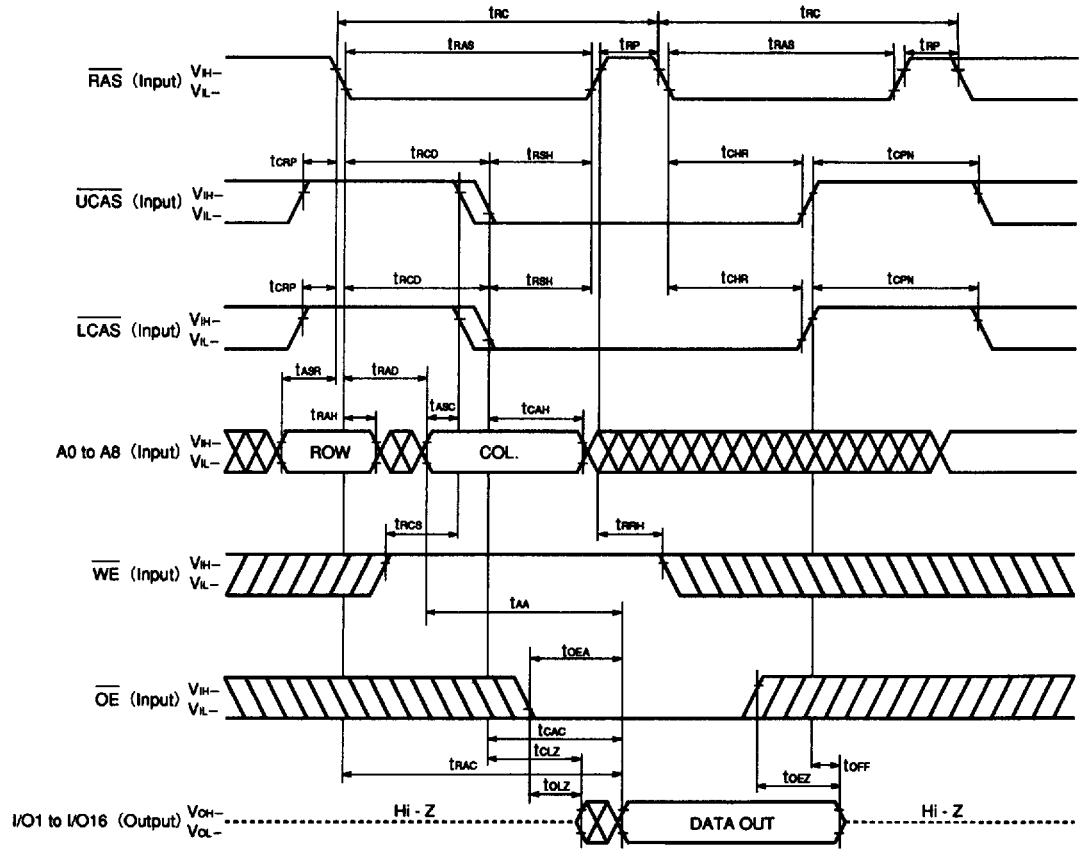


CAS BEFORE RAS REFRESH CYCLE

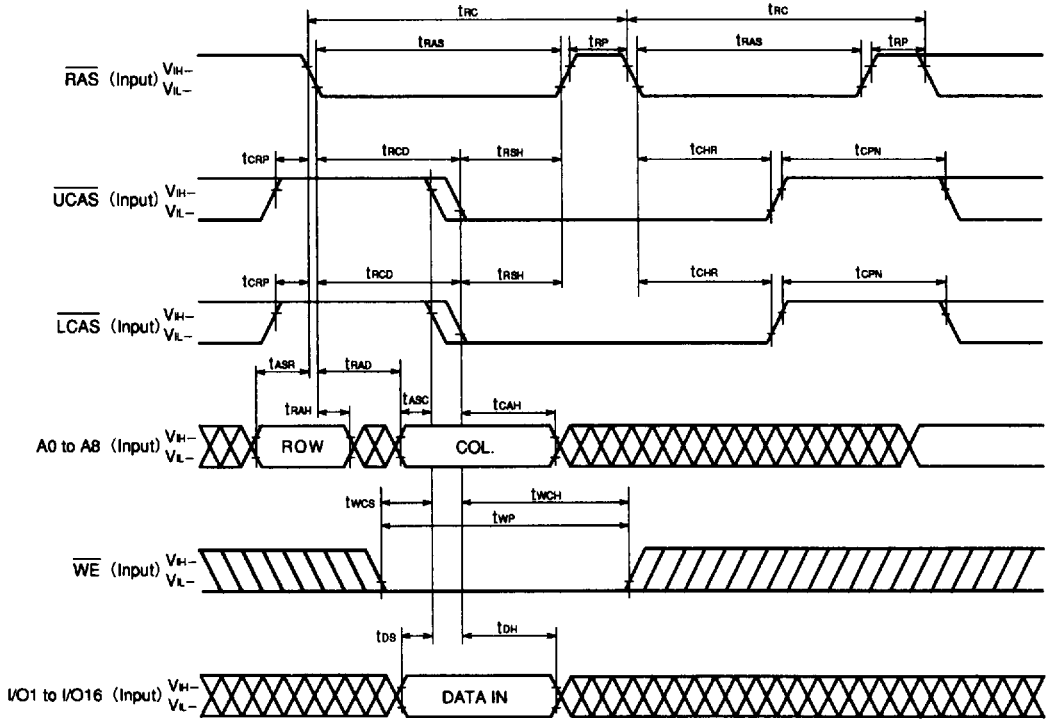


Remark A0 to A8, $\overline{\text{WE}}$, $\overline{\text{OE}}$ = Don't care I/O1 to I/O16 = Hi - Z

HIDDEN REFRESH CYCLE (READ)

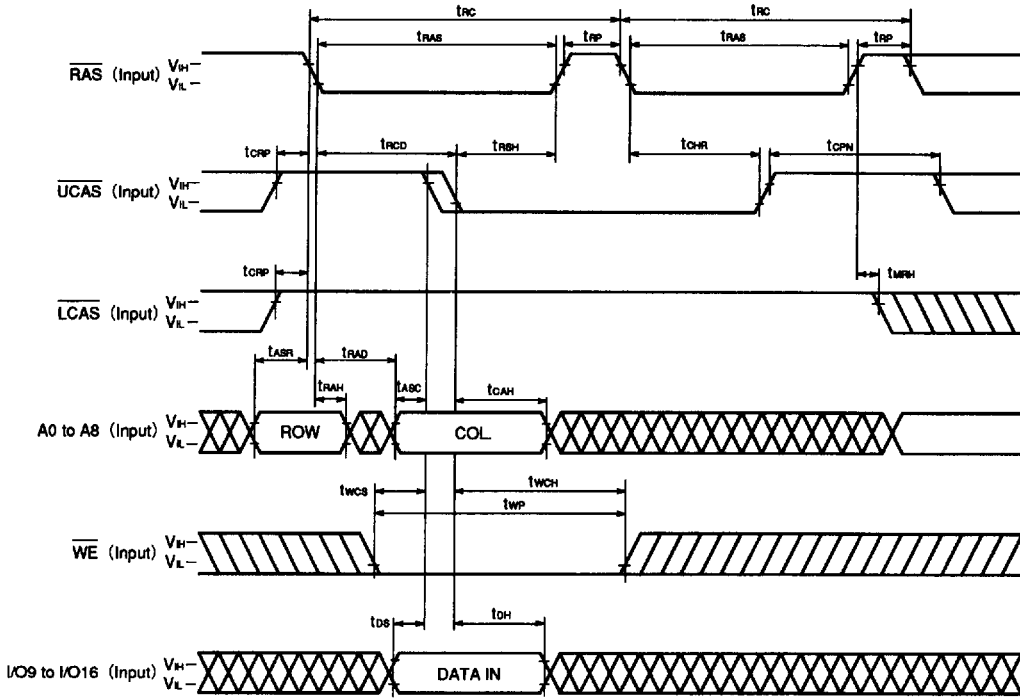


HIDDEN REFRESH CYCLE (WRITE)



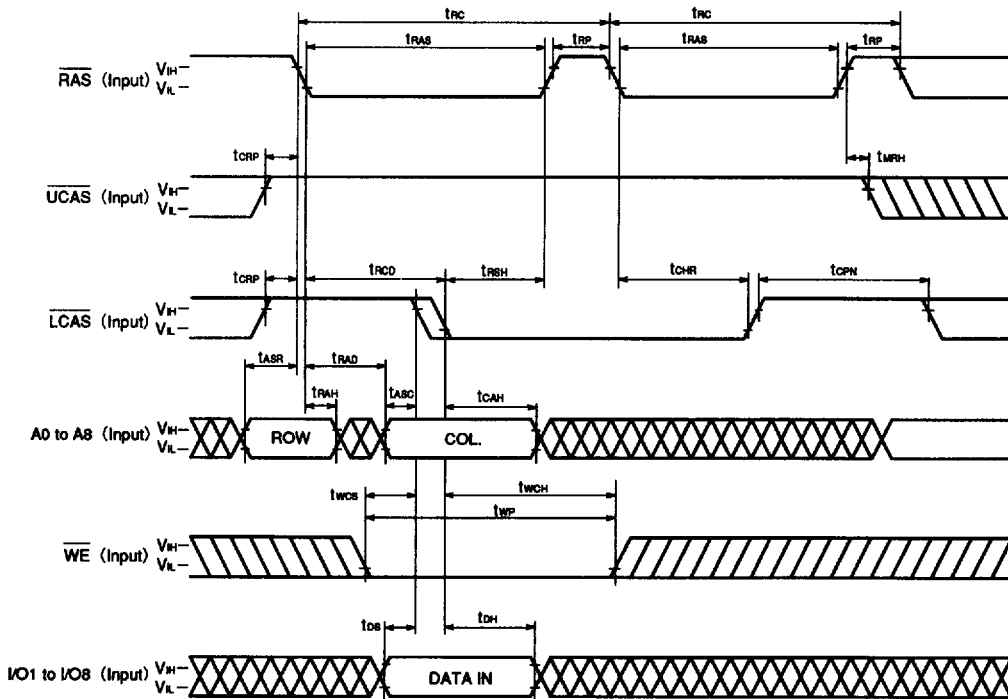
Remark \overline{OE} = Don't care

HIDDEN REFRESH CYCLE (UPPER BYTE WRITE)



Remark \overline{OE} , I/O1 to I/O8 = Don't care

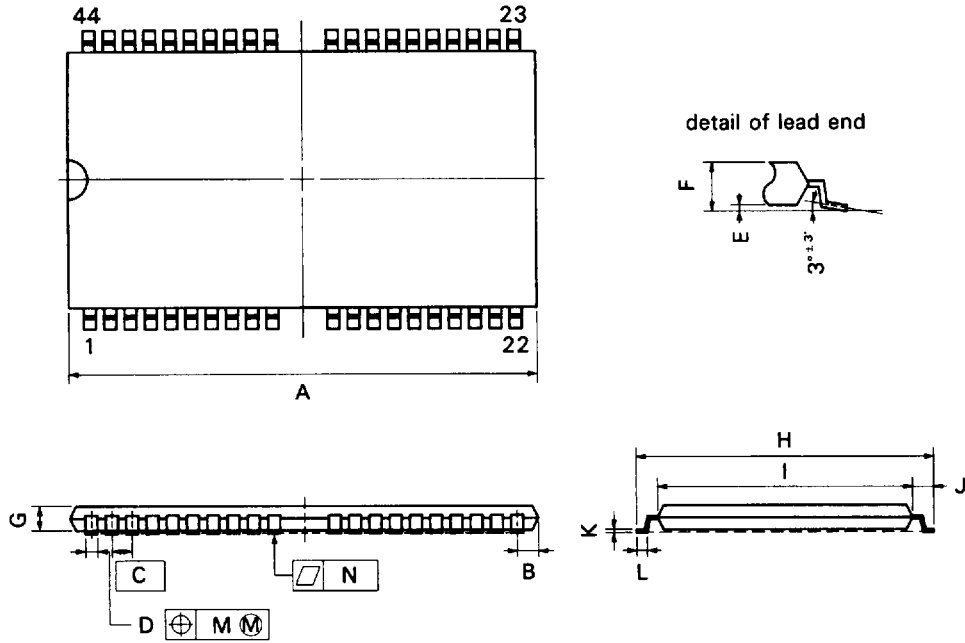
HIDDEN REFRESH CYCLE (LOWER BYTE WRITE)



Remark \overline{OE} , I/O9 to I/O16 = Don't care

PACKAGE INFORMATIONS

44 PIN PLASTIC TSOP (400mil)



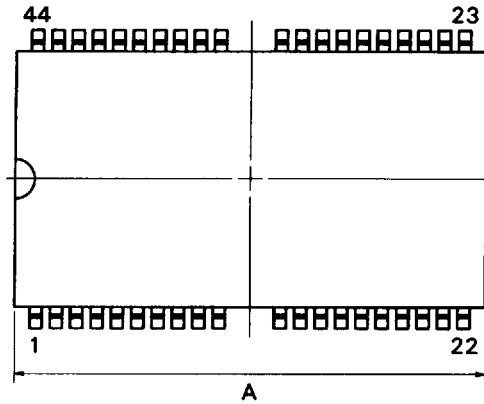
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

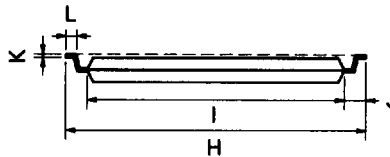
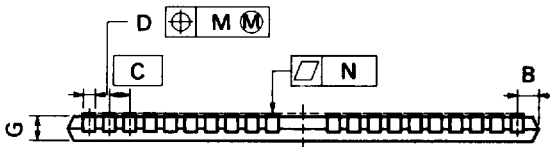
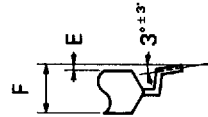
S44G5-80-7JF

ITEM	MILLIMETERS	INCHES
A	18.81 MAX	0.741 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30 ^{+0.10}	0.012 ^{+0.004}
E	0.05 ^{+0.05}	0.002 ^{+0.002}
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76 ^{±0.2}	0.463 ^{±0.008}
I	10.16 ^{±0.1}	0.400 ^{±0.004}
J	0.8 ^{±0.2}	0.031 ^{+0.008}
K	0.125 ^{+0.10}	0.005 ^{+0.004}
L	0.5 ^{±0.1}	0.020 ^{+0.004}
M	0.13	0.005
N	0.10	0.004

44 PIN PLASTIC TSOP (400mil)



detail of lead end



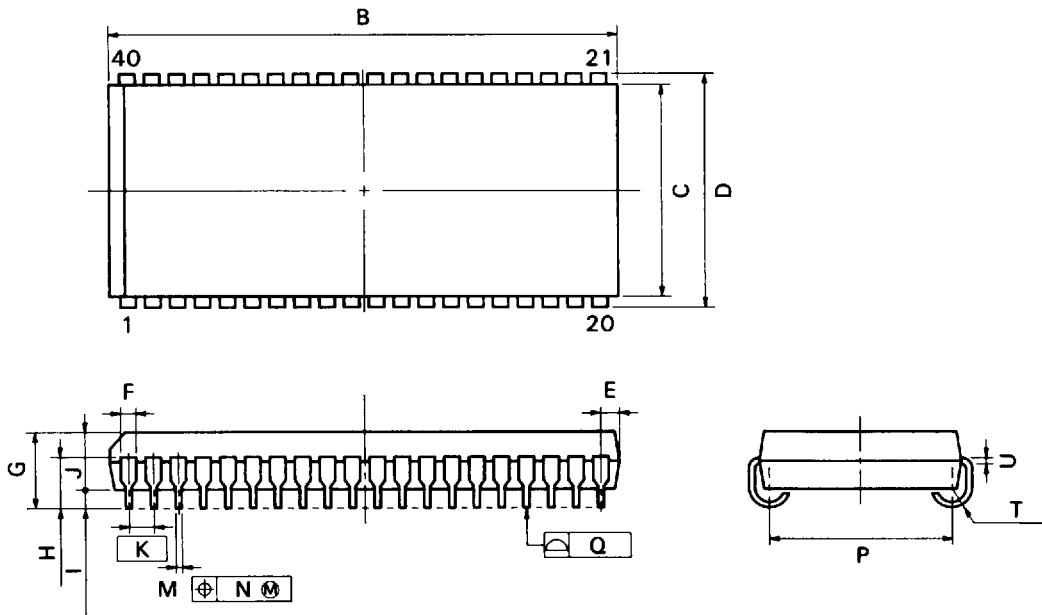
S44G5-80-7KF

NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30 ^{±0.10}	0.012 ^{±0.004}
E	0.05 ^{±0.05}	0.002 ^{±0.002}
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76 ^{±0.2}	0.463 ^{±0.008}
I	10.16 ^{±0.1}	0.400 ^{±0.004}
J	0.8 ^{±0.2}	0.031 ^{±0.008}
K	0.125 ^{±0.010}	0.005 ^{±0.002}
L	0.5 ^{±0.1}	0.020 ^{±0.004}
M	0.13	0.005
N	0.10	0.004

40PIN PLASTIC SOJ (400 mil)



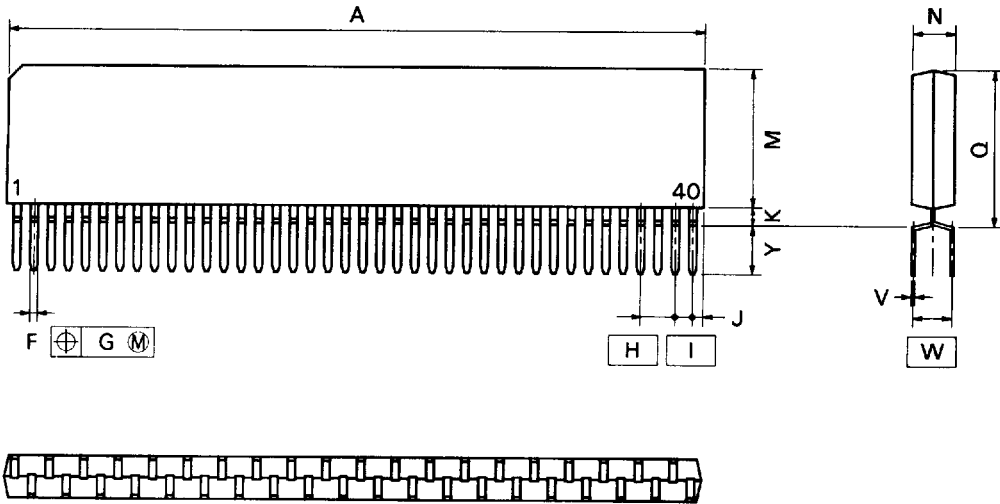
P40LE-400A-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	26.29 ^{+0.2} _{-0.35}	1.035 ^{+0.008} _{-0.014}
C	10.16	0.400
D	11.18 ^{±0.2}	0.440 ^{±0.008}
E	1.08 ^{±0.15}	0.043 ^{+0.005} _{-0.007}
F	0.7	0.028
G	3.5 ^{±0.2}	0.138 ^{±0.008}
H	2.4 ^{±0.2}	0.094 ^{+0.009} _{-0.008}
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40 ^{±0.10}	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.4 ^{±0.20}	0.370 ^{±0.008}
Q	0.15	0.006
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

40 PIN PLASTIC ZIP(475mil)



P40V-100-475A

NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	51.23 MAX.	2.017 MAX.
F	0.50 ^{±0.10}	0.020 ^{+0.004} _{-0.004}
G	0.25	0.010
H	2.54 (T.P.)	0.100 (T.P.)
I	1.27 (T.P.)	0.050 (T.P.)
J	0.85 MAX.	0.034 MAX.
K	0.9 MIN.	0.035 MIN.
M	10.5 MAX.	0.414 MAX.
N	2.8 ^{±0.2}	0.110 ^{+0.008} _{-0.008}
Q	12.07 MAX.	0.476 MAX.
V	0.25 ^{+0.10} _{-0.08}	0.010 ^{+0.004} _{-0.003}
W	2.54 (T.P.)	0.100 (T.P.)
Y	3.25 ^{±0.2}	0.128 ^{±0.008}

RECOMMENDED SOLDERING CONDITIONS



The following conditions (see tables below and next page) must be met when soldering μPD42S4260, 424260.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case other soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

μPD42S4260G5, 424260G5 (44-pin plastic TSOP)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process .	IR35-107-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process .	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S4260LE, 424260LE (40-pin plastic SOJ)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-207-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

TYPE OF THROUGH HOLE MOUNT DEVICE

μPD42S4260V, 424260V (40-pin plastic ZIP)

Soldering process	Soldering conditions
Wave soldering	Solder temperature: 260 °C or below, Flow time : 10 seconds or below
Partial heating method	Terminal temperature: 260 °C or below, Time : 10 seconds or below

Caution Do not jet molten solder on the surface of package.