NEC Electronics Inc.

APPLICATION NOTE 54
μPD42505
LINE BUFFER FOR COMMUNICATIONS SYSTEMS

Introduction

The current trend in storage devices is toward larger, faster, better-performing products. There is a complementary trend toward the development of storage devices designed for specific purposes. The video buffer is an example of a dedicated device. Line buffers, field (frame) buffers for TV and broadcast equipment, and graphics buffers for computers are examples of video storage devices. Table 1 shows some of NEC's dedicated video buffers.

Table 1. Video Buffers

Function	Product	Storage Configuration	Serial Cycle Time	Application in Video/Optical Systems
Line buffers	μPD42505	5048 x 8	50 or 75 ns	Line storage in facsimile machines, copiers, and scanners
	μPD41101/μPD42101	910 x 8	34 or 69 ns	Double-speed scan conversion for NTSC TV, luma/chroma separation
	μPD41102/μPD42102	1135 x 8	28 or 56 ns	Double-speed scan conversion for PAL TV, luma/chroma separation
Field buffer	μPD42270	263 x 910 x 4	60 ns	Image field storage
Dual-port graphics buffers	μPD41264	64K x 4/256 x 4	40 or 60 ns	High-speed drawing device
	μPD42274/μPD42273	256K x 4/512 x 4	30 or 40 ns	
Triple-port graphics buffer	μPD42232	32K x 8/256K x 1/128 x 8	40 or 60 ns	High-speed drawing/image processing device
Bidirectional data buffer	μPD42532	32K x 8	100 ns	Data transfer rate conversion

This application note introduces the μPD42505, a high-speed serial access device with the same general interface specifications as those of the μPD41101. The μPD42505 was developed specifically for office automation equipment that handles a large amount of data in each horizontal line, equipment such as G3 and G4 digital facsimile machines, high-performance copiers, and image scanners.

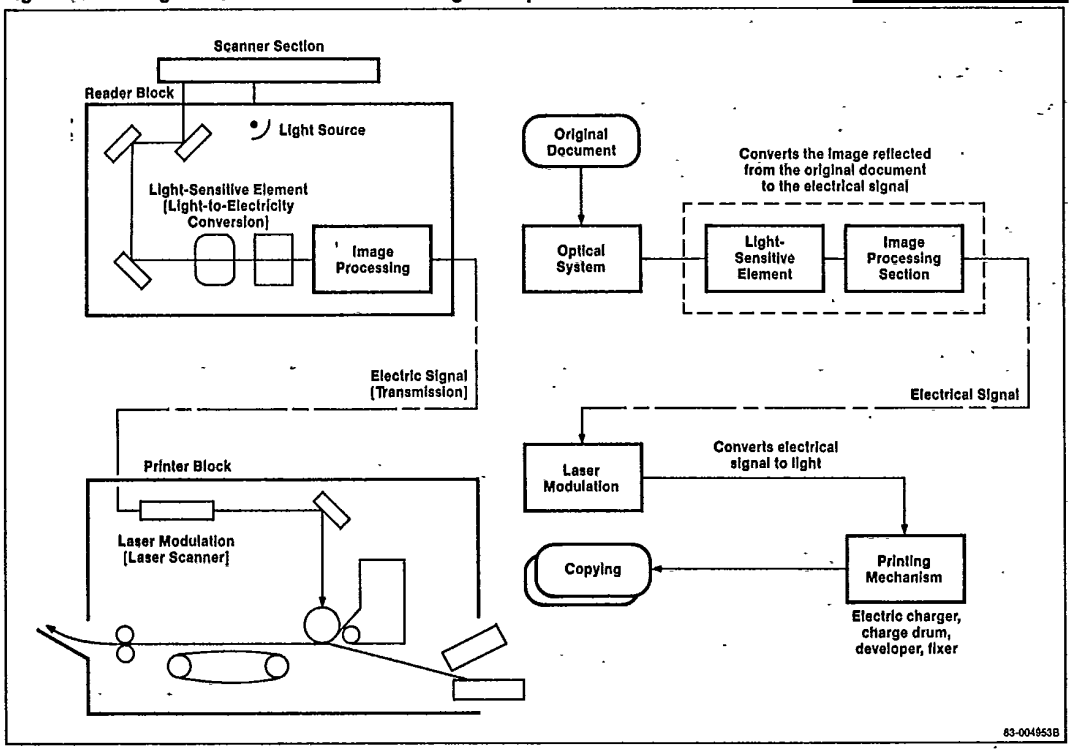
There has been a great deal of technical progress toward higher quality and performance in the development of this image-processing equipment. For example, there are already advances in image quality using two-dimensional filtering, image contraction and expansion, and high-speed video signal transfer. The μPD42505 achieves optimal processing with a storage array of 5048 x 8 bits, and by use of an internal algorithm to read out data in the order in which it was input. The fast cycle time of 50 ns allows the μPD42505 to perform various types of image processing.

Figure 1 shows a typical application for the μPD42505 using a digital copier as an example.

A digital copier mainly consists of a reader and a printer section. The image reflected from the original document placed in the scanner section is input to an image sensor (e.g., a CCD or contact-type image sensor) and photoelectrically converted to a digital signal. The digital signal is then input to the image processing section for image quality improvement and processing. The electronic image signal processed in the reader block is sent to the printer block, converted to light in the laser modulation section, developed, fixed, and printed out. If a communication facility is added to this copier, it can function as a facsimile machine.

Digital copiers and facsimile machines configured in this way can use dedicated video buffers in the image processing or transmission section.

Figure 1. Configuration and Data Flow in a Digital Copier

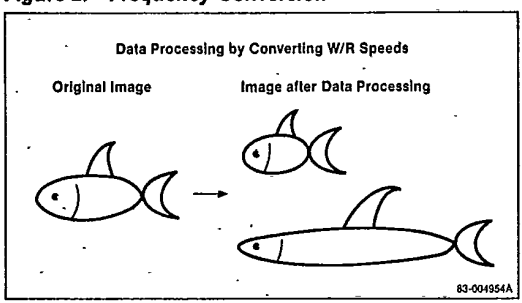


Uses for the μPD42505

The following discussion describes the types of applications for which the μPD42505 was developed: frequency (speed) conversion, a data delay line for one horizontal scanning line, and buffering for data transfer operations in a simple configuration with simple control.

Consider the need for a device that asynchronously converts the read and write speed for frequency conversion, e.g., a serial access device used for image contraction or expansion, with a word length of one to two horizontal lines. The buffer must be written to and read from asynchronously and at different rates. High speed is also a requirement. Figure 2 illustrates a frequency conversion application.

Figure 2. Frequency Conversion



Another application might require a data delay line with a delay length of one to two lines. This type of buffer could be used for image quality improvement in two-dimensional filtering, especially for filtering in the vertical direction, because it could be written to and read from simultaneously in synchronization with a single clock signal. Figure 3 illustrates two-dimensional filtering.

A third application is a buffer for data transfer operations. This application requires a device large enough to store the amount of data handled, with the capability to read and write asynchronously, simultaneously, and at different speeds. An output such as a flag to indicate the amount of data in the storage array might also be required. Figure 4 illustrates buffering for data transfer.

Figure 3. Two-Dimensional Filtering

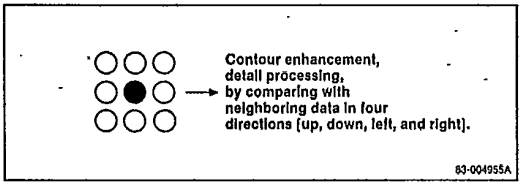
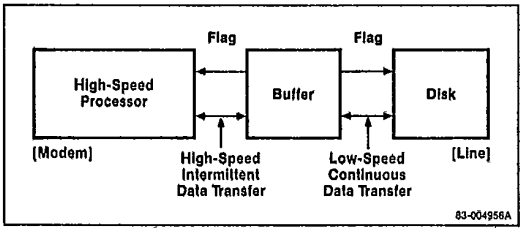


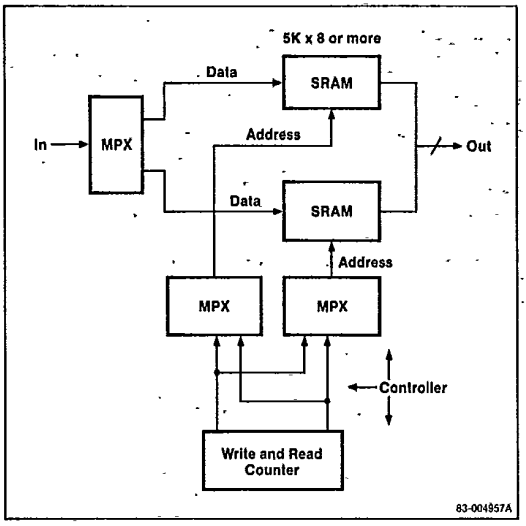
Figure 4. Data Transfer Buffering



These applications typically require a double-buffer configuration using high-speed SRAMs for data storage in bits, as shown in figure 5.

In the first phase, data is written to the first SRAM while data in the second SRAM is read simultaneously, alternating operations between the two SRAMs. However, this operation requires components such as read and write address counters, a multiplexer to switch address signals according to the read and write state of each device, a multiplexer to switch write data input and read data output, and a sophisticated controller to control the SRAMs and the other components. The μPD42505, by performing some of these functions itself, considerably simplifies these applications.

Figure 5. Typical System Using High-Speed SRAMs



Features of the μPD42505

The μPD42505 is a 5048-word x 8-bit high-speed serial access device that uses 1.5-μm CMOS processing and dual-port storage cell circuits allowing simultaneous, asynchronous read and write cycles at different speeds. An internal algorithm makes an external address signal unnecessary.

Read and write operations are fully and independently controlled by their own set of control signals. The storage array length of 5048 words meets the size required to sample one line of JIS A3-size paper on the shorter side (297 mm) with a sampling rate of 16 dots/mm (400 dots/in). On the longer side (418 mm), the sampling rate is 12 dots/mm (300 dots/in). The μPD42505 can easily process document data for each line. The configuration of 8 bits to 1 word corresponds to the number of bits for one sampling point, which allows the device to process natural-looking images.

The μPD42505 can be used in video applications that require high-speed processing because of its minimum simultaneous write/read cycle time of 50 ns and maximum access time of 40 ns. For example, the cycle time of 50 ns is fast enough to digitally process an NTSC or PAL composite video signal at a sampling rate of four times the color subcarrier frequency ($4f_{SC}$).

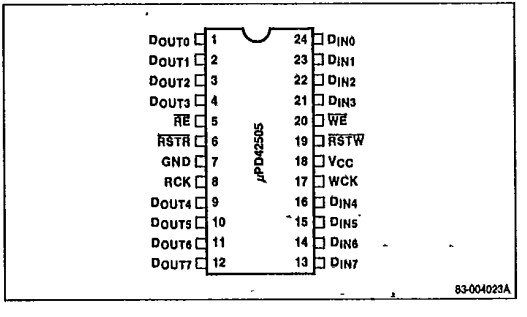
The μPD42505 is particularly suitable for use as a digital delay line with a delay length of up to 5048 cycles in one-cycle steps. The device is mounted in a 300-mil, 24-pin plastic slim DIP. The 300-mil width allows high-density mounting.

μPD42505 Pinout

Pins 1 through 12 control read operation (D_{OUT0}-D_{OUT7}, $\overline{RSTR}$, $\overline{RE}$, and RCK) and the GND pin. Pins 13 through 24 control write operation (D_{IN0}-D_{IN7}, $\overline{RSTW}$, $\overline{WE}$, and WCK) and the power supply (V_{CC}).

$\overline{RSTW}$ and $\overline{RSTR}$ are control signal inputs that reset the internal read and write address pointers to starting address 0. These pins are useful for initializing the chip after power-on or for returning the address to 0.

Figure 6. μPD42505 Pin Configuration



$\overline{WE}$ and $\overline{RE}$ are control signals that enable (low) or disable (high) write and read operation. When $\overline{WE}$ is high, write operation is disabled and the write address stops at the current value. When $\overline{RE}$ is high, read operation is disabled, the read address stops at the current value, and the output goes to high impedance. $\overline{WE}$ and $\overline{RE}$ may be input at any time, but they are latched in each cycle at the rising edge of WCK or RCK, respectively.

WCK and RCK are the write and read system clock inputs. One write or read cycle is executed in synchronization with each WCK or RCK input when $\overline{WE}$ or $\overline{RE}$ is low. The write or read address is incremented internally in single steps and wraps around automatically from 5047 to 0.

D_{IN0}-D_{IN7} are the write data input pins. Write data is clocked into the chip at the rising edge at the end of the WCK cycle. D_{OUT0}-D_{OUT7} are the read data output pins. Read data is output when the access time has elapsed from the rising edge at the beginning of the RCK cycle.

Read and Write Timing

Input a low-level signal to $\overline{RSTW}$ (for writing) or $\overline{RSTR}$ (for reading) to satisfy the setup and hold times measured from the rising edge at the beginning of the WCK or RCK cycle. This returns the cycle to starting address 0. Figure 7 shows read and write timing for the μPD42505.

As the figure shows, the $\overline{RSTW}$ or $\overline{RSTR}$ signal can end in one write or read cycle or can be repeated for successive write or read cycles. Repeating the reset cycle holds the address at 0. The address is incremented to address 1 only in a cycle when $\overline{RSTW}$ or $\overline{RSTR}$ is set high at the rising edge of the WCK (RCK) cycle. For write reset, the write data clocked in the last reset cycle is written to address 0. For read reset, the data in address 0 is output continuously. After the reset, write or read operation continues as the address is incremented by 1 for each cycle in synchronization with its appropriate clock. When the internal address reaches 5,047 (i.e., when write or read cycles are executed 5,048 times), the address returns to address 0 and the write or read operation starts over at that point.

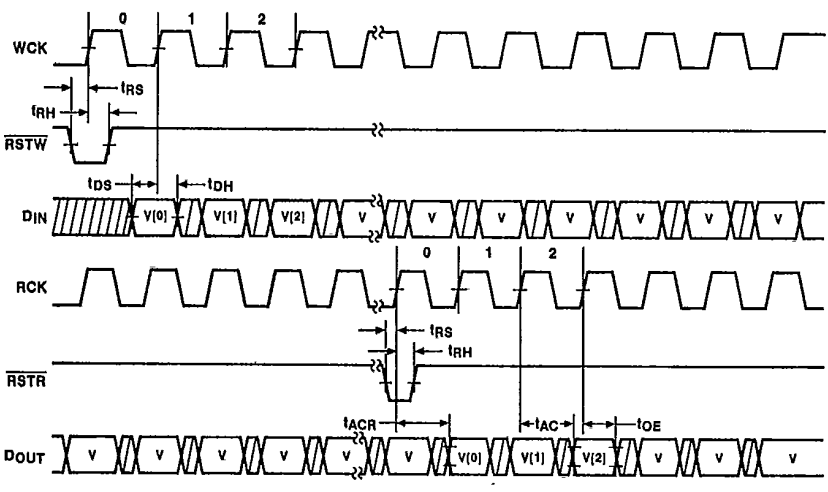
Speed Conversion. Independently controlling the read and write operations of the μPD42505 allows you to perform speed conversion. For example, when the read and write addresses are initialized by $\overline{RSTW}$ and $\overline{RSTR}$, data is written in synchronization with WCK and the write data is written to the chip from device address 0. Data written can be read out from address 0. In this case, the reset signal input timing and the clock signal speed (cycle time) can be independently controlled for read and write operation. The μPD42505 can be used for speed (frequency or time axis) conversion by outputting the data previously input with an arbitrary drive frequency and time at a different drive frequency and time.

Digital Delay Line. To use the μPD42505 as a digital delay line, input the same clock to WCK and RCK and reset the read and write cycles in parallel. Written data is read out after 5,048 cycles to provide a 5,048-cycle digital delay line.

There are three ways to control the delay length:

- By controlling the $\overline{WE}$ and $\overline{RE}$ signals
- By inputting $\overline{RSTW}$ and $\overline{RSTR}$ at different times (the delay length is determined by the offset between the signals)
- By changing the reset signal interval when $\overline{RSTW}$ and $\overline{RSTR}$ are concurrently controlled (the delay length is determined by the reset signal input interval)

Figure 7. Read and Write Timing



Notes:
[1] $\overline{WE} = \overline{RE} = V_{IL}$.
[2] V = Valid data.

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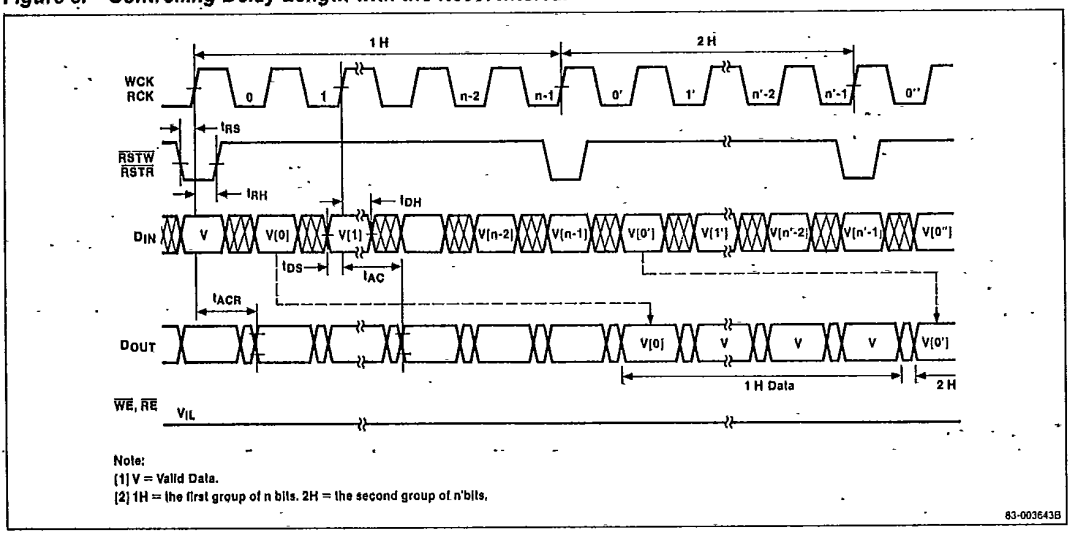
The delay length can be changed in one-cycle steps by controlling $\overline{WE}$ and $\overline{RE}$. When $\overline{WE}$ and $\overline{RE}$ are high, write and read operation is disabled. The write and read addresses remain where they were when the operations were disabled, regardless of WCK and RCK.

When $\overline{RSTW}$ and $\overline{RSTR}$ are used to control the delay length, the data written at address 0 when $\overline{RSTW}$ is input is read out from address 0 when $\overline{RSTR}$ is next input. The offset between $\overline{RSTW}$ and $\overline{RSTR}$ determines the delay length.

In the third method, changing the reset signal input interval, the same signal is used for WCK and RCK so that $\overline{RSTW}$ and $\overline{RSTR}$ are controlled together. The data, written after a reset signal, is read out after the next reset signal in the order it was written. This interval determines the delay length. For example, if the reset signal is input every 4,800 cycles, the delay length is 4,800 cycles. Figure 8 shows the timing for this method.

Figure 8. Controlling Delay Length with the Reset Interval



Note:
[1] V = Valid Data.
[2] 1H = the first group of n bits. 2H = the second group of n'bits.

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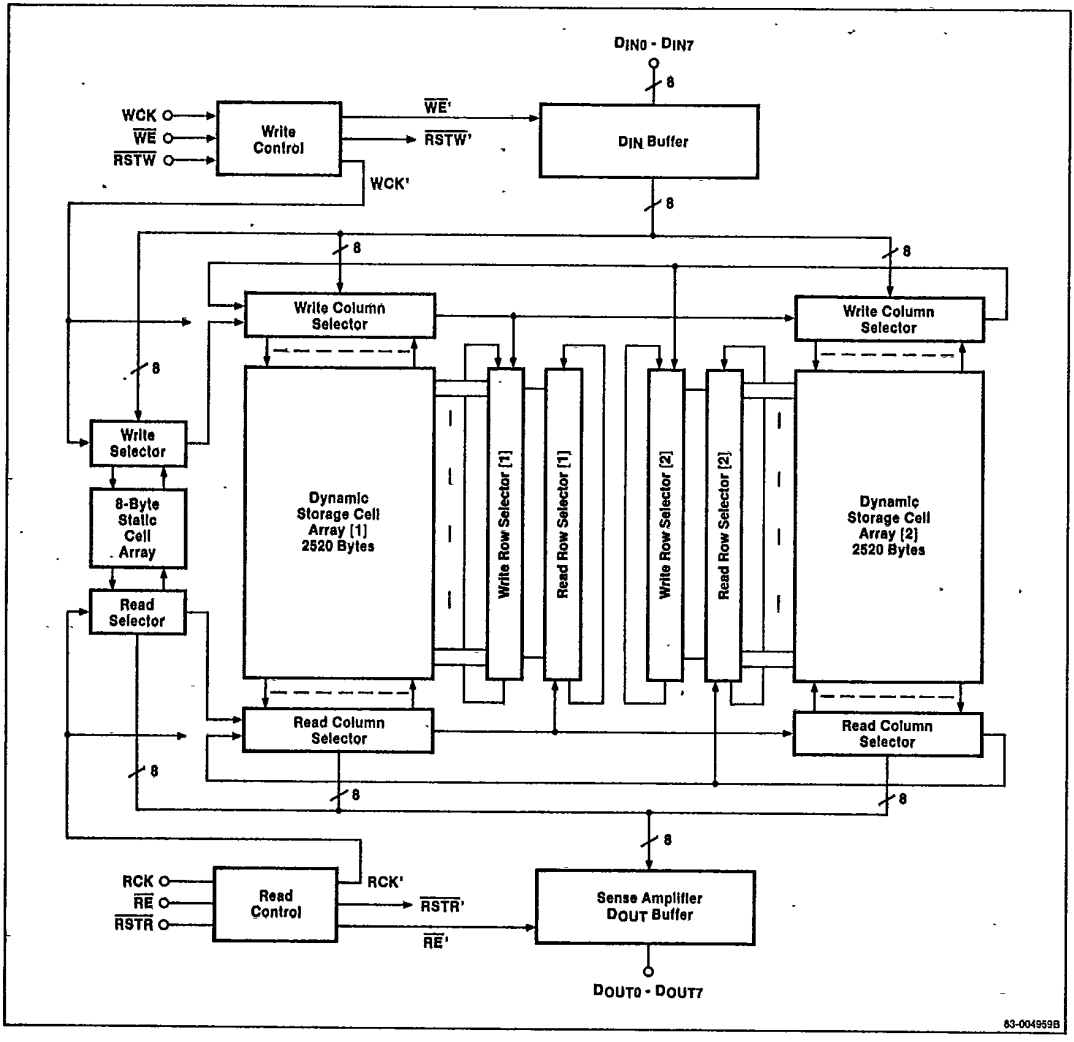
Functional Blocks

The write data input from pins D_{IN0}-D_{IN7} goes through the D_{IN} buffer and is serially written to either a static cell in an 8-byte configuration, or a dynamic cell in a 5,040-byte configuration, one byte (8 bits) at a time, in synchronization with WCK. The data read out from these cells is serially output from the D_{OUT} pins through the sense amplifier and the D_{OUT} buffer, one byte at a time, in synchronization with RCK. The read and write control circuits control these operations.

Figure 9. μPD42505 Block Diagram



Storage Cells

The μPD42505 uses dual-port storage cells to allow read and write cycles to be executed asynchronously and at different speeds. Figure 10 shows a circuit diagram of a static dual-port storage cell, and figure 11 shows a dynamic dual-port storage cell.

In the static cell, read and write data are input as a differential signal so that it can operate at a higher speed. The circuit size is larger because it requires more components.

Figure 10. Static Dual-Port Storage Cell

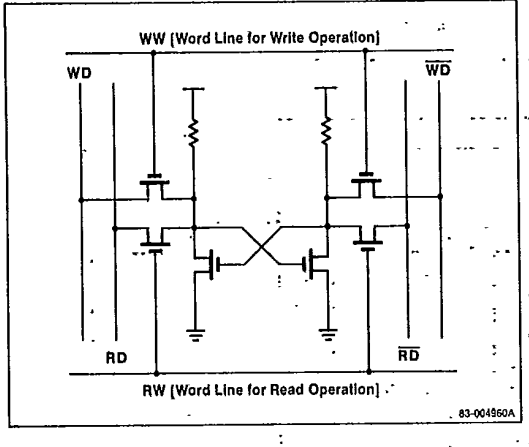
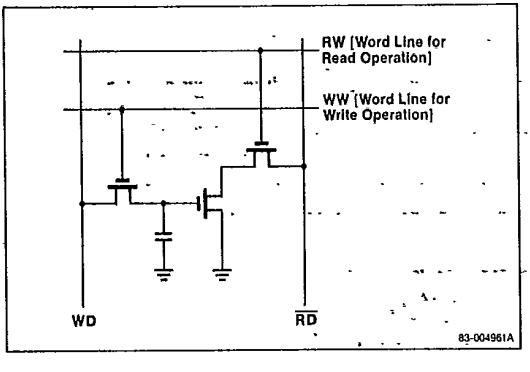


Figure 11. Dynamic Dual-Port Storage Cell



The dynamic cell has only one bit line for read operation and one for write operation. It requires a longer data sense phase, reducing the speed. However, it can be configured with fewer components.

Both types of cells are used in the μPD42505 to exploit the advantages of each. Other than initializing the internal address pointer to the starting address with the reset signal, the μPD42505 is configured so that the internal address is incremented one bit at a time and data is serially accessed. After a reset operation (immediately changing the addressing sequence), a static dual-port storage cell that can operate at higher speed is accessed. Simultaneously or subsequently, a dynamic cell is used as a pipeline, allowing both types of cells to be accessed at high speed.

Pipeline operation refers to an instance where the word line (row) to be selected next is set to the selected level in advance, so that it can be written or read at high speed in the time required to select a column in dynamic static-column mode.

Shift registers are used as read and write column and row selectors to enable the sequential selection of write or read addresses in pipeline processing.

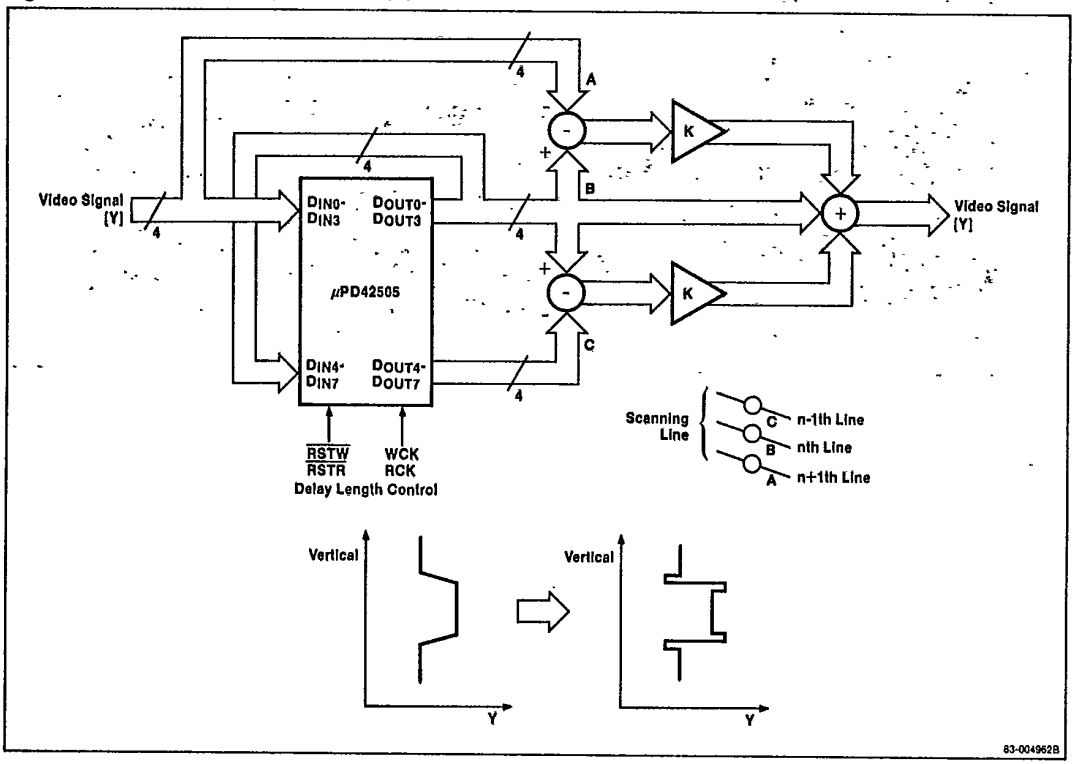
Applications

Signal processing technology aims toward higher quality in the development of digital copiers and facsimile machines. As examples, consider image quality improvement processing such as the adaptive bilevel control technique, which produces a stable and accurate binarization regardless of the original document type, and the two-dimensional equalizing filter, which corrects fading in photoelectric signal conversion. The μPD42505 fits easily into these processes. It can also reduce system size and cost.

Two-Dimensional Filter

In handling an image with half-tones, e.g., a photograph, there is some deterioration in the image quality, such as thin lines and small characters fading out; fading is usually caused by the lens or photoelectric signal conversion system in a CCD sensor. A two-dimensional filter is very effective in enhancing contours where contrast changes sharply and in reducing the fading problems. Figure 12 shows a contour enhancement circuit.

Figure 12. Contour Enhancement Circuit



In this example, the video input is handled as a 4-bit signal so that a circuit with a delay length equal to two scanning lines can be configured with a single μPD42505. Adding adders or subtractors and multipliers to the μPD42505 completes the contour enhancement configuration.

The video signal of the n+1th line (delayed by one scanning line) is input to D_{IN0}-D_{IN3} and output from D_{OUT0}-D_{OUT3} as the nth line. Applying this output directly to D_{IN4}-D_{IN7} delays the video signal another scanning line before it is output from D_{OUT4}-D_{OUT7} as the n−1th line. There is a delay of one scanning line between the signal input to D_{IN0}-D_{IN3} and the signal output from D_{OUT0}-D_{OUT3}, and a delay of another scanning line between the signal input to D_{IN4}-D_{IN7} and the signal output from D_{OUT4}-D_{OUT7}. Processing these signals in the adders and multipliers provides contour enhancement in the vertical direction. You can control the delay length by controlling the reset signals ($\overline{RSTW}$ and $\overline{RSTR}$) and the clock signals (WCK and RCK) in common, and by controlling the reset signal input interval.

The delay length of one scanning line is used in various applications for two-dimensional data processing. The μPD42505 can also be used in applications such as VTR jitter compensation (time axis variation) caused by the variance in head drum rotation rate or the expansion or shrinkage of the tape, applications requiring variable-length delay lines to contract or expand a video image in the horizontal direction, applications involving the synchronization of two or more digital signal inputs, and as a line buffer in data transfer operations between devices using different data transfer rates.

Figure 13. μPD42505 5048 x 8 Line Buffer